# SHARP

PRELIMINARY DATASHEET

# DATASHEET

**PRODUCT :**  64M (x16) Flash Memory

**MODEL NO :**  *LH28F640BFHB-PBTL60*

*Refer to SHARP's Website (www.sharp.co.jp) for the latest information.*

- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

  - Office electronics
  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliance
  - Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment <u>which demands high reliability</u>, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

  - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  - Mainframe computers
  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment <u>which demands extremely high performance</u> in terms of functionality, reliability, or accuracy.

  - Aerospace equipment
  - Communications equipment for trunk lines
  - Control equipment for the nuclear power industry
  - Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

# CONTENTS

# LH28F640BFHB-PBTL60
# 64Mbit (4Mbit×16)
# Page Mode Dual Work Flash MEMORY

■ 64M density with 16Bit I/O Interface

■ High Performance Reads
  • 60/25ns 8-Word Page Mode

■ Configurative 4-Plane Dual Work
  • Flexible Partitioning
  • Read operations during Block Erase or (Page Buffer) Program
  • Status Register for Each Partition

■ Low Power Operation
  • 2.7V Read and Write Operations
  • $V_{CCQ}$ for Input/Output Power Supply Isolation
  • Automatic Power Savings Mode Reduces $I_{CCR}$ in Static Mode

■ Enhanced Code + Data Storage
  • 5μs Typical Erase/Program Suspends

■ OTP (One Time Program) Block
  • 4-Word Factory-Programmed Area
  • 4-Word User-Programmable Area

■ High Performance Program with Page Buffer
  • 16-Word Page Buffer
  • 5μs/Word (Typ.) at 12V $V_{PP}$

■ Operating Temperature -40°C to +85°C

■ CMOS Process (P-type silicon substrate)

■ Flexible Blocking Architecture
  • Eight 4K-word Parameter Blocks
  • One-hundred and twenty-seven 32K-word Main Blocks
  • Bottom Parameter Location

■ Enhanced Data Protection Features
  • Individual Block Lock and Block Lock-Down with Zero-Latency
  • All blocks are locked at power-up or device reset.
  • Absolute Protection with $V_{PP} \leq V_{PPLK}$
  • Block Erase, Full Chip Erase, (Page Buffer) Word Program Lockout during Power Transitions

■ Automated Erase/Program Algorithms
  • 3.0V Low-Power 11μs/Word (Typ.) Programming
  • 12V No Glue Logic 9μs/Word (Typ.) Production Programming and 0.5s Erase (Typ.)

■ Cross-Compatible Command Support
  • Basic Command Set
  • Common Flash Interface (CFI)

■ Extended Cycling Capability
  • Minimum 100,000 Block Erase Cycles

■ 0.8mm pitch 60-Ball CSP

■ ETOX$^{TM*}$ Flash Technology

■ Not designed or rated as radiation hardened

The product, which is 4-Plane Page Mode Dual Work (Simultaneous Read while Erase/Program) Flash memory, is a low power, high density, low cost, nonvolatile read/write storage solution for a wide range of applications. The product can operate at $V_{CC}$=2.7V-3.6V and $V_{PP}$=1.65V-3.6V or 11.7V-12.3V. Its low voltage operation capability greatly extends battery life for portable applications.

The product provides high performance asynchronous page mode. It allows code execution directly from Flash, thus eliminating time consuming wait states. Furthermore, its newly configurative partitioning architecture allows flexible dual work operation.

The memory array block architecture utilizes Enhanced Data Protection features, and provides separate Parameter and Main Blocks that provide maximum flexibility for safe nonvolatile code and data storage.

Fast program capability is provided through the use of high speed Page Buffer Program.

Special OTP (One Time Program) block provides an area to store permanent code such as a unique number.

* ETOX is a trademark of Intel Corporation.

60-BALL CSP
PINOUT
11mm x 8mm
TOP VIEW

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|----|----|----|
| A | NC | NC | NC | $A_{14}$ | $A_{13}$ | $A_{15}$ | $A_{16}$ | GND | $V_{CCQ}$ | NC | NC | NC |
| B |   |   |   | $A_{11}$ | $A_{10}$ | $A_{12}$ | $DQ_{15}$ | $DQ_{14}$ | $DQ_7$ |   |   |   |
| C |   |   |   | $A_8$ | $A_{20}$ | $A_9$ | $DQ_6$ | $DQ_5$ | $DQ_{13}$ |   |   |   |
| D |   |   |   | WE# | RST# | $A_{21}$ | $DQ_{12}$ | $V_{CC}$ | $DQ_4$ |   |   |   |
| E |   |   |   | WP# | $V_{PP}$ | $A_{19}$ | $DQ_{10}$ | $DQ_{11}$ | $DQ_3$ |   |   |   |
| F |   |   |   | $A_{17}$ | $A_{18}$ | $A_7$ | $DQ_1$ | $DQ_2$ | $DQ_9$ |   |   |   |
| G |   |   |   | $A_5$ | $A_6$ | $A_4$ | OE# | $DQ_8$ | $DQ_0$ |   |   |   |
| H | NC | NC | NC | $A_2$ | $A_3$ | $A_1$ | $A_0$ | GND | CE# | NC | NC | NC |
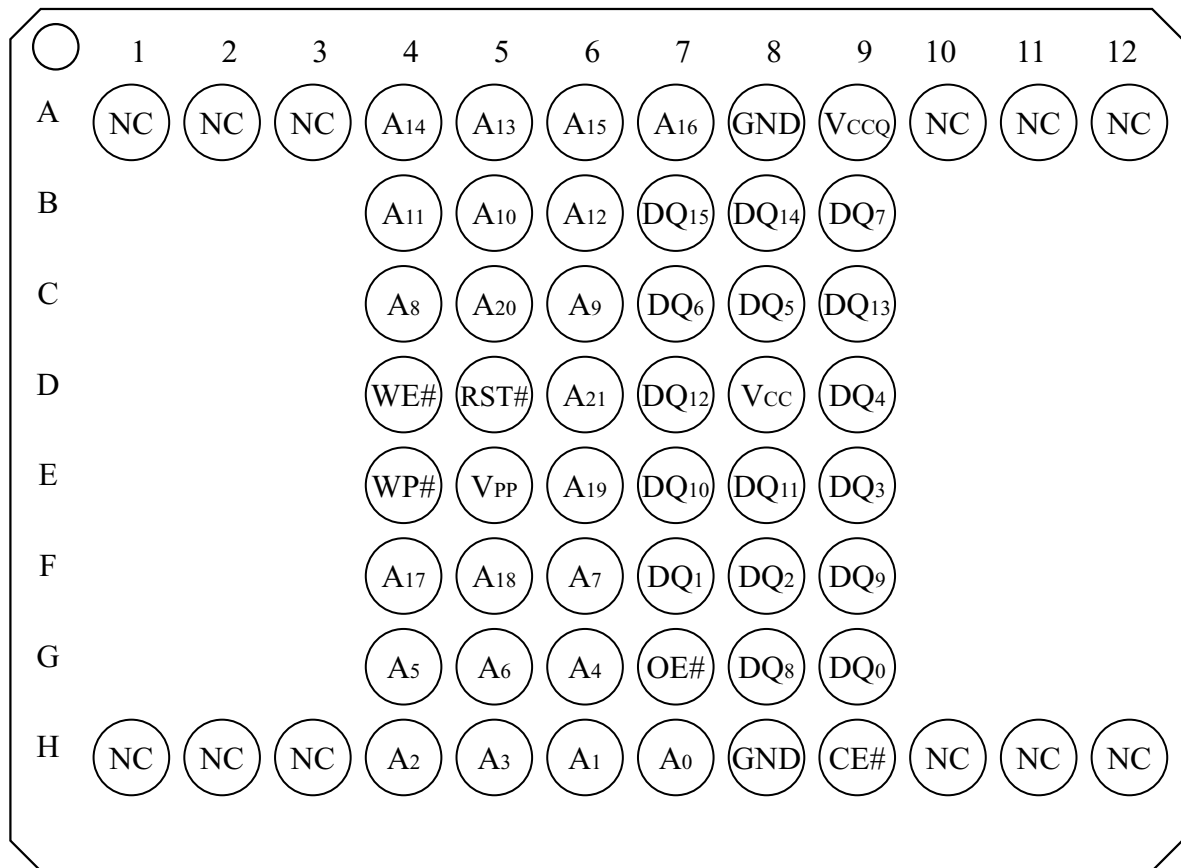
Figure 1.  0.8mm pitch 60-Ball CSP Pinout

Table 1.  Pin Descriptions

| Symbol | Type | Name and Function |
|---|---|---|
| $A_0$-$A_{21}$ | INPUT | ADDRESS INPUTS: Inputs for addresses. 64M: $A_0$-$A_{21}$ |
| $DQ_0$-$DQ_{15}$ | INPUT/ OUTPUT | DATA INPUTS/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query code, identifier code and partition configuration register code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle. |
| CE# | INPUT | CHIP ENABLE: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high ($V_{IH}$) deselects the device and reduces power consumption to standby levels. |
| RST# | INPUT | RESET: When low ($V_{IL}$), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high ($V_{IH}$) enables normal operation. After power-up or reset mode, the device is automatically set to read array mode. RST# must be low during power-up/down. |
| OE# | INPUT | OUTPUT ENABLE: Gates the device's outputs during a read cycle. |
| WE# | INPUT | WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first). |
| WP# | INPUT | WRITE PROTECT: When WP# is $V_{IL}$, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and not locked-down. When WP# is $V_{IH}$, lock-down is disabled. |
| $V_{PP}$ | INPUT | MONITORING POWER SUPPLY VOLTAGE: $V_{PP}$ is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V±0.3V to $V_{PP}$ provides fast erasing or fast programming mode. In this mode, $V_{PP}$ is power supply pin. Applying 12V±0.3V to $V_{PP}$ during erase/program can only be done for a maximum of 1,000 cycles on each block. $V_{PP}$ may be connected to 12V±0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage. |
| $V_{CC}$ | SUPPLY | DEVICE POWER SUPPLY (2.7V-3.6V): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid $V_{CC}$ voltage (see DC Characteristics) produce spurious results and should not be attempted. |
| $V_{CCQ}$ | SUPPLY | INPUT/OUTPUT POWER SUPPLY (2.7V-3.6V): Power supply for all input/output pins. |
| GND | SUPPLY | GROUND: Do not float any ground pins. |
| NC | | NO CONNECT: Lead is not internally connected; it may be driven or floated. |

Table 2. Simultaneous Operation Modes Allowed with Four Planes[1, 2]

| IF ONE PARTITION IS: | THEN THE MODES ALLOWED IN THE OTHER PARTITION IS: | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Read Array | Read ID/OTP | Read Status | Read Query | Word Program | Page Buffer Program | OTP Program | Block Erase | Full Chip Erase | Program Suspend | Block Erase Suspend |
| Read Array | X | X | X | X | X | X | | X | | X | X |
| Read ID/OTP | X | X | X | X | X | X | | X | | X | X |
| Read Status | X | X | X | X | X | X | X | X | X | X | X |
| Read Query | X | X | X | X | X | X | | X | | X | X |
| Word Program | X | X | X | X | | | | | | | X |
| Page Buffer Program | X | X | X | X | | | | | | | X |
| OTP Program | | | X | | | | | | | | |
| Block Erase | X | X | X | X | | | | | | | |
| Full Chip Erase | | | X | | | | | | | | |
| Program Suspend | X | X | X | X | | | | | | | X |
| Block Erase Suspend | X | X | X | X | X | X | | | | X | |

NOTES:
1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition. Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.

| BLOCK NUMBER | | ADDRESS RANGE |
|---|---|---|
| 70 | 32K-WORD | 1F8000H - 1FFFFFH |
| 69 | 32K-WORD | 1F0000H - 1F7FFFH |
| 68 | 32K-WORD | 1E8000H - 1EFFFFH |
| 67 | 32K-WORD | 1E0000H - 1E7FFFH |
| 66 | 32K-WORD | 1D8000H - 1DFFFFH |
| 65 | 32K-WORD | 1D0000H - 1D7FFFH |
| 64 | 32K-WORD | 1C8000H - 1CFFFFH |
| 63 | 32K-WORD | 1C0000H - 1C7FFFH |
| 62 | 32K-WORD | 1B8000H - 1BFFFFH |
| 61 | 32K-WORD | 1B0000H - 1B7FFFH |
| 60 | 32K-WORD | 1A8000H - 1AFFFFH |
| 59 | 32K-WORD | 1A0000H - 1A7FFFH |
| 58 | 32K-WORD | 198000H - 19FFFFH |
| 57 | 32K-WORD | 190000H - 197FFFH |
| 56 | 32K-WORD | 188000H - 18FFFFH |
| 55 | 32K-WORD | 180000H - 187FFFH |
| 54 | 32K-WORD | 178000H - 17FFFFH |
| 53 | 32K-WORD | 170000H - 177FFFH |
| 52 | 32K-WORD | 168000H - 16FFFFH |
| 51 | 32K-WORD | 160000H - 167FFFH |
| 50 | 32K-WORD | 158000H - 15FFFFH |
| 49 | 32K-WORD | 150000H - 157FFFH |
| 48 | 32K-WORD | 148000H - 14FFFFH |
| 47 | 32K-WORD | 140000H - 147FFFH |
| 46 | 32K-WORD | 138000H - 13FFFFH |
| 45 | 32K-WORD | 130000H - 137FFFH |
| 44 | 32K-WORD | 128000H - 12FFFFH |
| 43 | 32K-WORD | 120000H - 127FFFH |
| 42 | 32K-WORD | 118000H - 11FFFFH |
| 41 | 32K-WORD | 110000H - 117FFFH |
| 40 | 32K-WORD | 108000H - 10FFFFH |
| 39 | 32K-WORD | 100000H - 107FFFH |

PLANE1 (UNIFORM PLANE)

| BLOCK NUMBER | | ADDRESS RANGE |
|---|---|---|
| 134 | 32K-WORD | 3F8000H - 3FFFFFH |
| 133 | 32K-WORD | 3F0000H - 3F7FFFH |
| 132 | 32K-WORD | 3E8000H - 3EFFFFH |
| 131 | 32K-WORD | 3E0000H - 3E7FFFH |
| 130 | 32K-WORD | 3D8000H - 3DFFFFH |
| 129 | 32K-WORD | 3D0000H - 3D7FFFH |
| 128 | 32K-WORD | 3C8000H - 3CFFFFH |
| 127 | 32K-WORD | 3C0000H - 3C7FFFH |
| 126 | 32K-WORD | 3B8000H - 3BFFFFH |
| 125 | 32K-WORD | 3B0000H - 3B7FFFH |
| 124 | 32K-WORD | 3A8000H - 3AFFFFH |
| 123 | 32K-WORD | 3A0000H - 3A7FFFH |
| 122 | 32K-WORD | 398000H - 39FFFFH |
| 121 | 32K-WORD | 390000H - 397FFFH |
| 120 | 32K-WORD | 388000H - 38FFFFH |
| 119 | 32K-WORD | 380000H - 387FFFH |
| 118 | 32K-WORD | 378000H - 37FFFFH |
| 117 | 32K-WORD | 370000H - 377FFFH |
| 116 | 32K-WORD | 368000H - 36FFFFH |
| 115 | 32K-WORD | 360000H - 367FFFH |
| 114 | 32K-WORD | 358000H - 35FFFFH |
| 113 | 32K-WORD | 350000H - 357FFFH |
| 112 | 32K-WORD | 348000H - 34FFFFH |
| 111 | 32K-WORD | 340000H - 347FFFH |
| 110 | 32K-WORD | 338000H - 33FFFFH |
| 109 | 32K-WORD | 330000H - 337FFFH |
| 108 | 32K-WORD | 328000H - 32FFFFH |
| 107 | 32K-WORD | 320000H - 327FFFH |
| 106 | 32K-WORD | 318000H - 31FFFFH |
| 105 | 32K-WORD | 310000H - 317FFFH |
| 104 | 32K-WORD | 308000H - 30FFFFH |
| 103 | 32K-WORD | 300000H - 307FFFH |

PLANE3 (UNIFORM PLANE)

| 38 | 32K-WORD | 0F8000H - 0FFFFFH |
|---|---|---|
| 37 | 32K-WORD | 0F0000H - 0F7FFFH |
| 36 | 32K-WORD | 0E8000H - 0EFFFFH |
| 35 | 32K-WORD | 0E0000H - 0E7FFFH |
| 34 | 32K-WORD | 0D8000H - 0DFFFFH |
| 33 | 32K-WORD | 0D0000H - 0D7FFFH |
| 32 | 32K-WORD | 0C8000H - 0CFFFFH |
| 31 | 32K-WORD | 0C0000H - 0C7FFFH |
| 30 | 32K-WORD | 0B8000H - 0BFFFFH |
| 29 | 32K-WORD | 0B0000H - 0B7FFFH |
| 28 | 32K-WORD | 0A8000H - 0AFFFFH |
| 27 | 32K-WORD | 0A0000H - 0A7FFFH |
| 26 | 32K-WORD | 098000H - 09FFFFH |
| 25 | 32K-WORD | 090000H - 097FFFH |
| 24 | 32K-WORD | 088000H - 08FFFFH |
| 23 | 32K-WORD | 080000H - 087FFFH |
| 22 | 32K-WORD | 078000H - 07FFFFH |
| 21 | 32K-WORD | 070000H - 077FFFH |
| 20 | 32K-WORD | 068000H - 06FFFFH |
| 19 | 32K-WORD | 060000H - 067FFFH |
| 18 | 32K-WORD | 058000H - 05FFFFH |
| 17 | 32K-WORD | 050000H - 057FFFH |
| 16 | 32K-WORD | 048000H - 04FFFFH |
| 15 | 32K-WORD | 040000H - 047FFFH |
| 14 | 32K-WORD | 038000H - 03FFFFH |
| 13 | 32K-WORD | 030000H - 037FFFH |
| 12 | 32K-WORD | 028000H - 02FFFFH |
| 11 | 32K-WORD | 020000H - 027FFFH |
| 10 | 32K-WORD | 018000H - 01FFFFH |
| 9 | 32K-WORD | 010000H - 017FFFH |
| 8 | 32K-WORD | 008000H - 00FFFFH |
| 7 | 4K-WORD | 007000H - 007FFFH |
| 6 | 4K-WORD | 006000H - 006FFFH |
| 5 | 4K-WORD | 005000H - 005FFFH |
| 4 | 4K-WORD | 004000H - 004FFFH |
| 3 | 4K-WORD | 003000H - 003FFFH |
| 2 | 4K-WORD | 002000H - 002FFFH |
| 1 | 4K-WORD | 001000H - 001FFFH |
| 0 | 4K-WORD | 000000H - 000FFFH |

PLANE0 (PARAMETER PLANE)

| 102 | 32K-WORD | 2F8000H - 2FFFFFH |
|---|---|---|
| 101 | 32K-WORD | 2F0000H - 2F7FFFH |
| 100 | 32K-WORD | 2E8000H - 2EFFFFH |
| 99 | 32K-WORD | 2E0000H - 2E7FFFH |
| 98 | 32K-WORD | 2D8000H - 2DFFFFH |
| 97 | 32K-WORD | 2D0000H - 2D7FFFH |
| 96 | 32K-WORD | 2C8000H - 2CFFFFH |
| 95 | 32K-WORD | 2C0000H - 2C7FFFH |
| 94 | 32K-WORD | 2B8000H - 2BFFFFH |
| 93 | 32K-WORD | 2B0000H - 2B7FFFH |
| 92 | 32K-WORD | 2A8000H - 2AFFFFH |
| 91 | 32K-WORD | 2A0000H - 2A7FFFH |
| 90 | 32K-WORD | 298000H - 29FFFFH |
| 89 | 32K-WORD | 290000H - 297FFFH |
| 88 | 32K-WORD | 288000H - 28FFFFH |
| 87 | 32K-WORD | 280000H - 287FFFH |
| 86 | 32K-WORD | 278000H - 27FFFFH |
| 85 | 32K-WORD | 270000H - 277FFFH |
| 84 | 32K-WORD | 268000H - 26FFFFH |
| 83 | 32K-WORD | 260000H - 267FFFH |
| 82 | 32K-WORD | 258000H - 25FFFFH |
| 81 | 32K-WORD | 250000H - 257FFFH |
| 80 | 32K-WORD | 248000H - 24FFFFH |
| 79 | 32K-WORD | 240000H - 247FFFH |
| 78 | 32K-WORD | 238000H - 23FFFFH |
| 77 | 32K-WORD | 230000H - 237FFFH |
| 76 | 32K-WORD | 228000H - 22FFFFH |
| 75 | 32K-WORD | 220000H - 227FFFH |
| 74 | 32K-WORD | 218000H - 21FFFFH |
| 73 | 32K-WORD | 210000H - 217FFFH |
| 72 | 32K-WORD | 208000H - 20FFFFH |
| 71 | 32K-WORD | 200000H - 207FFFH |

PLANE2 (UNIFORM PLANE)

Figure 2.  Memory Map (Bottom Parameter)

Table 3. Identifier Codes and OTP Address for Read Operation

| | Code | Address [$A_{15}$-$A_0$] | Data [$DQ_{15}$-$DQ_0$] | Notes |
|---|---|---|---|---|
| Manufacturer Code | Manufacturer Code | 0000H | 00B0H | 1 |
| Device Code | Bottom Parameter Device Code | 0001H | 00B1H | 1, 2 |
| Block Lock Configuration Code | Block is Unlocked | Block Address + 2 | $DQ_0 = 0$ | 3 |
| | Block is Locked | | $DQ_0 = 1$ | 3 |
| | Block is not Locked-Down | | $DQ_1 = 0$ | 3 |
| | Block is Locked-Down | | $DQ_1 = 1$ | 3 |
| Device Configuration Code | Partition Configuration Register | 0006H | PCRC | 1, 4 |
| OTP | OTP Lock | 0080H | OTP-LK | 1, 5 |
| | OTP | 0081-0088H | OTP | 1, 6 |

NOTES:
1. The address $A_{21}$-$A_{16}$ are shown in below table for reading the manufacturer code, device code, device configuration code and OTP data.
2. Bottom parameter device has its parameter blocks in the plane0 (The lowest address).
3. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes/OTP command (90H) has been written.
   $DQ_{15}$-$DQ_2$ are reserved for future implementation.
4. PCRC=Partition Configuration Register Code.
5. OTP-LK=OTP Block Lock configuration.
6. OTP=OTP Block data.

Table 4. Identifier Codes and OTP Address for Read Operation on Partition Configuration[1] (64M-bit device)

| Partition Configuration Register [2] | | | Address (64M-bit device) |
|---|---|---|---|
| PCR.10 | PCR.9 | PCR.8 | [$A_{21}$-$A_{16}$] |
| 0 | 0 | 0 | 00H |
| 0 | 0 | 1 | 00H or 10H |
| 0 | 1 | 0 | 00H or 20H |
| 1 | 0 | 0 | 00H or 30H |
| 0 | 1 | 1 | 00H or 10H or 20H |
| 1 | 1 | 0 | 00H or 20H or 30H |
| 1 | 0 | 1 | 00H or 10H or 30H |
| 1 | 1 | 1 | 00H or 10H or 20H or 30H |

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).
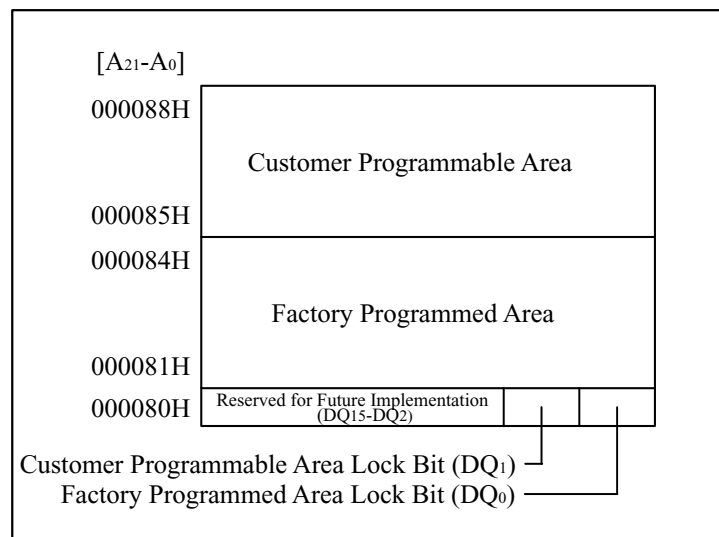2. Refer to Table 12 for the partition configuration register.

$[A_{21}-A_0]$

| Address | |
|---|---|
| 000088H | Customer Programmable Area |
| 000085H | |
| 000084H | Factory Programmed Area |
| 000081H | |
| 000080H | Reserved for Future Implementation (DQ15-DQ2) |

Customer Programmable Area Lock Bit (DQ1)

Factory Programmed Area Lock Bit (DQ0)

Figure 3.  OTP Block Address Map for OTP Program
(The area outside 80H~88H cannot be used.)

Table 5.  Bus Operation[1, 2]

| Mode | Notes | RST# | CE# | OE# | WE# | Address | $V_{PP}$ | $DQ_{0-15}$ |
|---|---|---|---|---|---|---|---|---|
| Read Array | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | X | X | $D_{OUT}$ |
| Output Disable | | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | X | High Z |
| Standby | | $V_{IH}$ | $V_{IH}$ | X | X | X | X | High Z |
| Reset | 3 | $V_{IL}$ | X | X | X | X | X | High Z |
| Read Identifier Codes/OTP | 6 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | See Table 3 and Table 4 | X | See Table 3 and Table 4 |
| Read Query | 6,7 | $V_{IH}$ | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | See Appendix | X | See Appendix |
| Write | 4,5,6 | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | X | X | $D_{IN}$ |

NOTES:
1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be $V_{IL}$ or $V_{IH}$ for control pins and addresses, and $V_{PPLK}$ or $V_{PPH1/2}$ for $V_{PP}$. See DC Characteristics for $V_{PPLK}$ and $V_{PPH1/2}$ voltages.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when $V_{PP} = V_{PPH1/2}$ and $V_{CC} = 2.7V$-$3.6V$.
5. Refer to Table 6 for valid $D_{IN}$ during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LH28F640BF series for more information about query code.

Table 6.  Command Definitions[11]

| Command | Bus Cycles Req'd | Notes | First Bus Cycle | | | Second Bus Cycle | | |
|---|---|---|---|---|---|---|---|---|
| | | | Oper[1] | Addr[2] | Data | Oper[1] | Addr[2] | Data[3] |
| Read Array | 1 | | Write | PA | FFH | | | |
| Read Identifier Codes/OTP | ≥ 2 | 4 | Write | PA | 90H | Read | IA or OA | ID or OD |
| Read Query | ≥ 2 | 4 | Write | PA | 98H | Read | QA | QD |
| Read Status Register | 2 | | Write | PA | 70H | Read | PA | SRD |
| Clear Status Register | 1 | | Write | PA | 50H | | | |
| Block Erase | 2 | 5 | Write | BA | 20H | Write | BA | D0H |
| Full Chip Erase | 2 | 5,9 | Write | X | 30H | Write | X | D0H |
| Program | 2 | 5,6 | Write | WA | 40H or 10H | Write | WA | WD |
| Page Buffer Program | ≥ 4 | 5,7 | Write | WA | E8H | Write | WA | N-1 |
| Block Erase and (Page Buffer) Program Suspend | 1 | 8,9 | Write | PA | B0H | | | |
| Block Erase and (Page Buffer) Program Resume | 1 | 8,9 | Write | PA | D0H | | | |
| Set Block Lock Bit | 2 | | Write | BA | 60H | Write | BA | 01H |
| Clear Block Lock Bit | 2 | 10 | Write | BA | 60H | Write | BA | D0H |
| Set Block Lock-down Bit | 2 | | Write | BA | 60H | Write | BA | 2FH |
| OTP Program | 2 | 9 | Write | OA | C0H | Write | OA | OD |
| Set Partition Configuration Register | 2 | | Write | PCRC | 60H | Write | PCRC | 04H |

NOTES:

1. Bus operations are defined in Table 5.

2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.

   X=Any valid address within the device.

   PA=Address within the selected partition.

   IA=Identifier codes address (See Table 3 and Table 4).

   QA=Query codes address. Refer to Appendix of LH28F640BF series for details.

   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.

   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.

   OA=Address of OTP block to be read or programmed (See Figure 3).

   PCRC=Partition configuration register code presented on the address $A_0$-$A_{15}$.

3. ID=Data read from identifier codes. (See Table 3 and Table 4).

   QD=Data read from query database. Refer to Appendix of LH28F640BF series for details.

   SRD=Data read from status register. See Table 10 and Table 11 for a description of the status register bits.

   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.

   OD=Data within OTP block. Data is latched on the rising edge of WE# or CE# (whichever goes high first) during command write cycles.

   N-1=N is the number of the words to be loaded into a page buffer.

4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See Table 3 and Table 4).

   The Read Query command is available for reading CFI (Common Flash Interface) information.

5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is $V_{IH}$.

6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.

7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to Appendix of

LH28F640BF series for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.

9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.

10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is $V_{IL}$. When WP# is $V_{IH}$, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.

11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 7.  Functions of Block Lock[5] and Block Lock-Down

| Current State | | | | | Erase/Program Allowed [2] |
|---|---|---|---|---|---|
| State | WP# | $DQ_1$ [1] | $DQ_0$ [1] | State Name | |
| [000] | 0 | 0 | 0 | Unlocked | Yes |
| [001][3] | 0 | 0 | 1 | Locked | No |
| [011] | 0 | 1 | 1 | Locked-down | No |
| [100] | 1 | 0 | 0 | Unlocked | Yes |
| [101][3] | 1 | 0 | 1 | Locked | No |
| [110][4] | 1 | 1 | 0 | Lock-down Disable | Yes |
| [111] | 1 | 1 | 1 | Lock-down Disable | No |

NOTES:
1. $DQ_0$=1: a block is locked; $DQ_0$=0: a block is unlocked.
   $DQ_1$=1: a block is locked-down; $DQ_1$=0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation.
4. When WP# is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
5. OTP (One Time Program) block has the lock function which is different from those described above.

Table 8.  Block Locking State Transitions upon Command Write[4]

| Current State | | | Result after Lock Command Written (Next State) | | |
|---|---|---|---|---|---|
| State | WP# | $DQ_1$ | $DQ_0$ | Set Lock[1] | Clear Lock[1] | Set Lock-down[1] |
| [000] | 0 | 0 | 0 | [001] | No Change | [011][2] |
| [001] | 0 | 0 | 1 | No Change[3] | [000] | [011] |
| [011] | 0 | 1 | 1 | No Change | No Change | No Change |
| [100] | 1 | 0 | 0 | [101] | No Change | [111][2] |
| [101] | 1 | 0 | 1 | No Change | [100] | [111] |
| [110] | 1 | 1 | 0 | [111] | No Change | [111][2] |
| [111] | 1 | 1 | 1 | No Change | [110] | No Change |

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block ($DQ_0$=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP# is not changed and fixed $V_{IL}$ or $V_{IH}$.

Table 9.  Block Locking State Transitions upon WP# Transition[4]

| Previous State | Current State | | | | Result after WP# Transition (Next State) | |
|---|---|---|---|---|---|---|
| | State | WP# | $DQ_1$ | $DQ_0$ | WP#=0→1[1] | WP#=1→0[1] |
| - | [000] | 0 | 0 | 0 | [100] | - |
| - | [001] | 0 | 0 | 1 | [101] | - |
| [110][2] | [011] | 0 | 1 | 1 | [110] | - |
| Other than [110][2] | | | | | [111] | - |
| - | [100] | 1 | 0 | 0 | - | [000] |
| - | [101] | 1 | 0 | 1 | - | [001] |
| - | [110] | 1 | 1 | 0 | - | [011][3] |
| - | [111] | 1 | 1 | 1 | - | [011] |

NOTES:

1. "WP#=0→1" means that WP# is driven to $V_{IH}$ and "WP#=1→0" means that WP# is driven to $V_{IL}$.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP# is driven to $V_{IL}$ in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

Table 10.  Status Register Definition

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| WSMS | BESS | BEFCES | PBPOPS | VPPS | PBPSS | DPS | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| | NOTES: |
|---|---|
| SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R) | |
| SR.7 = WRITE STATE MACHINE STATUS (WSMS)<br>   1 = Ready<br>   0 = Busy | Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration. |
| SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)<br>   1 = Block Erase Suspended<br>   0 = Block Erase in Progress/Completed | Check SR.7 to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.1 are invalid while SR.7="0". |
| SR.5 = BLOCK ERASE AND FULL CHIP ERASE<br>      STATUS (BEFCES)<br>   1 = Error in Block Erase or Full Chip Erase<br>   0 = Successful Block Erase or Full Chip Erase | If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit, set partition configuration register attempt, an improper command sequence was entered. |
| SR.4 = (PAGE BUFFER) PROGRAM AND<br>      OTP PROGRAM STATUS (PBPOPS)<br>   1 = Error in (Page Buffer) Program or OTP Program<br>   0 = Successful (Page Buffer) Program or OTP Program | SR.3 does not provide a continuous indication of $V_{PP}$ level. The WSM interrogates and indicates the $V_{PP}$ level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1}$, $V_{PPH2}$ or $V_{PPLK}$. |
| SR.3 = $V_{PP}$ STATUS (VPPS)<br>   1 = $V_{PP}$ LOW Detect, Operation Abort<br>   0 = $V_{PP}$ OK | |
| SR.2 = (PAGE BUFFER) PROGRAM SUSPEND<br>      STATUS (PBPSS)<br>   1 = (Page Buffer) Program Suspended<br>   0 = (Page Buffer) Program in Progress/Completed | SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status. |
| SR.1 = DEVICE PROTECT STATUS (DPS)<br>   1 = Erase or Program Attempted on a<br>      Locked Block, Operation Abort<br>   0 = Unlocked | SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register. |
| SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | |

Table 11.  Extended Status Register Definition

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SMS | R | R | R | R | R | R | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)<br><br>XSR.7 = STATE MACHINE STATUS (SMS)<br>  1 = Page Buffer Program available<br>  0 = Page Buffer Program not available<br><br>XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | NOTES:<br>After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.<br><br>XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register. |

Table 12.  Partition Configuration Register Definition

| R | R | R | R | R | PC2 | PC1 | PC0 |
|---|---|---|---|---|-----|-----|-----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| R | R | R | R | R | R | R | R |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

PCR.15-11 = RESERVED FOR FUTURE
 ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)
 000 = No partitioning. Dual Work is not allowed.
 001 = Plane1-3 are merged into one partition.
 (default in a bottom parameter device)
 010 = Plane 0-1 and Plane2-3 are merged into one
 partition respectively.
 100 = Plane 0-2 are merged into one partition.
 (default in a top parameter device)
 011 = Plane 2-3 are merged into one partition. There are
 three partitions in this configuration. Dual work
 operation is available between any two partitions.
 110 = Plane 0-1 are merged into one partition. There are
 three partitions in this configuration. Dual work
 operation is available between any two partitions.
 101 = Plane 1-2 are merged into one partition. There are
 three partitions in this configuration. Dual work
 operation is available between any two partitions.

 111 = There are four partitions in this configuration.
 Each plane corresponds to each partition respec-
 tively. Dual work operation is available between any
 two partitions.

PCR.7-0 = RESERVED FOR FUTURE
 ENHANCEMENTS (R)

NOTES:

After power-up or device reset, PCR10-8 (PC2-0) is set to
"001" in a bottom parameter device and "100" in a top
parameter device.

See Figure 4 for the detail on partition configuration.

PCR.15-11 and PCR.7-0 are reserved for future use and
should be masked out when checking the partition
configuration register.



Figure 4.  Partition Configuration

# 1  Electrical Specifications

## 1.1  Absolute Maximum Ratings[*]

Operating Temperature

   During Read, Erase and Program ...-40°C to +85°C [(1)]

Storage Temperature

   During under Bias.............................. -40°C to +85°C
   During non Bias................................ -65°C to +125°C

Voltage On Any Pin

   (except $V_{CC}$ and $V_{PP}$).............. -0.5V to $V_{CC}$+0.5V [(2)]

$V_{CC}$ and $V_{CCQ}$ Supply Voltage .......... -0.2V to +3.9V [(2)]

$V_{PP}$ Supply Voltage .................... -0.2V to +12.6V [(2, 3, 4)]

Output Short Circuit Current ........................... 100mA [(5)]

*WARNING:* Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

NOTES:
1. Operating temperature is for extended temperature product defined by this specification.
2. All specified voltages are with respect to GND. Minimum DC voltage is -0.5V on input/output pins and -0.2V on $V_{CC}$ and $V_{PP}$ pins. During transitions, this level may undershoot to -2.0V for periods <20ns. Maximum DC voltage on input/output pins is $V_{CC}$+0.5V which, during transitions, may overshoot to $V_{CC}$+2.0V for periods <20ns.
3. Maximum DC voltage on $V_{PP}$ may overshoot to +13.0V for periods <20ns.
4. $V_{PP}$ erase/program voltage is normally 2.7V-3.6V. Applying 11.7V-12.3V to $V_{PP}$ during erase/program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. $V_{PP}$ may be connected to 11.7V-12.3V for a total of 80 hours maximum.
5. Output shorted for no more than one second. No more than one output shorted at a time.

## 1.2  Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| Operating Temperature | $T_A$ | -40 | +25 | +85 | °C | |
| $V_{CC}$ Supply Voltage | $V_{CC}$ | 2.7 | 3.0 | 3.6 | V | 1 |
| I/O Supply Voltage | $V_{CCQ}$ | 2.7 | 3.0 | 3.6 | V | 1 |
| $V_{PP}$ Voltage when Used as a Logic Control | $V_{PPH1}$ | 1.65 | 3.0 | 3.6 | V | 1 |
| $V_{PP}$ Supply Voltage | $V_{PPH2}$ | 11.7 | 12 | 12.3 | V | 1, 2 |
| Main Block Erase Cycling: $V_{PP}=V_{PPH1}$ | | 100,000 | | | Cycles | |
| Parameter Block Erase Cycling: $V_{PP}=V_{PPH1}$ | | 100,000 | | | Cycles | |
| Main Block Erase Cycling: $V_{PP}=V_{PPH2}$, 80 hrs. | | | | 1,000 | Cycles | |
| Parameter Block Erase Cycling: $V_{PP}=V_{PPH2}$, 80 hrs. | | | | 1,000 | Cycles | |
| Maximum $V_{PP}$ hours at $V_{PPH2}$ | | | | 80 | Hours | |

NOTES:
1. See DC Characteristics tables for voltage range-specific specification.
2. Applying $V_{PP}$=11.7V-12.3V during a erase or program can be done for a maximum of 1,000 cycles on the main blocks and 1,000 cycles on the parameter blocks. A permanent connection to $V_{PP}$=11.7V-12.3V is not allowed and can cause damage to the device.

## 1.2.1  Capacitance[1] ($T_A$=+25°C, f=1MHz)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-----------|--------|-----------|------|------|------|------|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0.0V | | 4 | 7 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0.0V | | 6 | 10 | pF |

NOTE:
1. Sampled, not 100% tested.

## 1.2.2  AC Input/Output Test Conditions



AC test inputs are driven at $V_{CCQ}$(min) for a Logic "1" and 0.0V for a Logic "0".
Input timing begins, and output timing ends at $V_{CCQ}$/2. Input rise and fall times (10% to 90%) < 5ns.
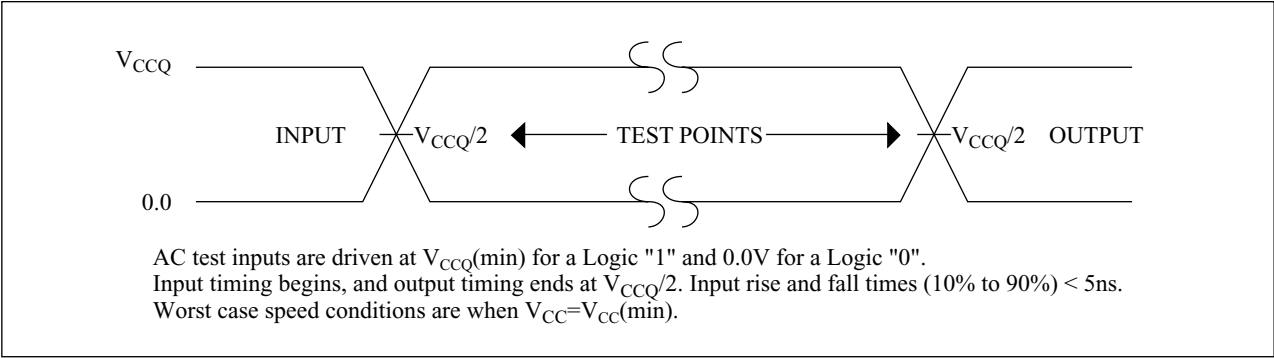Worst case speed conditions are when $V_{CC}$=$V_{CC}$(min).

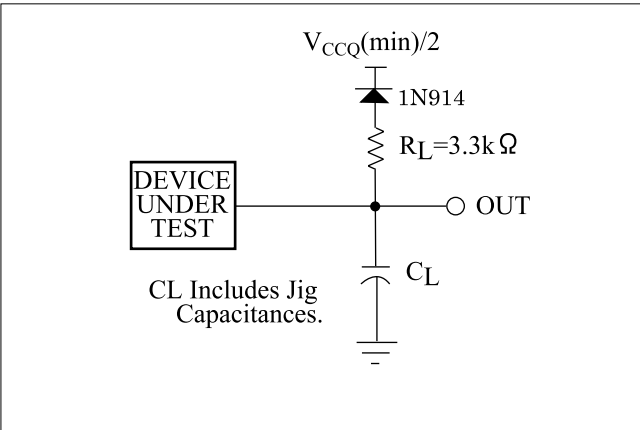Figure 5.  Transient Input/Output Reference Waveform for $V_{CC}$=2.7V-3.6V



Figure 6.  Transient Equivalent Testing Load Circuit

Table 13.  Configuration Capacitance Loading Value

| Test Configuration | $C_L$ (pF) |
|--------------------|------------|
| $V_{CC}$=2.7V-3.6V | 30pF, 50pF, 70pF |

## 1.2.3  DC Characteristics

$V_{CC}$=2.7V-3.6V

| Symbol | Parameter | | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | | 1 | -1.0 | | +1.0 | μA | $V_{CC}=V_{CC}$Max., $V_{CCQ}=V_{CCQ}$Max., $V_{IN}/V_{OUT}=V_{CCQ}$ or GND |
| $I_{LO}$ | Output Leakage Current | | 1 | -1.0 | | +1.0 | μA | |
| $I_{CCS}$ | $V_{CC}$ Standby Current | | 1 | | 4 | 20 | μA | $V_{CC}=V_{CC}$Max., CE#=RST#= $V_{CCQ}\pm0.2V$, WP#=$V_{CCQ}$ or GND |
| $I_{CCAS}$ | $V_{CC}$ Automatic Power Savings Current | | 1,4 | | 4 | 20 | μA | $V_{CC}=V_{CC}$Max., CE#=GND±0.2V, WP#=$V_{CCQ}$ or GND |
| $I_{CCD}$ | $V_{CC}$ Reset Power-Down Current | | 1 | | 4 | 20 | μA | RST#=GND±0.2V |
| $I_{CCR}$ | Average $V_{CC}$ Read Current Normal Mode | | 1,7 | | 15 | 25 | mA | $V_{CC}=V_{CC}$Max., CE#=$V_{IL}$, OE#=$V_{IH}$, f=5MHz |
| | Average $V_{CC}$ Read Current Page Mode | 8 Word Read | 1,7 | | 5 | 10 | mA | |
| $I_{CCW}$ | $V_{CC}$ (Page Buffer) Program Current | | 1,5,7 | | 20 | 60 | mA | $V_{PP}=V_{PPH1}$ |
| | | | 1,5,7 | | 10 | 20 | mA | $V_{PP}=V_{PPH2}$ |
| $I_{CCE}$ | $V_{CC}$ Block Erase, Full Chip Erase Current | | 1,5,7 | | 10 | 30 | mA | $V_{PP}=V_{PPH1}$ |
| | | | 1,5,7 | | 4 | 10 | mA | $V_{PP}=V_{PPH2}$ |
| $I_{CCWS}$ $I_{CCES}$ | $V_{CC}$ (Page Buffer) Program or Block Erase Suspend Current | | 1,2,7 | | 10 | 200 | μA | CE#=$V_{IH}$ |
| $I_{PPS}$ $I_{PPR}$ | $V_{PP}$ Standby or Read Current | | 1,6,7 | | 2 | 5 | μA | $V_{PP}\leq V_{CC}$ |
| $I_{PPW}$ | $V_{PP}$ (Page Buffer) Program Current | | 1,5,6,7 | | 2 | 5 | μA | $V_{PP}=V_{PPH1}$ |
| | | | 1,5,6,7 | | 10 | 30 | mA | $V_{PP}=V_{PPH2}$ |
| $I_{PPE}$ | $V_{PP}$ Block Erase, Full Chip Erase Current | | 1,5,6,7 | | 2 | 5 | μA | $V_{PP}=V_{PPH1}$ |
| | | | 1,5,6,7 | | 5 | 15 | mA | $V_{PP}=V_{PPH2}$ |
| $I_{PPWS}$ | $V_{PP}$ (Page Buffer) Program Suspend Current | | 1,6,7 | | 2 | 5 | μA | $V_{PP}=V_{PPH1}$ |
| | | | 1,6,7 | | 10 | 200 | μA | $V_{PP}=V_{PPH2}$ |
| $I_{PPES}$ | $V_{PP}$ Block Erase Suspend Current | | 1,6,7 | | 2 | 5 | μA | $V_{PP}=V_{PPH1}$ |
| | | | 1,6,7 | | 10 | 200 | μA | $V_{PP}=V_{PPH2}$ |

DC Characteristics (Continued)

$V_{CC}$=2.7V-3.6V

| Symbol | Parameter | Notes | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | 5 | -0.4 | | 0.4 | V | |
| $V_{IH}$ | Input High Voltage | 5 | 2.4 | | $V_{CCQ}$ + 0.4 | V | |
| $V_{OL}$ | Output Low Voltage | 5 | | | 0.2 | V | $V_{CC}$=$V_{CC}$Min., $V_{CCQ}$=$V_{CCQ}$Min., $I_{OL}$=100μA |
| $V_{OH}$ | Output High Voltage | 5 | $V_{CCQ}$ -0.2 | | | V | $V_{CC}$=$V_{CC}$Min., $V_{CCQ}$=$V_{CCQ}$Min., $I_{OH}$=-100μA |
| $V_{PPLK}$ | $V_{PP}$ Lockout during Normal Operations | 3,5,6 | | | 0.4 | V | |
| $V_{PPH1}$ | $V_{PP}$ during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations | 6 | 1.65 | 3.0 | 3.6 | V | |
| $V_{PPH2}$ | $V_{PP}$ during Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program Operations | 6 | 11.7 | 12 | 12.3 | V | |
| $V_{LKO}$ | $V_{CC}$ Lockout Voltage | | 1.5 | | | V | |

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values are the reference values at $V_{CC}$=3.0V and $T_A$=+25°C unless $V_{CC}$ is specified.
2. $I_{CCWS}$ and $I_{CCES}$ are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of $I_{CCES}$ and $I_{CCR}$ or $I_{CCW}$. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of $I_{CCWS}$ and $I_{CCR}$.
3. Block erase, full chip erase, (page buffer) program and OTP program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed in the range between $V_{PPLK}$(max.) and $V_{PPH1}$(min.), between $V_{PPH1}$(max.) and $V_{PPH2}$(min.) and above $V_{PPH2}$(max.).
4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings ($t_{AVQV}$) provide new data when addresses are changed.
5. Sampled, not 100% tested.
6. $V_{PP}$ is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.
Applying 12V±0.3V to $V_{PP}$ provides fast erasing or fast programming mode. In this mode, $V_{PP}$ is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the $V_{CC}$ power bus.
Applying 12V±0.3V to $V_{PP}$ during erase/program can only be done for a maximum of 1,000 cycles on each block. $V_{PP}$ may be connected to 12V±0.3V for a total of 80 hours maximum.
7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.

## 1.2.4  AC Characteristics - Read-Only Operations[1]

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C, $C_L$=30pF

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Read Cycle Time | | 60 | | ns |
| $t_{AVQV}$ | Address to Output Delay | | | 60 | ns |
| $t_{ELQV}$ | CE# to Output Delay | 3 | | 60 | ns |
| $t_{APA}$ | Page Address Access Time | | | 25 | ns |
| $t_{GLQV}$ | OE# to Output Delay | 3 | | 20 | ns |
| $t_{PHQV}$ | RST# High to Output Delay | | | 150 | ns |
| $t_{EHQZ}$, $t_{GHQZ}$ | CE# or OE# to Output in High Z, Whichever Occurs First | 2 | | 20 | ns |
| $t_{ELQX}$ | CE# to Output in Low Z | 2 | 0 | | ns |
| $t_{GLQX}$ | OE# to Output in Low Z | 2 | 0 | | ns |
| $t_{OH}$ | Output Hold from First Occurring Address, CE# or OE# change | 2 | 0 | | ns |
| $t_{AVEL}$, $t_{AVGL}$ | Address Setup to CE#, OE# Going Low for Reading Status Register | 4, 6 | 10 | | ns |
| $t_{ELAX}$, $t_{GLAX}$ | Address Hold from CE#, OE# Going Low for Reading Status Register | 5, 6 | 30 | | ns |
| $t_{EHEL}$, $t_{GHGL}$ | CE#, OE# Pulse Width High for Reading Status Register | 6 | 15 | | ns |

NOTES:  Refer to NOTE 1 through NOTE 6 on next page.

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C, $C_L$=50pF

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{AVAV}$ | Read Cycle Time | | 65 | | ns |
| $t_{AVQV}$ | Address to Output Delay | | | 65 | ns |
| $t_{ELQV}$ | CE# to Output Delay | 3 | | 65 | ns |
| $t_{APA}$ | Page Address Access Time | | | 25 | ns |
| $t_{GLQV}$ | OE# to Output Delay | 3 | | 20 | ns |
| $t_{PHQV}$ | RST# High to Output Delay | | | 150 | ns |
| $t_{EHQZ}$, $t_{GHQZ}$ | CE# or OE# to Output in High Z, Whichever Occurs First | 2 | | 20 | ns |
| $t_{ELQX}$ | CE# to Output in Low Z | 2 | 0 | | ns |
| $t_{GLQX}$ | OE# to Output in Low Z | 2 | 0 | | ns |
| $t_{OH}$ | Output Hold from First Occurring Address, CE# or OE# change | 2 | 0 | | ns |
| $t_{AVEL}$, $t_{AVGL}$ | Address Setup to CE#, OE# Going Low for Reading Status Register | 4, 6 | 10 | | ns |
| $t_{ELAX}$, $t_{GLAX}$ | Address Hold from CE#, OE# Going Low for Reading Status Register | 5, 6 | 30 | | ns |
| $t_{EHEL}$, $t_{GHGL}$ | CE#, OE# Pulse Width High for Reading Status Register | 6 | 15 | | ns |

NOTES:  Refer to NOTE 1 through NOTE 6 on next page.

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C, $C_L$=70pF

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|--------|-----------|-------|------|------|------|
| $t_{AVAV}$ | Read Cycle Time | | 70 | | ns |
| $t_{AVQV}$ | Address to Output Delay | | | 70 | ns |
| $t_{ELQV}$ | CE# to Output Delay | 3 | | 70 | ns |
| $t_{APA}$ | Page Address Access Time | | | 30 | ns |
| $t_{GLQV}$ | OE# to Output Delay | 3 | | 25 | ns |
| $t_{PHQV}$ | RST# High to Output Delay | | | 150 | ns |
| $t_{EHQZ}$, $t_{GHQZ}$ | CE# or OE# to Output in High Z, Whichever Occurs First | 2 | | 25 | ns |
| $t_{ELQX}$ | CE# to Output in Low Z | 2 | 0 | | ns |
| $t_{GLQX}$ | OE# to Output in Low Z | 2 | 0 | | ns |
| $t_{OH}$ | Output Hold from First Occurring Address, CE# or OE# change | 2 | 0 | | ns |
| $t_{AVEL}$, $t_{AVGL}$ | Address Setup to CE#, OE# Going Low for Reading Status Register | 4, 6 | 10 | | ns |
| $t_{ELAX}$, $t_{GLAX}$ | Address Hold from CE#, OE# Going Low for Reading Status Register | 5, 6 | 30 | | ns |
| $t_{EHEL}$, $t_{GHGL}$ | CE#, OE# Pulse Width High for Reading Status Register | 6 | 15 | | ns |

NOTES:
1. See AC input/output reference waveform for timing measurements and maximum allowable input slew rate.
2. Sampled, not 100% tested.
3. OE# may be delayed up to $t_{ELQV}$ — $t_{GLQV}$ after the falling edge of CE# without impact to $t_{ELQV}$.
4. Address setup time ($t_{AVEL}$, $t_{AVGL}$) is defined from the falling edge of CE# or OE# (whichever goes low last).
5. Address hold time ($t_{ELAX}$, $t_{GLAX}$) is defined from the falling edge of CE# or OE# (whichever goes low last).
6. Specifications $t_{AVEL}$, $t_{AVGL}$, $t_{ELAX}$, $t_{GLAX}$ and $t_{EHEL}$, $t_{GHGL}$ for read operations apply to only status register read operations.
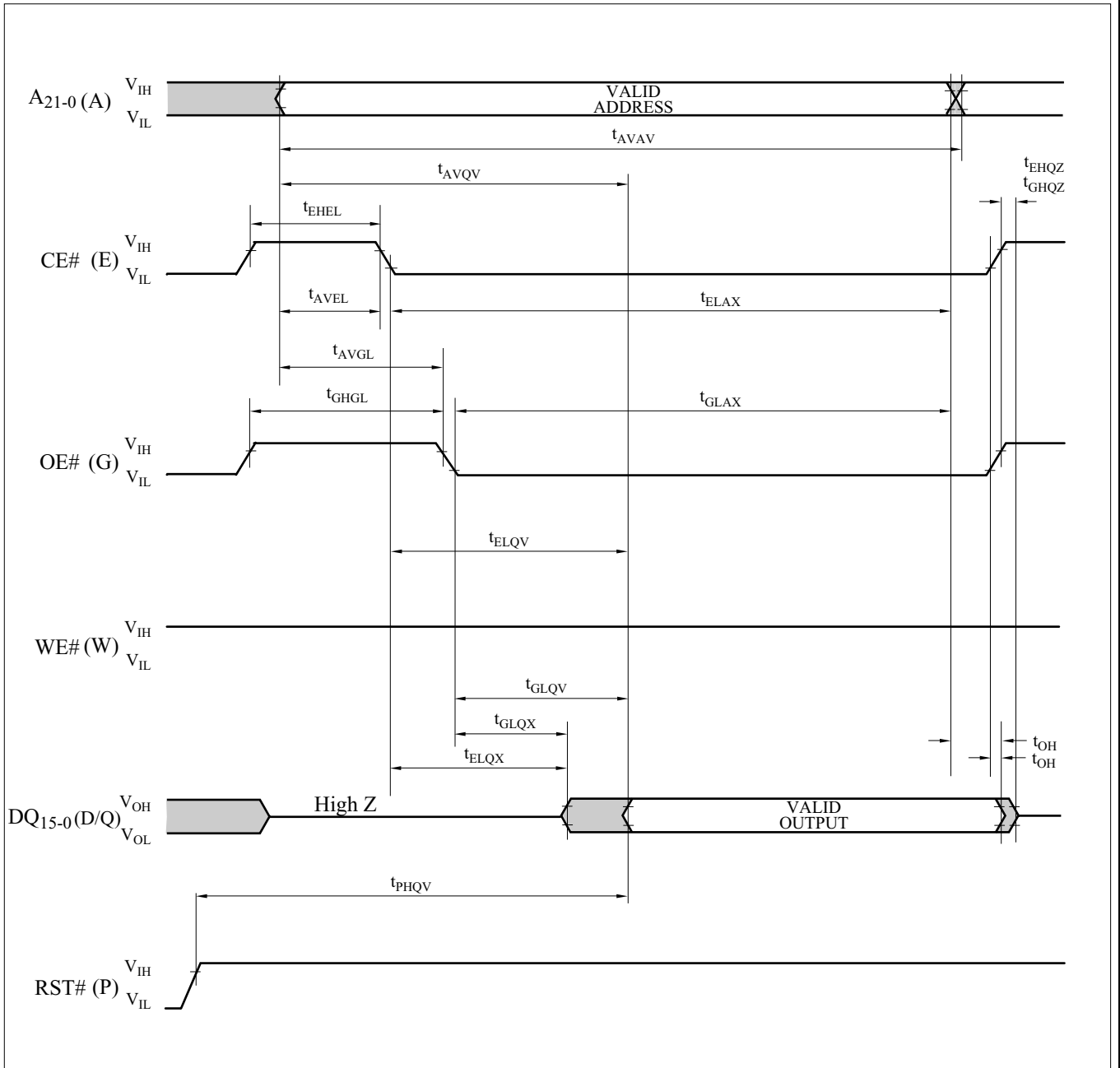
Figure 7.  AC Waveform for Single Asynchronous Read Operations
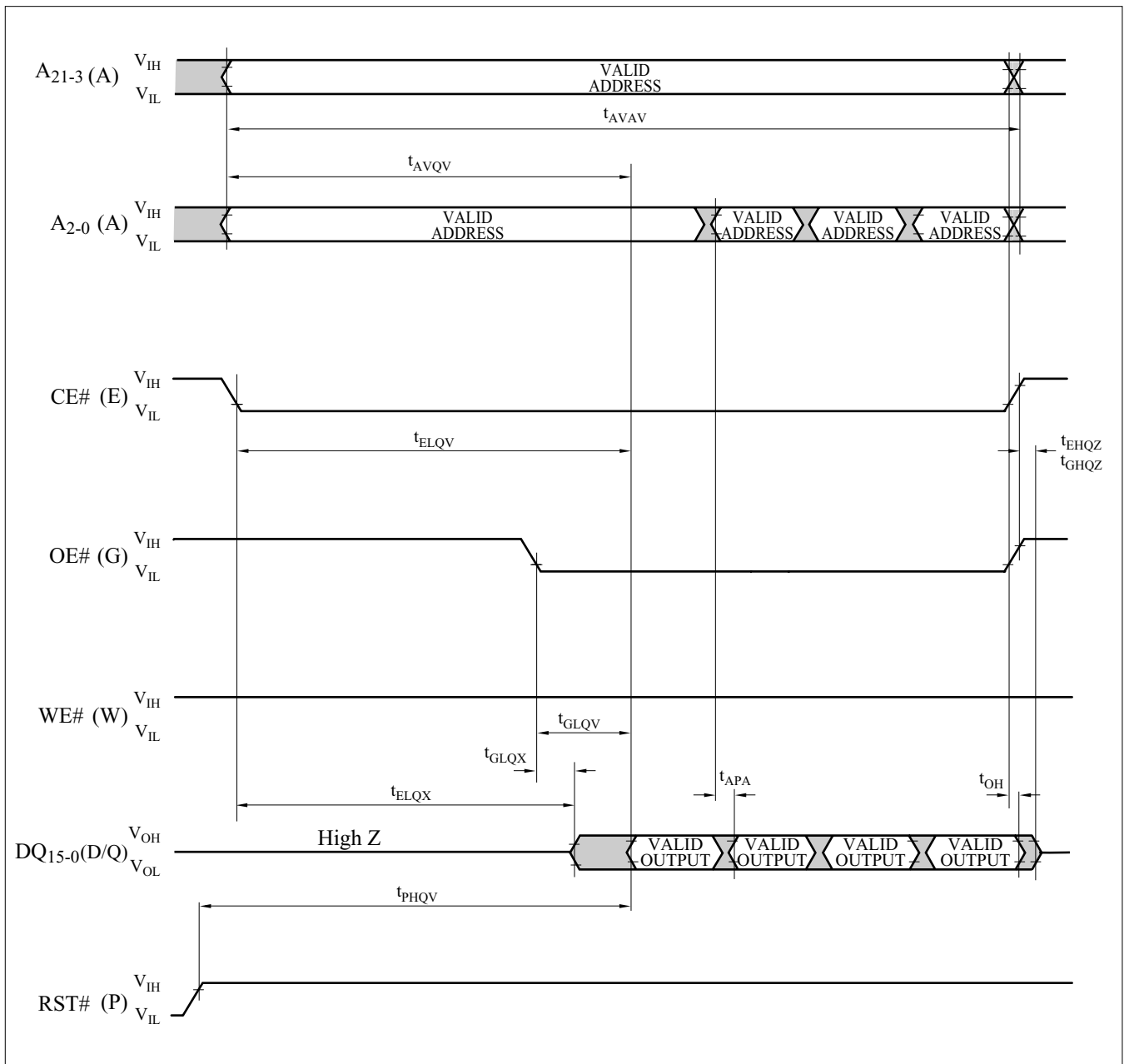from Status Register, Identifier Codes, OTP Block or Query Code

Figure 8.  AC Waveform for Asynchronous 4-Word Page Mode
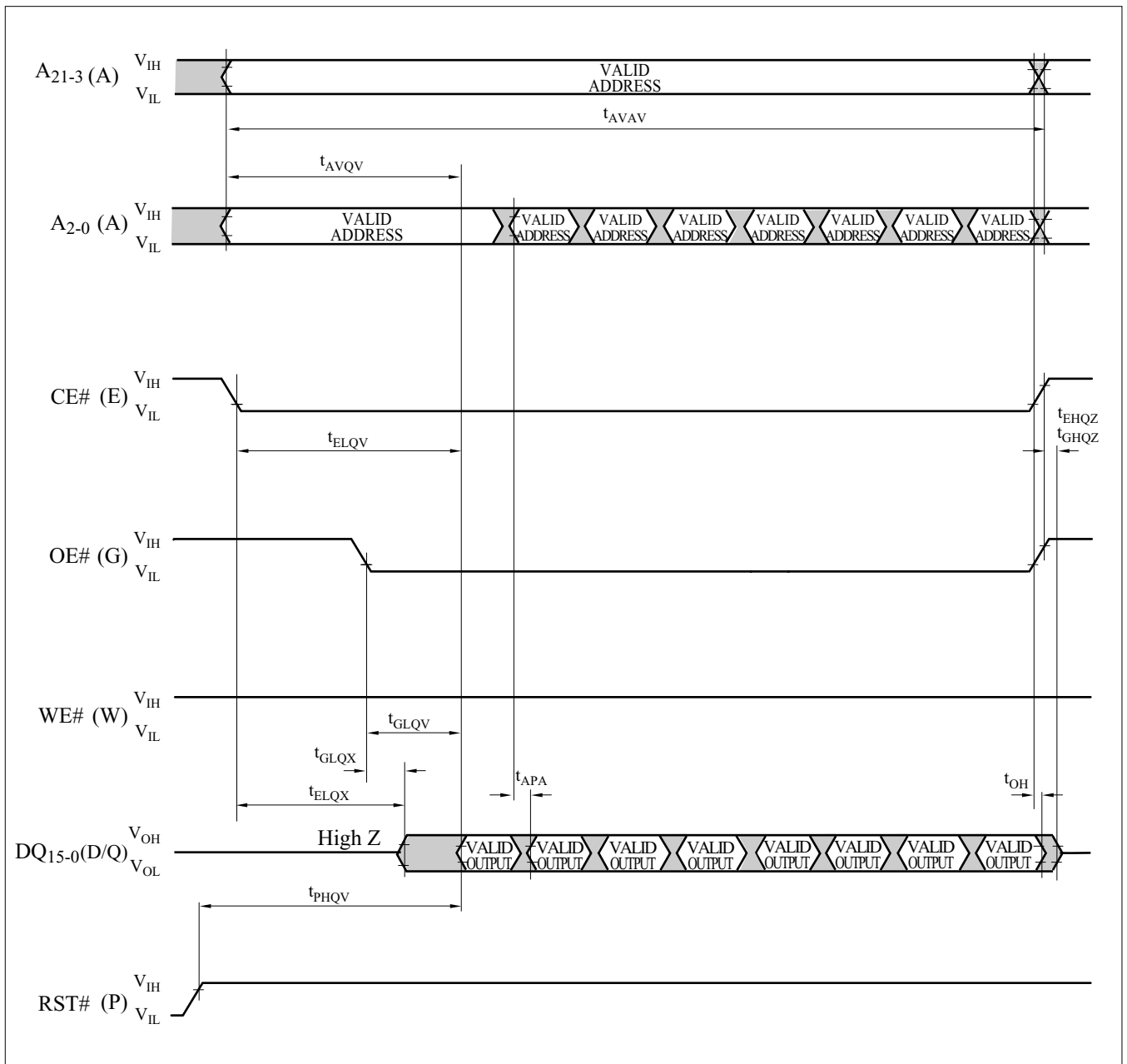Read Operations from Main Blocks or Parameter Blocks

Figure 9.  AC Waveform for Asynchronous 8-Word Page Mode
Read Operations from Main Blocks or Parameter Blocks

## 1.2.5  AC Characteristics - Write Operations[(1), (2)]

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C

| Symbol | Parameter | | Notes | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{AVAV}$ | Write Cycle Time | | | 60 | | ns |
| | | | | 65 | | ns |
| | | | | 70 | | ns |
| $t_{PHWL}$ ($t_{PHEL}$) | RST# High Recovery to WE# (CE#) Going Low | | 3 | 150 | | ns |
| $t_{ELWL}$ ($t_{WLEL}$) | CE# (WE#) Setup to WE# (CE#) Going Low | | | 0 | | ns |
| $t_{WLWH}$ ($t_{ELEH}$) | WE# (CE#) Pulse Width | $t_{AVAV}$=60ns | 4, 9 | 45 | | ns |
| | | $t_{AVAV}$=65ns | | 50 | | ns |
| | | $t_{AVAV}$=70ns | | 55 | | ns |
| $t_{DVWH}$ ($t_{DVEH}$) | Data Setup to WE# (CE#) Going High | | 8 | 40 | | ns |
| $t_{AVWH}$ ($t_{AVEH}$) | Address Setup to WE# (CE#) Going High | $t_{AVAV}$=60ns | 8, 9 | 45 | | ns |
| | | $t_{AVAV}$=65ns | | 50 | | ns |
| | | $t_{AVAV}$=70ns | | 55 | | ns |
| $t_{WHEH}$ ($t_{EHWH}$) | CE# (WE#) Hold from WE# (CE#) High | | | 0 | | ns |
| $t_{WHDX}$ ($t_{EHDX}$) | Data Hold from WE# (CE#) High | | | 0 | | ns |
| $t_{WHAX}$ ($t_{EHAX}$) | Address Hold from WE# (CE#) High | | | 0 | | ns |
| $t_{WHWL}$ ($t_{EHEL}$) | WE# (CE#) Pulse Width High | | 5 | 15 | | ns |
| $t_{SHWH}$ ($t_{SHEH}$) | WP# High Setup to WE# (CE#) Going High | | 3 | 0 | | ns |
| $t_{VVWH}$ ($t_{VVEH}$) | $V_{PP}$ Setup to WE# (CE#) Going High | | 3 | 200 | | ns |
| $t_{WHGL}$ ($t_{EHGL}$) | Write Recovery before Read | | | 30 | | ns |
| $t_{QVSL}$ | WP# High Hold from Valid SRD | | 3, 6 | 0 | | ns |
| $t_{QVVL}$ | $V_{PP}$ Hold from Valid SRD | | 3, 6 | 0 | | ns |
| $t_{WHR0}$ ($t_{EHR0}$) | WE# (CE#) High to SR.7 Going "0" | | 3, 7 | | $t_{AVQV}$+ 50 | ns |

NOTES:
1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. Refer to AC Characteristics for read-only operations.
2. A write operation can be initiated and terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width ($t_{WP}$) is defined from the falling edge of CE# or WE# (whichever goes low last) to the rising edge of CE# or WE# (whichever goes high first). Hence, $t_{WP}$=$t_{WLWH}$=$t_{ELEH}$=$t_{WLEH}$=$t_{ELWH}$.
5. Write pulse width high ($t_{WPH}$) is defined from the rising edge of CE# or WE# (whichever goes high first) to the falling edge of CE# or WE# (whichever goes low last). Hence, $t_{WPH}$=$t_{WHWL}$=$t_{EHEL}$=$t_{WHEL}$=$t_{EHWL}$.
6. $V_{PP}$ should be held at $V_{PP}$=$V_{PPH1/2}$ until determination of block erase, full chip erase, (page buffer) program or OTP program success (SR.1/3/4/5=0).
7. $t_{WHR0}$ ($t_{EHR0}$) after the Read Query or Read Identifier Codes/OTP command=$t_{AVQV}$+100ns.
8. Refer to Table 6 for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.
9. $t_{WLWH}$ ($t_{ELEH}$) and $t_{AVWH}$ ($t_{AVEH}$) values vary depending on the write cycle time ($t_{AVAV}$).
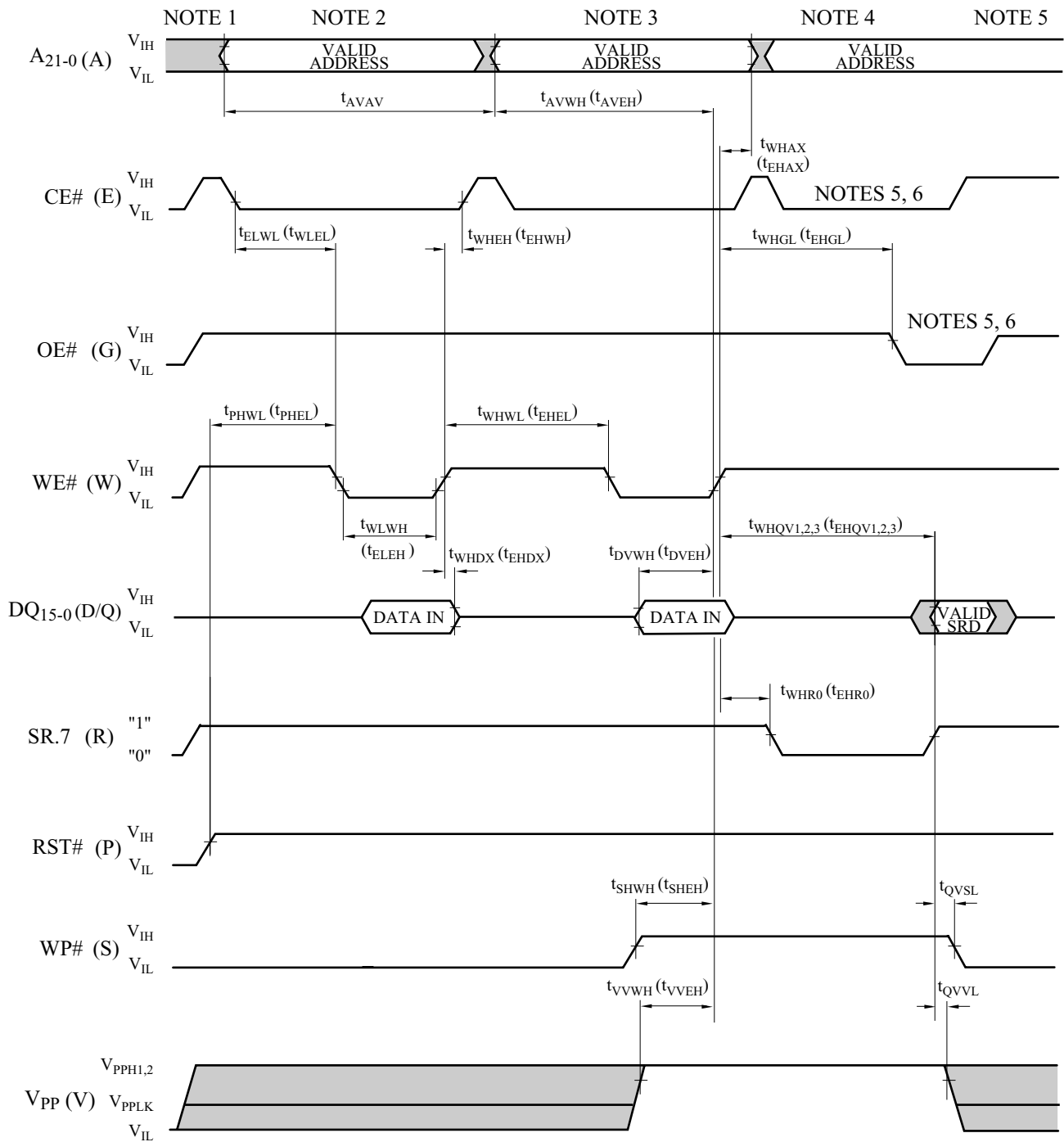
NOTES:
1. $V_{CC}$ power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, OE# and CE# must be driven active, and WE# de-asserted.

Figure 10.  AC Waveform for Write Operations
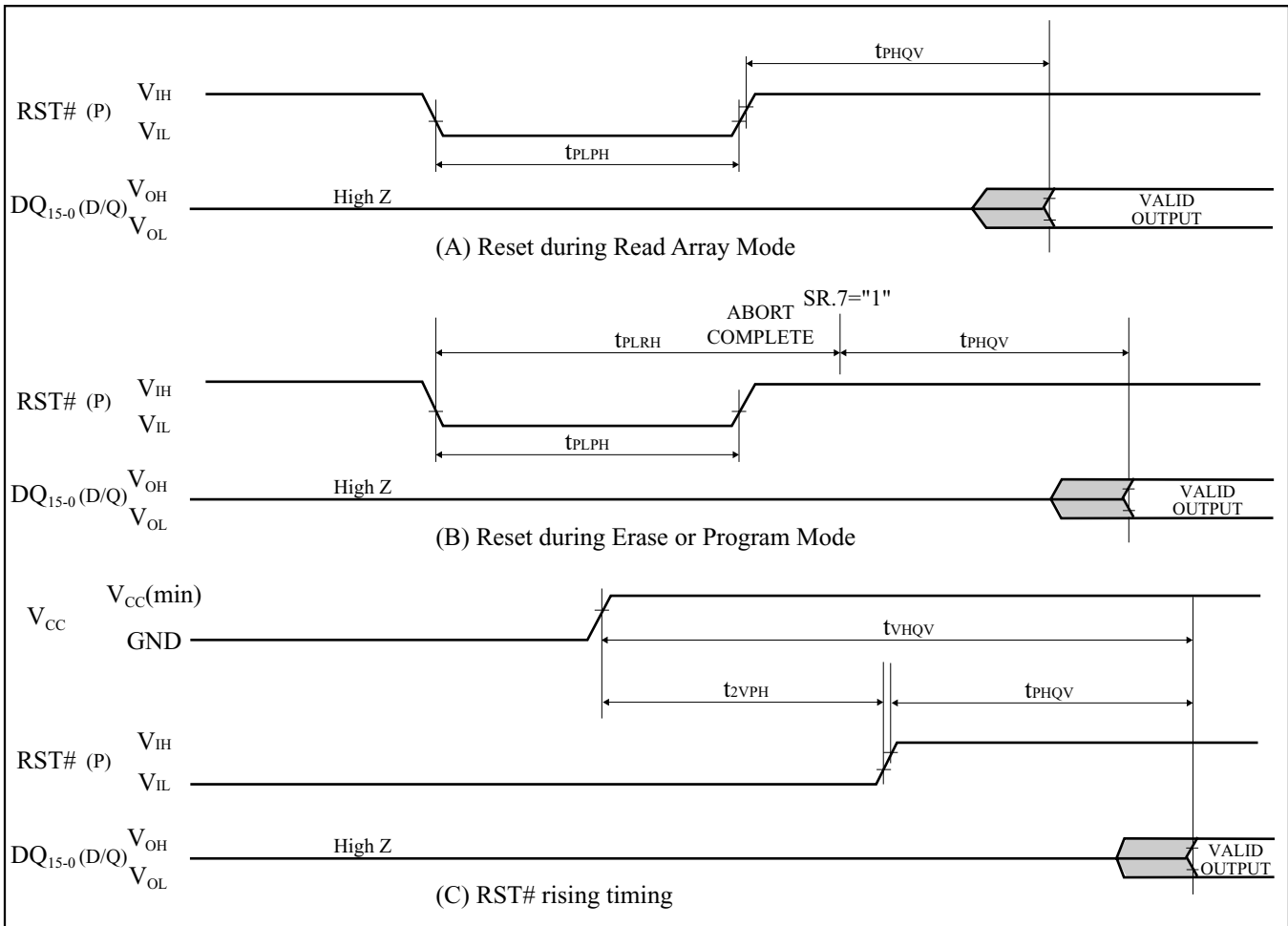
## 1.2.6  Reset Operations



Figure 11.  AC Waveform for Reset Operations

Reset AC Specifications ($V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C)

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|--------|-----------|-------|------|------|------|
| $t_{PLPH}$ | RST# Low to Reset during Read (RST# should be low during power-up.) | 1, 2, 3 | 100 | | ns |
| $t_{PLRH}$ | RST# Low to Reset during Erase or Program | 1, 3, 4 | | 22 | µs |
| $t_{2VPH}$ | $V_{CC}$ 2.7V to RST# High | 1, 3, 5 | 100 | | ns |
| $t_{VHQV}$ | $V_{CC}$ 2.7V to Output Delay | 3 | | 1 | ms |

NOTES:
1. A reset time, $t_{PHQV}$, is required from the later of SR.7 going "1" or RST# going high until outputs are valid. Refer to AC Characteristics - Read-Only Operations for $t_{PHQV}$.
2. $t_{PLPH}$ is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If RST# asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding RST# low minimum 100ns is required after $V_{CC}$ has been in predefined range and also has been in stable there.

### 1.2.7 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance[3]

$V_{CC}$=2.7V-3.6V, $T_A$=-40°C to +85°C

| Symbol | Parameter | Notes | Page Buffer Command is Used or not Used | $V_{PP}=V_{PPH1}$ (In System) | | | $V_{PP}=V_{PPH2}$ (In Manufacturing) | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ.[1] | Max.[2] | Min. | Typ.[1] | Max.[2] | |
| $t_{WPB}$ | 4K-Word Parameter Block Program Time | 2 | Not Used | | 0.05 | 0.3 | | 0.04 | 0.12 | s |
| | | 2 | Used | | 0.03 | 0.12 | | 0.02 | 0.06 | s |
| $t_{WMB}$ | 32K-Word Main Block Program Time | 2 | Not Used | | 0.38 | 2.4 | | 0.31 | 1.0 | s |
| | | 2 | Used | | 0.24 | 1.0 | | 0.17 | 0.5 | s |
| $t_{WHQV1}/$ $t_{EHQV1}$ | Word Program Time | 2 | Not Used | | 11 | 200 | | 9 | 185 | µs |
| | | 2 | Used | | 7 | 100 | | 5 | 90 | µs |
| $t_{WHOV1}/$ $t_{EHOV1}$ | OTP Program Time | 2 | Not Used | | 36 | 400 | | 27 | 185 | µs |
| $t_{WHQV2}/$ $t_{EHQV2}$ | 4K-Word Parameter Block Erase Time | 2 | - | | 0.3 | 4 | | 0.2 | 4 | s |
| $t_{WHQV3}/$ $t_{EHQV3}$ | 32K-Word Main Block Erase Time | 2 | - | | 0.6 | 5 | | 0.5 | 5 | s |
| | Full Chip Erase Time | 2 | | | 80 | 700 | | 65 | 700 | s |
| $t_{WHRH1}/$ $t_{EHRH1}$ | (Page Buffer) Program Suspend Latency Time to Read | 4 | - | | 5 | 10 | | 5 | 10 | µs |
| $t_{WHRH2}/$ $t_{EHRH2}$ | Block Erase Suspend Latency Time to Read | 4 | - | | 5 | 20 | | 5 | 20 | µs |
| $t_{ERES}$ | Latency Time from Block Erase Resume Command to Block Erase Suspend Command | 5 | - | 500 | | | 500 | | | µs |

NOTES:
1. Typical values measured at $V_{CC}$=3.0V, $V_{PP}$=3.0V or 12V, and $T_A$=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (WE# or CE# going high) until SR.7 going "1".
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than $t_{ERES}$ and its sequence is repeated, the block erase operation may not be finished.

## 2 Related Document Information[1]

| Document No. | Document Name |
|---|---|
| FUM00701 | LH28F640BF series Appendix |

NOTE:

1. International customers should contact their local SHARP or distribution sales offices.

## LH28F640BFXX-XXXXXX Flash MEMORY ERRATA

### 1.  AC Characteristics

### <u>PROBLEM</u>

The table below summarizes the AC characteristics.

AC Characteristics - Write Operations

$V_{CC}$=2.7V-3.6V

| Page | Symbol | Parameter | | Min. | Max. | Unit |
|------|--------|-----------|------|------|------|------|
| 26 | $t_{AVAV}$ | Write Cycle Time | | 75 | | ns |
| | | | | 75 | | ns |
| | | | | 75 | | ns |
| 26 | $t_{WLWH}$ ($t_{ELEH}$) | WE# (CE#) Pulse Width | $t_{AVAV}$=75ns | 50 | | ns |
| | | | $t_{AVAV}$=75ns | 50 | | ns |
| | | | $t_{AVAV}$=75ns | 50 | | ns |
| 26 | $t_{WHWL}$ ($t_{EHEL}$) | WE# (CE#) Pulse Width High | | 25 | | ns |

### <u>WORKAROUND</u>

System designers should consider these specifications.

### <u>STATUS</u>

This is intended to be fixed in future devices.

## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.
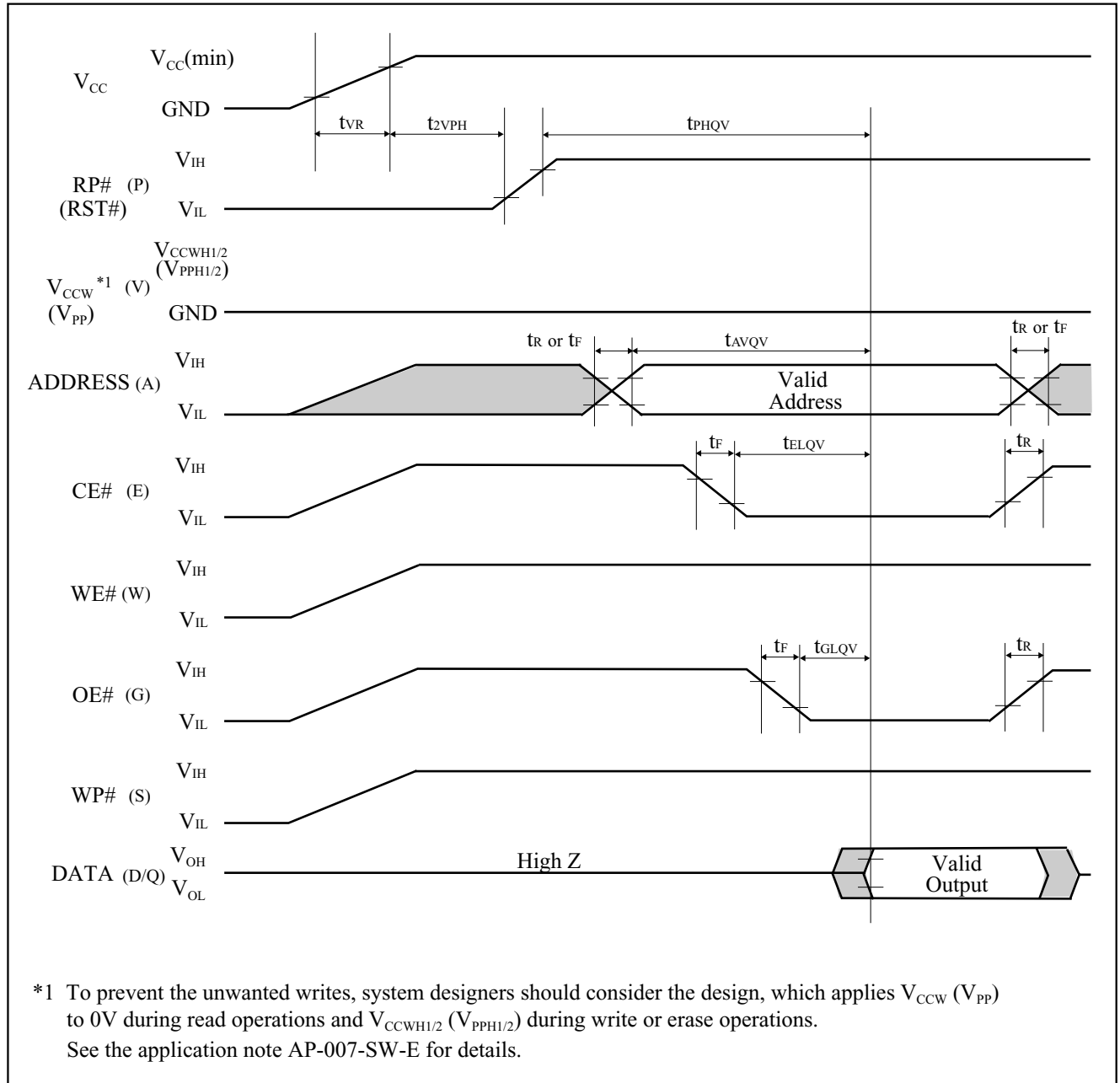


*1 To prevent the unwanted writes, system designers should consider the design, which applies $V_{CCW}$ ($V_{PP}$) to 0V during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations. See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications $t_{VR}$, $t_R$, $t_F$ in the figure, refer to the next page. See the "ELECTRICAL SPECIFICATIONS" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1   Rise and Fall Time

| Symbol | Parameter | Notes | Min. | Max. | Unit |
|--------|-----------|-------|------|------|------|
| $t_{VR}$ | $V_{CC}$ Rise Time | 1 | 0.5 | 30000 | µs/V |
| $t_R$ | Input Signal Rise Time | 1, 2 | | 1 | µs/V |
| $t_F$ | Input Signal Fall Time | 1, 2 | | 1 | µs/V |

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

## A-1.2  Glitch Noises

Do not input the glitch noises which are below $V_{IH}$ (Min.) or above $V_{IL}$ (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).
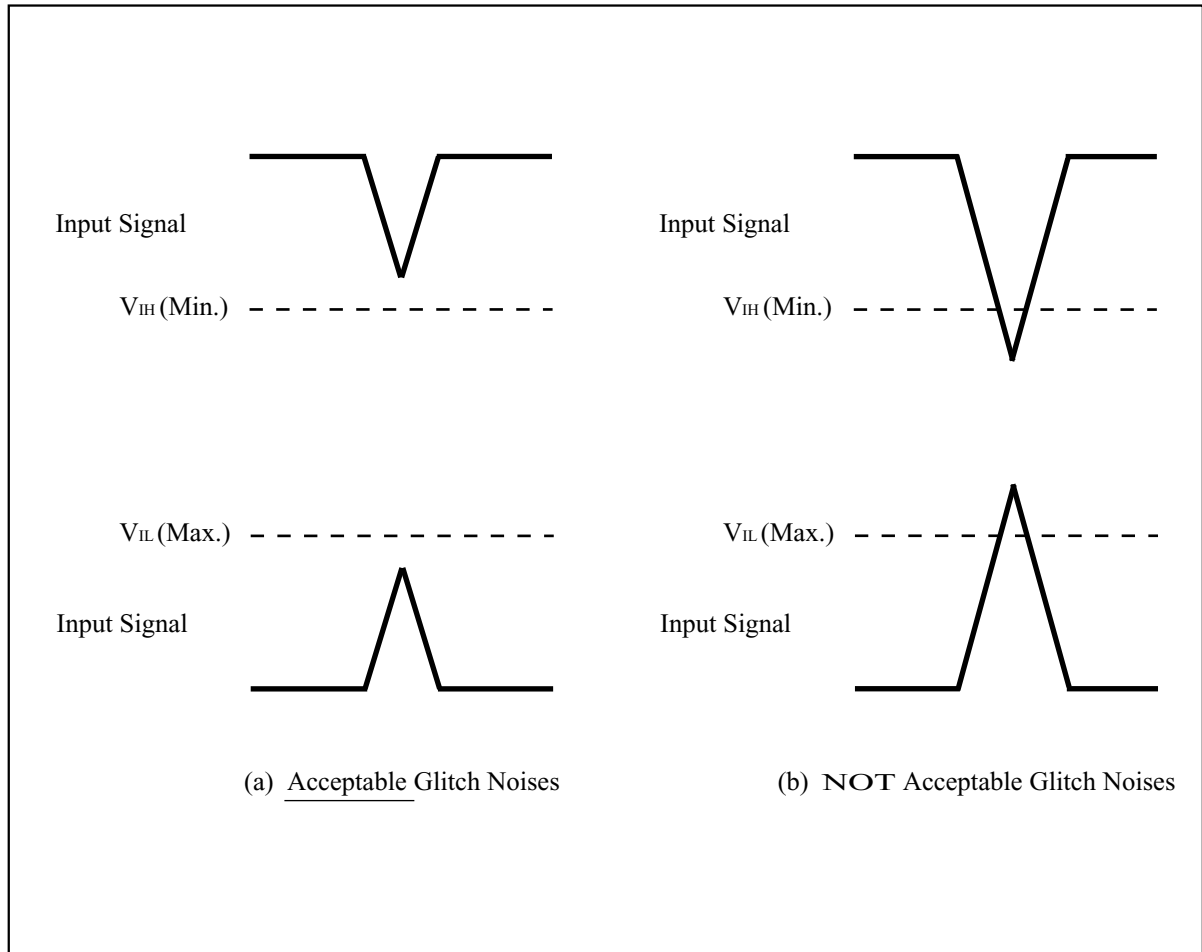
Input Signal

$V_{IH}$ (Min.)

Input Signal

$V_{IH}$ (Min.)

$V_{IL}$ (Max.)

Input Signal

$V_{IL}$ (Max.)

Input Signal

(a)  Acceptable Glitch Noises

(b)  NOT Acceptable Glitch Noises

Figure A-2.  Waveform for Glitch Noises

See the "DC CHARACTERISTICS" described in specifications for $V_{IH}$ (Min.) and $V_{IL}$ (Max.).

## A-2 RELATED DOCUMENT INFORMATION[1]

| Document No. | Document Name |
|---|---|
| AP-001-SD-E | Flash Memory Family Software Drivers |
| AP-006-PT-E | Data Protection Method of SHARP Flash Memory |
| AP-007-SW-E | RP#, $V_{PP}$ Electric Potential Switching Circuit |

NOTE:

1. International customers should contact their local SHARP or distribution sales office.

## A-3  STATUS REGISTER READ OPERATIONS

If AC timing for reading the status register described in specifications is not satisfied, a system processor can check the status register bit SR.15 instead of SR.7 to determine when the erase or program operation has been completed.

Table A-3-1.  Status Register Definition (SR.15 and SR.7)

| | NOTES: |
|---|---|
| SR.15 = WRITE STATE MACHINE STATUS: $(DQ_{15})$<br>  1 = Ready in All Partitions<br>  0 = Busy in Any Partition<br><br>SR.7 = WRITE STATE MACHINE STATUS<br>    FOR EACH PARTITION: $(DQ_7)$<br>  1 = Ready in the Addressed Partition<br>  0 = Busy in the Addressed Partition | SR.15 indicates the status of WSM (Write State Machine). If SR.15="0", erase or program operation is in progress in any partition.<br><br>SR.7 indicates the status of the partition. If SR.7="0", erase or program operation is in progress in the addressed partition. Even if the SR.7 is "1", the WSM may be occupied by the other partition. |
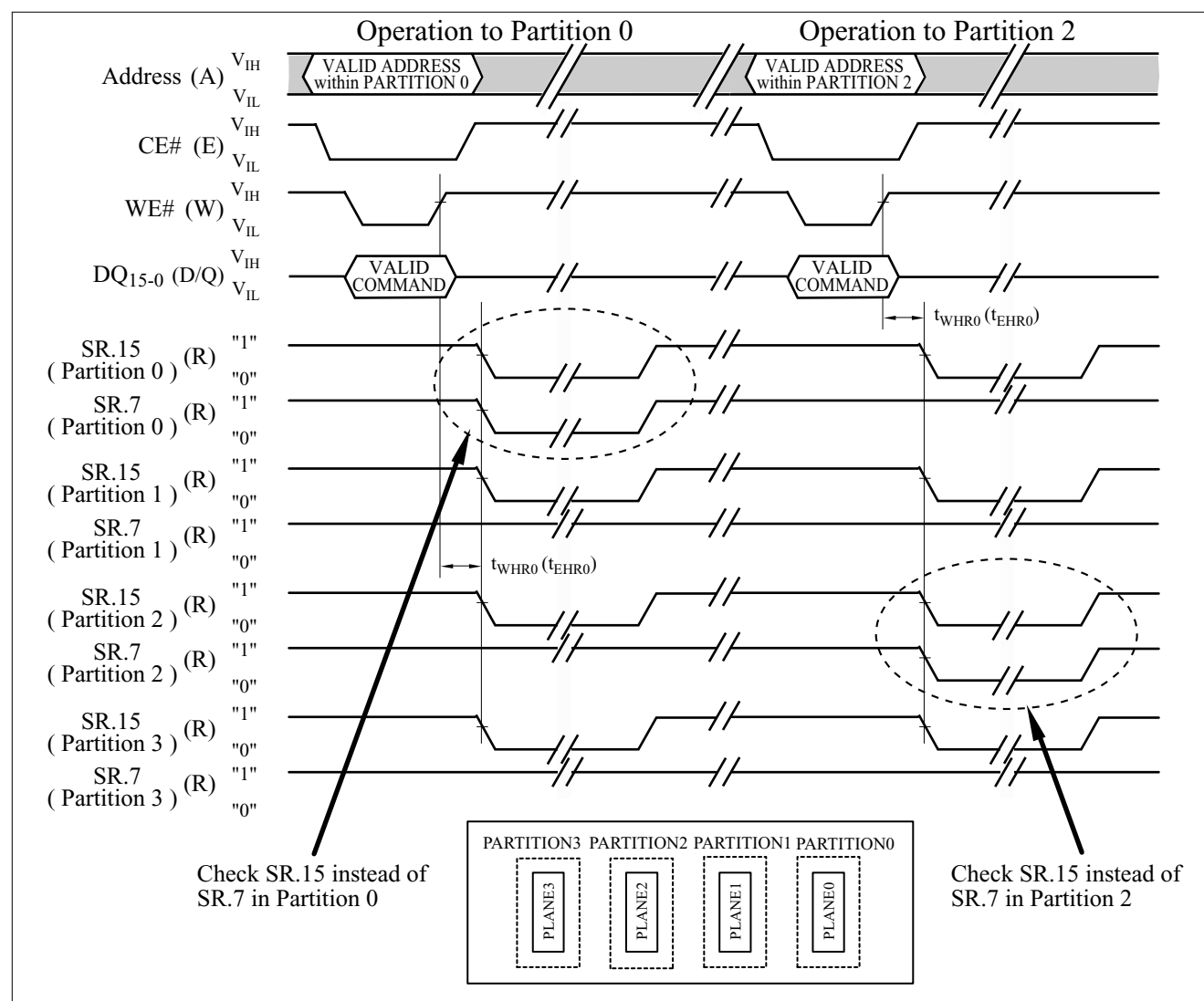


Figure A-3-1.  Example of Checking the Status Register
(In this example, the device contains four partitions.)

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