MC74AC109, MC74ACT109

Dual $\overline{JK}$ Positive Edge-Triggered Flip-Flop

The MC74AC109/74ACT109 consists of two high–speed completely independent transition clocked $\overline{JK}$ flip–flops. The clocking operation is independent of rise and fall times of the clock waveform. The $\overline{JK}$ design allows operation as a D flip–flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:

LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

- Outputs Source/Sink 24 mA
- ′ACT109 Has TTL Compatible Inputs

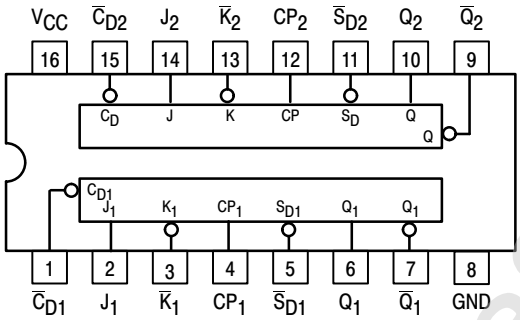

Figure 1. Pinout; 16–Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

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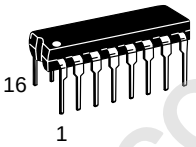
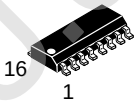
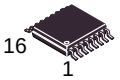


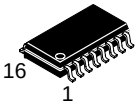
DIP–16
N SUFFIX
CASE 648



SO–16
D SUFFIX
CASE 751B



TSSOP–16
DT SUFFIX
CASE 948F



EIAJ–16
M SUFFIX
CASE 966

ORDERING INFORMATION

Device	Package	Shipping
MC74AC109N	PDIP–16	25 Units/Rail
MC74ACT109N	PDIP–16	25 Units/Rail
MC74AC109D	SOIC–16	48 Units/Rail
MC74ACT109D	SOIC–16	48 Units/Rail
MC74AC109DR2	SOIC–16	2500 Tape & Reel
MC74ACT109DR2	SOIC–16	2500 Tape & Reel
MC74AC109DT	TSSOP–16	96 Units/Rail
MC74ACT109DT	TSSOP–16	96 Units/Rail
MC74AC109DTR2	TSSOP–16	2500 Tape & Reel
MC74ACT109DTR2	TSSOP–16	2500 Tape & Reel
MC74AC109M	EIAJ–16	50 Units/Rail
MC74ACT109M	EIAJ–16	50 Units/Rail
MC74AC109MEL	EIAJ–16	2000 Tape & Reel
MC74ACT109MEL	EIAJ–16	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 111 of this data sheet.

TRUTH TABLE

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐⌐	L	L	L	H
H	H	⌐⌐	H	L	Toggle	
H	H	⌐⌐	L	H	Q_0	$\overline{Q}_0$
H	H	⌐⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
⌐⌐ = LOW–to–HIGH Clock Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW–to–HIGH Transition of Clock

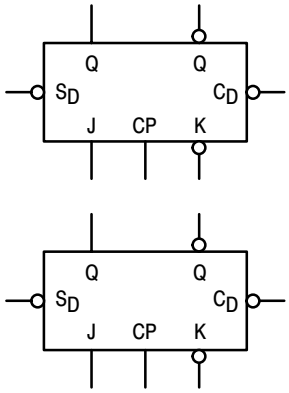
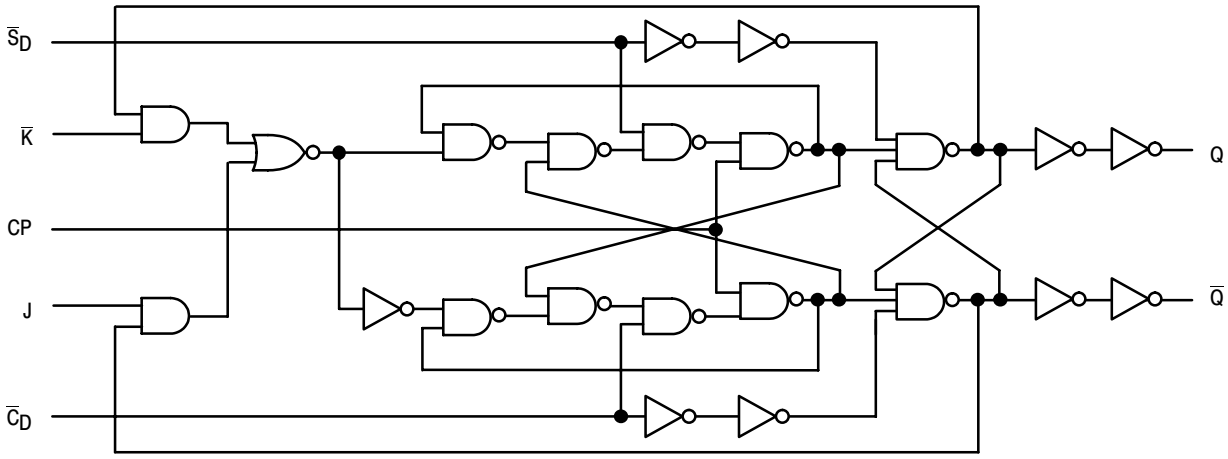


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram
(One Half Shown)

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	–0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	–	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	–	150	–	ns/V
		V_{CC} @ 4.5 V	–	40	–	
		V_{CC} @ 5.5 V	–	25	–	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	–	10	–	ns/V
		V_{CC} @ 5.5 V	–	8.0	–	
T_J	Junction Temperature (PDIP)		–	–	140	°C
T_A	Operating Ambient Temperature Range		–40	25	85	°C
I_{OH}	Output Current – High		–	–	–24	mA
I_{OL}	Output Current – Low		–	–	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C		74AC T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = –50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0	–	2.56	2.46	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} –12 mA
		4.5	–	3.86	3.76		I_{OH} –24 mA
		5.5	–	4.86	4.76		I_{OH} –24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0	–	0.36	0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5	–	0.36	0.44		I_{OL} 24 mA
		5.5	–	0.36	0.44		I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = –40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150	– –	– –	100 125	– –	MHz	3–3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	4.0 2.5	– –	13.5 10.0	3.5 2.0	16.0 10.5	ns	3–6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	14.0 10.0	3.0 1.5	14.5 10.5	ns	3–6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.5	– –	12.0 9.0	2.5 2.0	13.0 10.0	ns	3–6
t_{PHL}	Propagation Delay $\overline{CD}_n$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	3.0 2.0	– –	12.0 9.5	3.0 2.0	13.5 10.5	ns	3–6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = –40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set–up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	– –	6.5 4.5	7.5 5.0	ns	3–9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	– –	0 0.5	0 0.5	ns	3–9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	– –	4.0 3.5	4.5 3.5	ns	3–6
t_{rec}	Recovery TIme $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	– –	0 0	0 0	ns	3–9

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C	74ACT T_A = –40°C to +85°C		Unit	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} – 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = –50 μA
		4.5 5.5	– –	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} –24 mA I_{OH} –24 mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

DC CHARACTERISTICS (continued)

Symbol	Parameter	V_{CC} (V)	74ACT T_A = +25°C		74ACT T_A = –40°C to +85°C	Unit	Conditions
			Typ	Guaranteed Limits			
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	– –	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	–	1.5	mA	V_I = V_{CC} – 2.1 V
I_{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	–	–	–75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	–	4.0	40	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = –40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	–	–	125	–	MHz	3–3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	4.0	–	11.0	3.5	13.0	ns	3–6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	3.0	–	10.0	2.5	11.5	ns	3–6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	–	9.5	2.0	10.5	ns	3–6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	2.5	–	10.0	2.0	11.5	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = –40°C to +85°C, C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set–up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	–	2.0	2.5	ns	3–9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	–	2.0	2.0	ns	3–9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	–	5.0	6.0	ns	3–6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS (continued)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_{rec}	Recovery TIme $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	–	0	0	ns	3–9

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

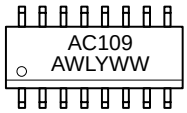
CAPACITANCE

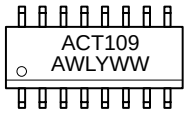
Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0 V

MARKING DIAGRAMS

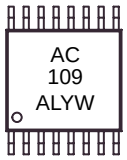
DIP–16

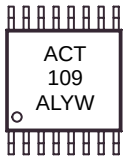
SO–16



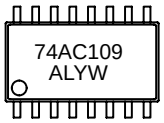


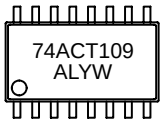
TSSOP–16





EIAJ–16





A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week