

## DUAL RETRIGGERABLE PRECISION MONOSTABLE MULTIVIBRATOR

### FEATURES

- Separate reset inputs
- Triggering from leading or trailing edge
- Output capability: standard
- I<sub>CC</sub> category: MSI
- Power-on reset on-chip

### GENERAL DESCRIPTION

The 74HC/HCT4538 are high-speed Si-gate CMOS devices and are pin compatible with "4538" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4538 are dual retriggerable-resettable monostable multivibrators. Each multivibrator has an active LOW trigger/retrigger input ( $\overline{nA_0}$ ), an active HIGH trigger/retrigger input ( $nA_1$ ), an overriding active LOW direct reset input ( $\overline{nRD}$ ), an output ( $nQ$ ) and its complement ( $\overline{nQ}$ ), and two pins ( $nC_{TC}$  and  $nRC_{TC}$ ) for connecting the external timing components  $C_t$  and  $R_t$ . Typical pulse width variation over temperature range is  $\pm 0.2\%$ .

The "4538" may be triggered by either the positive or the negative edges of the input pulse. The duration and accuracy of the output pulse are determined by the external timing components  $C_t$  and  $R_t$ . The output pulse width (T) is equal to  $0.7 \times R_t \times C_t$ . The linear design techniques guarantee precise control of the output pulse width.

A LOW level at  $\overline{nRD}$  terminates the output pulse immediately.

Schmitt-trigger action in the trigger inputs makes the circuit highly tolerant to slower rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{nA_0}, nA_1$ to $nQ, \overline{nQ}$	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	27	30	ns
$C_i$	input capacitance		3.5	3.5	pF
$C_{pD}$	power dissipation capacitance per multivibrator	notes 1 and 2	136	138	pF

$GND = 0 \text{ V}; T_{amb} = 25^\circ\text{C}; t_r = t_f = 6 \text{ ns}$

### Notes

1.  $C_{pD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{pD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + 0.48 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 0.8 \times V_{CC} \text{ where:}$$

$f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V  
 $D$  = duty factor in %  
 $C_{EXT}$  = timing capacitance in pF

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$   
 For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

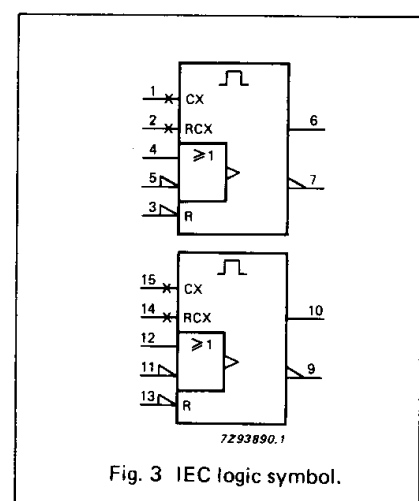
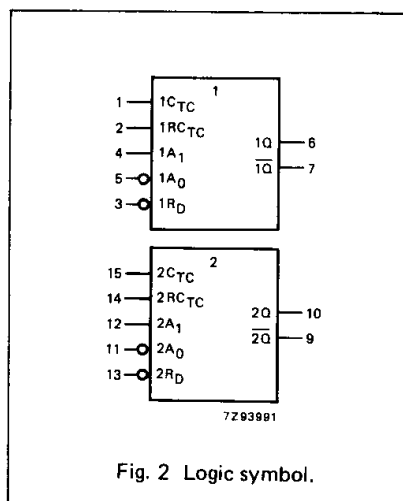
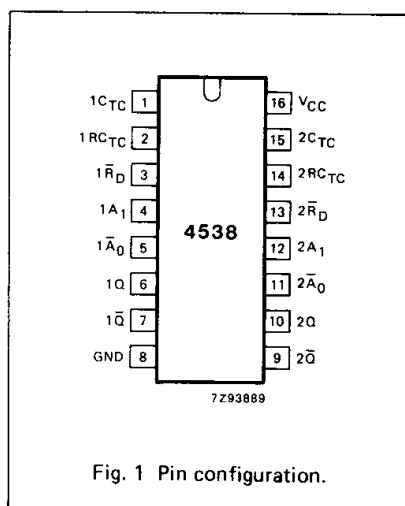
### PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

### PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1C_{TC}, 2C_{TC}$	external capacitor connections
2, 14	$1RC_{TC}, 2RC_{TC}$	external resistor/capacitor connections
3, 13	$1\overline{RD}, 2\overline{RD}$	direct reset inputs (active LOW)
4, 12	$1A_1, 2A_1$	trigger inputs (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{A_0}, 2\overline{A_0}$	trigger inputs (HIGH-to-LOW, edge-triggered)
6, 10	$1Q, 2Q$	pulse outputs
7, 9	$1\overline{Q}, 2\overline{Q}$	complementary pulse outputs
8	GND	ground (0 V)
16	$V_{CC}$	positive supply voltage



FUNCTION TABLE

INPUTS			OUTPUTS	
$n\bar{A}_0$	$nA_1$	$n\bar{R}_D$	$nQ$	$n\bar{Q}$
↓	L	H		
H	↑	H		
X	X	L	L	H

H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↑ = LOW-to-HIGH transition  
↓ = HIGH-to-LOW transition  
 = one HIGH level output pulse  
 = one LOW level output pulse

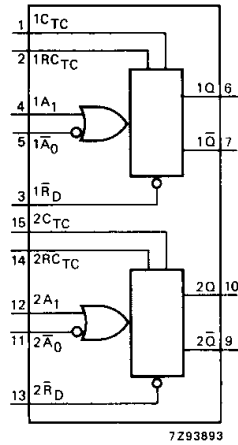
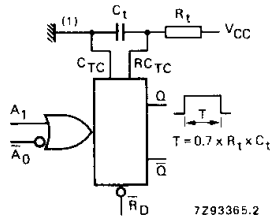
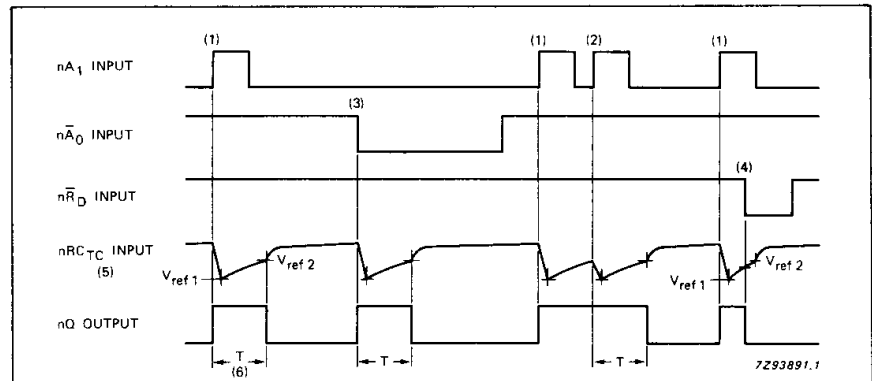


Fig. 4 Functional diagram.



(1) Connect  $C_{TC}$  (pins 1 and 15) to GND (pin 8).

Fig. 5 Connection of the external timing components  $R_T$  and  $C_T$ .



- (1) Positive edge triggering.
- (2) Positive edge retriggering (pulse lengthening).
- (3) Negative edge triggering.
- (4) Reset (pulse shortening).
- (5)  $V_{ref1}$  and  $V_{ref2}$  are internal reference voltages.
- (6)  $T = 0.7 \times R_T \times C_T$  (see also Fig. 5).

Fig. 6 Timing diagram.

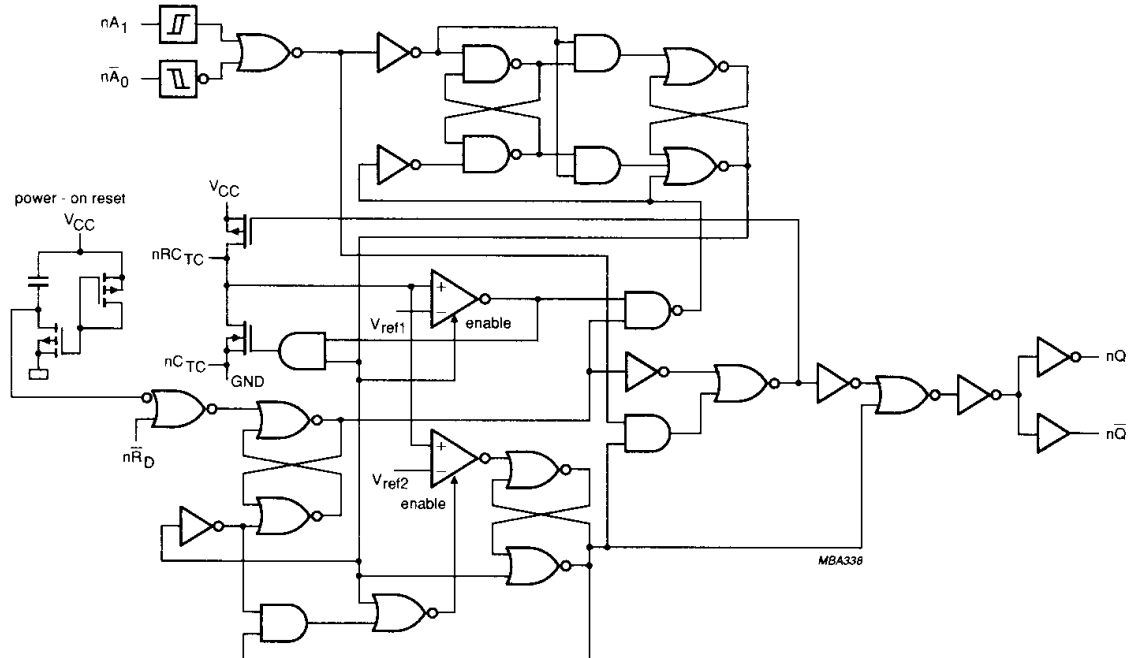


Fig. 7 Logic diagram ( $V_{ref1}$  and  $V_{ref2}$  are internal reference voltages).

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								UNIT	TEST CONDITIONS	
		74HC									V <sub>CC</sub> V	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PLH</sub>	propagation delay nA <sub>0</sub> , nA <sub>1</sub> to nQ		85 31 25	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8	
t <sub>PHL</sub>	propagation delay nA <sub>0</sub> , nA <sub>1</sub> to nQ		83 30 24	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8	
t <sub>PHL</sub>	propagation delay nR <sub>D</sub> to nQ		80 29 23	265 53 45		330 66 56		400 80 68	ns	2.0 4.5 6.0	Fig. 8	
t <sub>PLH</sub>	propagation delay nR <sub>D</sub> to nQ		83 30 24	265 53 45		340 68 58		400 80 68	ns	2.0 4.5 6.0	Fig. 8	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 8	
t <sub>w</sub>	nA <sub>0</sub> pulse width LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t <sub>w</sub>	nA <sub>1</sub> pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t <sub>w</sub>	nR <sub>D</sub> pulse width LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8	
t <sub>w</sub>	nQ, nQ pulse width HIGH or LOW	0.63	0.70	0.77	0.60	0.798	0.595	0.805	ms	5.0	Fig. 8; R <sub>T</sub> = 10 kΩ; C <sub>T</sub> = 0.1 μF	
t <sub>rem</sub>	removal time R <sub>D</sub> to nA <sub>0</sub> , nA <sub>1</sub>	35 7 6	6 2 2		45 9 8		55 11 9		ns	2.0 4.5 6.0	Fig. 8	
t <sub>rt</sub>	retrigger time nA <sub>0</sub> , nA <sub>1</sub>	— — —	455+X 80+X 55+X		— — —		— — —		ns	2.0 4.5 6.0	Fig. 8 X = C <sub>EXT</sub> /(4.5 × V <sub>CC</sub> )	
R <sub>EXT</sub>	external timing resistor	10 2		1000 1000					kΩ	2.0 5.0		
C <sub>EXT</sub>	external timing capacitor	no limits							pF	5.0		

**NON-STANDARD DC CHARACTERISTICS FOR 74HC**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> V	V <sub>I</sub> V	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.		max.			
±I <sub>l</sub>	input leakage current nR <sub>CEXT</sub>			0.5		5.0		10.0	μA	6.0	2.0 or GND	V <sub>CC</sub> or GND; note 1

**Note**

1. This measurement can only be carried out after a trigger pulse is applied.

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given in the family specifications. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA <sub>0</sub> , nA <sub>1</sub>	0.50
nR <sub>D</sub>	0.65

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS	
		74HCT									$V_{CC}$ V	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PLH}$	propagation delay $n\bar{A}_0, nA_1$ to $nQ$		35	60		75		90	ns	4.5	Fig. 8	
$t_{PHL}$	propagation delay $n\bar{A}_0, nA_1$ to $n\bar{Q}$		35	60		75		90	ns	4.5	Fig. 8	
$t_{PHL}$	propagation delay $n\bar{R}_D$ to $nQ$		35	60		75		90	ns	4.5	Fig. 8	
$t_{PLH}$	propagation delay $n\bar{R}_D$ to $n\bar{Q}$		35	60		75		90	ns	4.5	Fig. 8	
$t_{HL}/$ $t_{LH}$	output transition time		7	15		19		21	ns	4.5	Fig. 8	
$t_W$	$n\bar{A}_0$ pulse width LOW	20	11		25		30		ns	4.5	Fig. 8	
$t_W$	$nA_1$ pulse width HIGH	16	5		20		24		ns	4.5	Fig. 8	
$t_W$	$n\bar{R}_D$ pulse width LOW	20	11		25		30		ns	4.5	Fig. 8	
$t_W$	$nQ, n\bar{Q}$ pulse width HIGH or LOW	0.63	0.70	0.77	0.602	0.798	0.595	0.805	ms	5.0	Fig. 8; $R_t = 10$ k $\Omega$ ; $C_t = 0.1$ $\mu$ F	
$t_{rem}$	removal time $\bar{R}_D$ to $n\bar{A}_0, nA_1$	7	2		9		11		ns	4.5	Fig. 8	
$t_{rt}$	retrigger time $n\bar{A}_0, nA_1$	-	80+x		-		-		ns	4.5	Fig. 8 $X = C_{EXT}/(4.5 \times V_{CC})$	
$R_{EXT}$	external timing resistor	2		1000					k $\Omega$	5.0		
$C_{EXT}$	external timing capacitor	no limits							pF	5.0		

## NON-STANDARD DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	$T_{amb}$ (°C)								UNIT	TEST CONDITIONS		
		74HCT									$V_{CC}$ V	$V_I$ V	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
$\pm I_I$	input leakage current $nR_{EXT}$			0.5		5.0		10.0	$\mu$ A	5.5	2.0 or GND	$V_{CC}$ or GND; note 1	

## Note

1. This measurement can only be carried out after a trigger pulse is applied.

AC WAVEFORMS

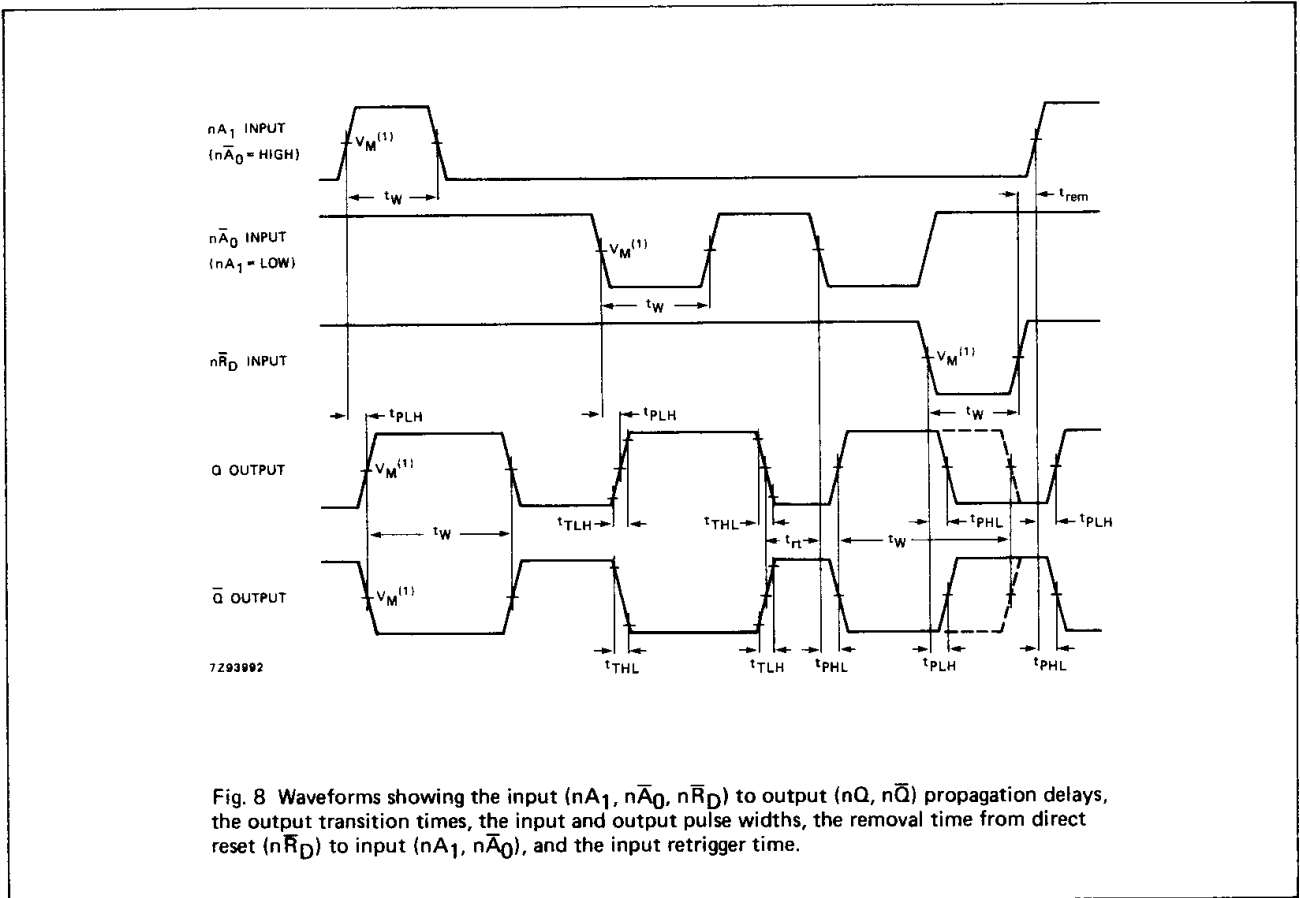


Fig. 8 Waveforms showing the input (nA<sub>1</sub>, nA<sub>0</sub>, nR<sub>D</sub>) to output (nQ, nQ̄) propagation delays, the output transition times, the input and output pulse widths, the removal time from direct reset (nR<sub>D</sub>) to input (nA<sub>1</sub>, nA<sub>0</sub>), and the input retrigger time.

Note to AC waveforms

- (1) HC : V<sub>M</sub> = 50%; V<sub>I</sub> = GND to V<sub>CC</sub>.
- HCT: V<sub>M</sub> = 1.3 V; V<sub>I</sub> = GND to 3 V.

APPLICATION INFORMATION

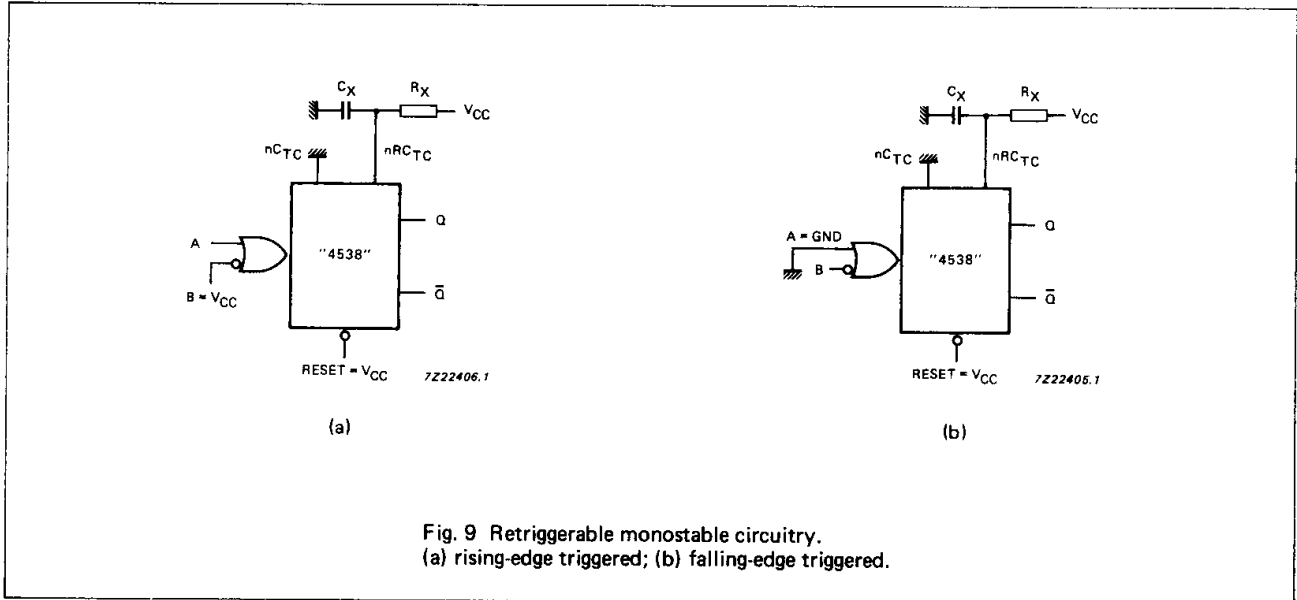


Fig. 9 Retriggerable monostable circuitry.  
(a) rising-edge triggered; (b) falling-edge triggered.

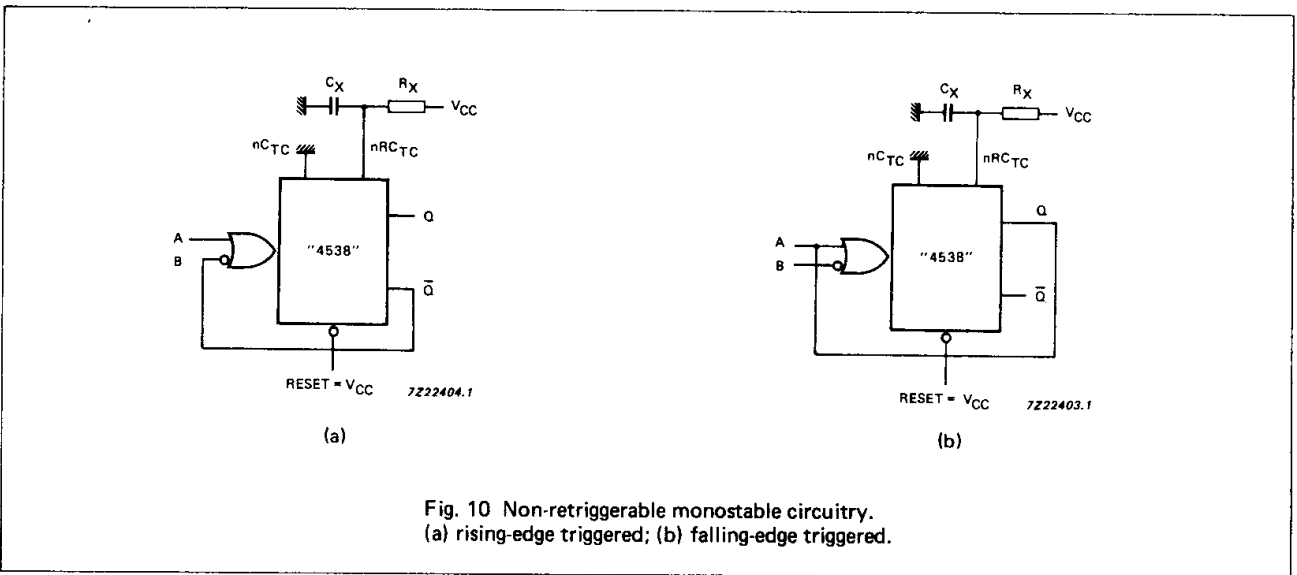


Fig. 10 Non-retriggerable monostable circuitry.  
(a) rising-edge triggered; (b) falling-edge triggered.

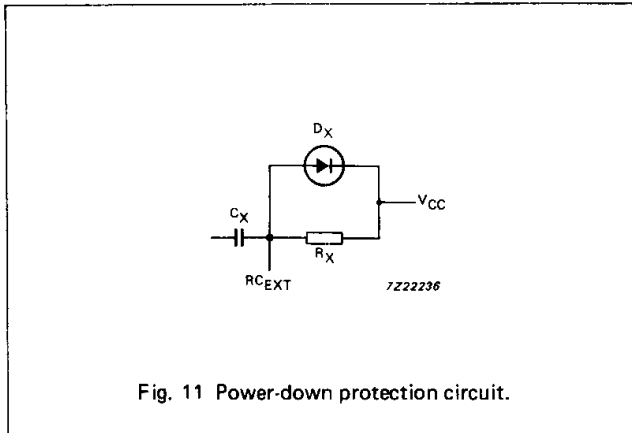


Fig. 11 Power-down protection circuit.

**Power-down considerations**

A large capacitor ( $C_X$ ) may cause problems when powering-down the monostable due to the energy stored in this capacitor. When a system containing this device is powered-down or a rapid decrease of  $V_{CC}$  to zero occurs, the monostable may sustain damage, due to the capacitor discharging through the input protection diodes. To avoid this possibility, use a damping diode ( $D_X$ ) preferably a germanium or Schottky type diode able to withstand large current surges and connect as shown in Fig. 11.

**APPLICATION INFORMATION (Continued)**

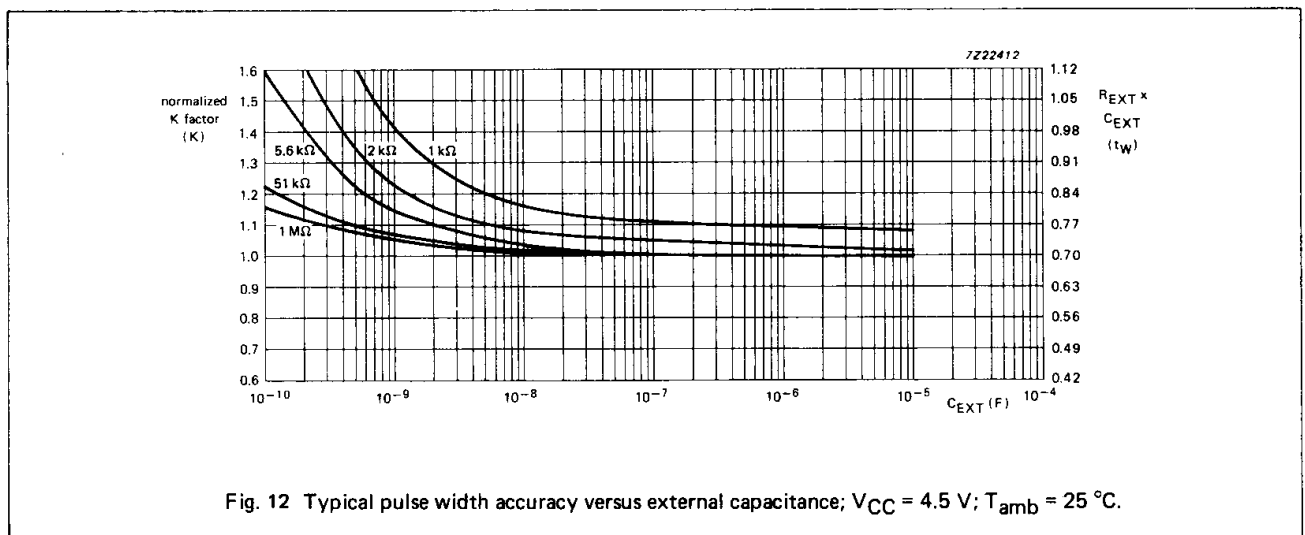


Fig. 12 Typical pulse width accuracy versus external capacitance;  $V_{CC} = 4.5 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

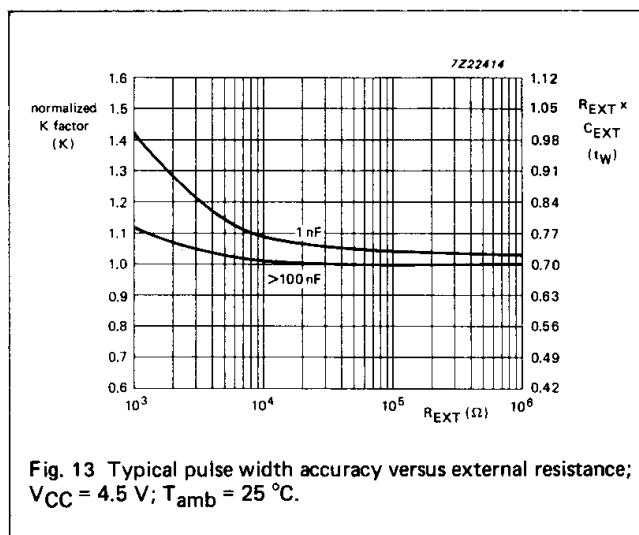


Fig. 13 Typical pulse width accuracy versus external resistance;  $V_{CC} = 4.5 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .



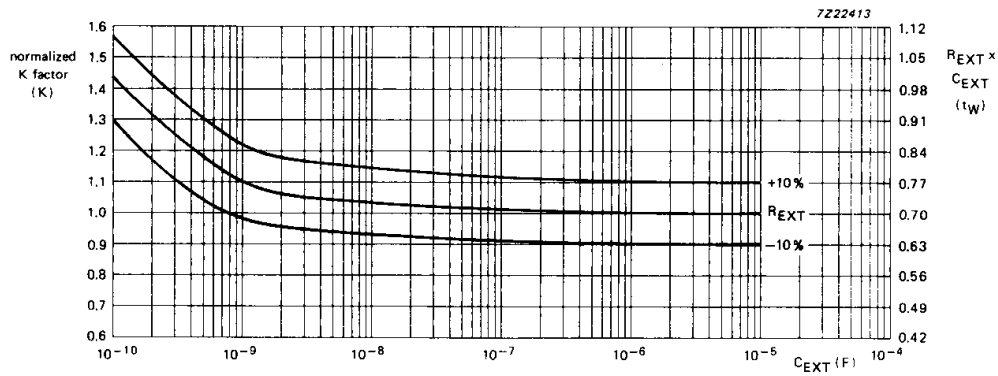


Fig. 14 Typical pulse width accuracy versus external capacitance;  $R_{EXT} = 10 \text{ k}\Omega$ ;  $V_{CC} = 4.5 \text{ V}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

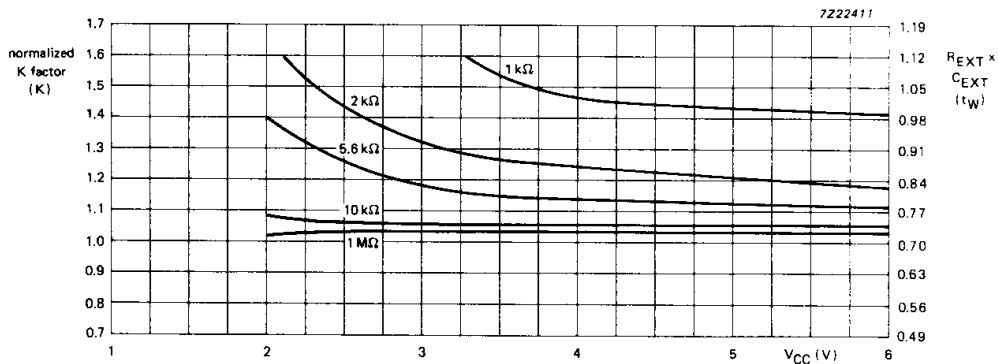


Fig. 15 Typical pulse width accuracy versus power supply;  $C_{EXT} = 1 \text{ nF}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

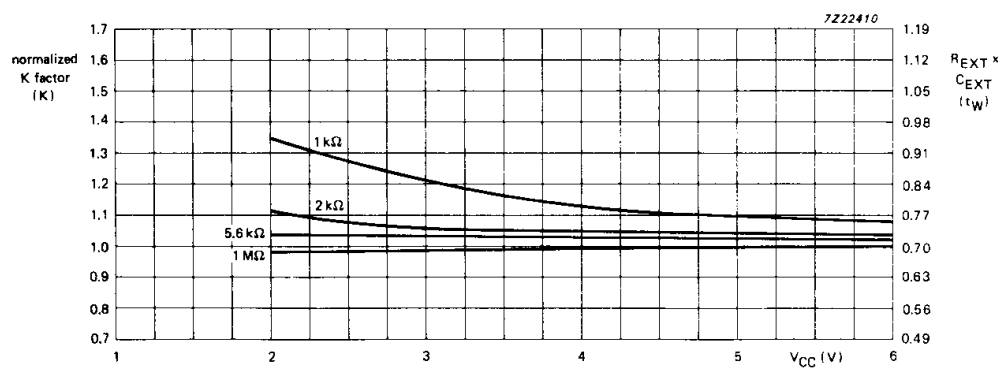


Fig. 16 Typical pulse width accuracy versus power supply;  $C_{EXT} = 100 \text{ nF}$ ;  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

APPLICATION INFORMATION (Continued)

