Advance Data Sheet
July 1995

AT&T Microelectronics

AT&T CSP1088 GSM Conversion Signal Processor for Cellular Handset and Modem Applications v2.2

Features

- Seamless interface to the DSP1618 processor and W2020 RF transceiver
- Complete A/D and D/A functions for voiceband including digital audio interface
- Complete A/D and D/A functions for baseband
- Event timing and control state machine that monitors the internal quarter-bit counter and internal frame counter until a programmed time is reached, and then executes the control portion of the register and may issue an interrupt to the DSP
- GMSK modulator that takes 88 or 148 bits of burst data from an internal register and modulates it to GSM standards. Phase information is converted into I and Q output voltages that can be connected directly to a W2020 transceiver or RF modulator
- Received baseband I and Q signals are A/D converted and stored in a double buffer that holds 16 I and 16 Q samples before issuing an interrupt to the DSP to read the sample information
- 14 output control lines that can be used to control external circuits for such functions as power on/off or digital gain control
- Serial port that can be used to program an external RF frequency synthesizer
- Interrupt handling capabilities for voiceband samples, received baseband data as ciphering, timing and control interrupts, and for end of transmission notification
- Voiceband output connects directly to 15 Ω
- Voiceband input connects directly to electret microphone
- *IEEE** 1149.1 JTAG controller and boundary scan register
- Hardware support for A5.1 and A5.2 ciphering
- Frequency synthesizer compatibility with DSP1618

Description

The AT&T CSP1088 integrates the timing and control functions for GSM mobile application with the A/D and D/A functions. It serves as the interface that connects a DSP to the RF circuitry in a GSM mobile telephone.

For example, a DSP can load 148 bits of burst data into the AT&T CSP1088's internal register, and program the AT&T CSP1088's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal register are GMSK modulated to GSM standards, and the resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator. An end-of-transmit interrupt notifies the DSP when the transmission is complete.

For receiving baseband data, a DSP can program the AT&T CSP1088's event timing and control register with the exact time to start receiving I and Q samples. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 16 sample pairs. The AT&T CSP1088 then issues an interrupt to the DSP which has ample time to read the information out before the next 16 sample pairs are stored.

The voiceband A/D converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voiceband output D/A converter with a new PCM output word. The D/A output can be connected directly to a 15 Ω load or higher.

* *IEEE* is a registered trade mark of The Institute of Electrical and Electronics Engineers, Inc.

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Description (continued)

The AT&T CSP1088 is designed to interface a digital signal processor with analog audio and baseband signals, and programmable events, power timers, and filters. The device provides analog interfacing and timing for a GSM mobile cellular telecommunications terminal requiring low power consumption. Figure 1, is a block diagram of the AT&T CSP1088 v2.2.

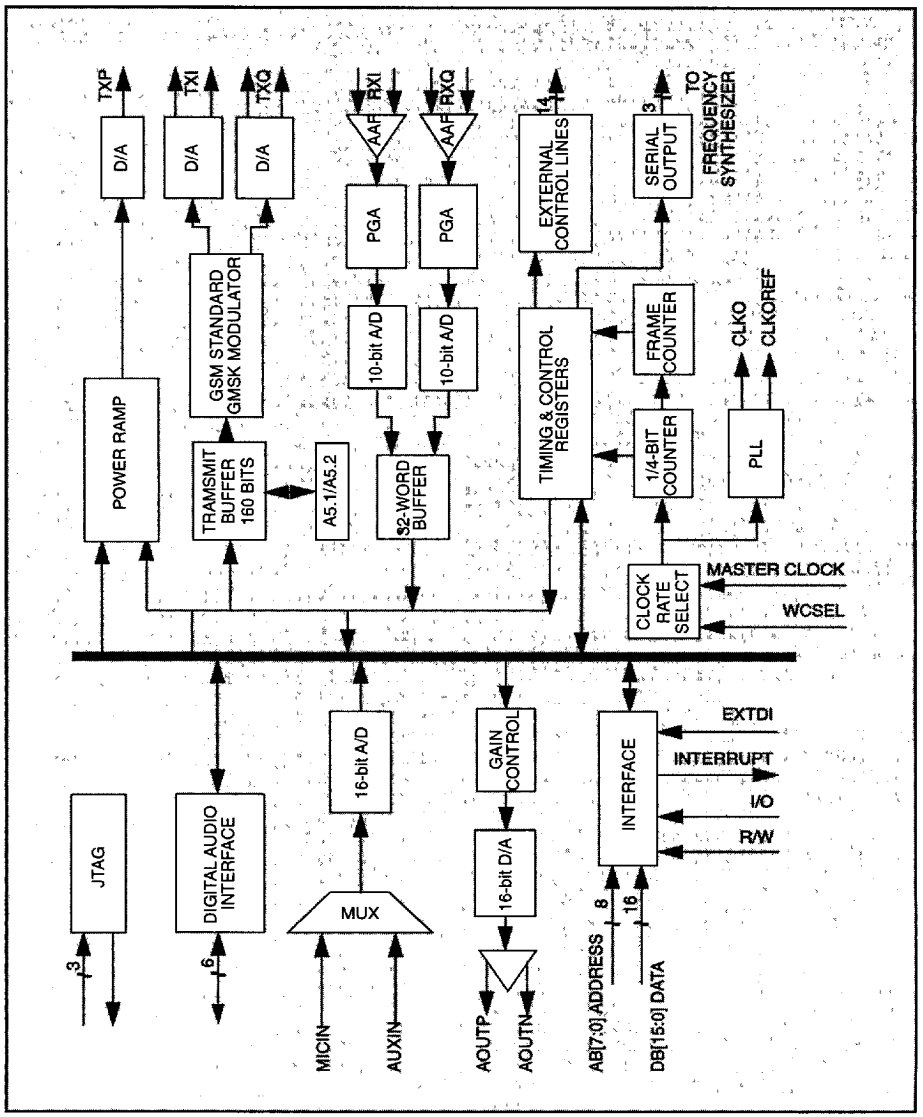


Figure 1. AT&T CSP1088 Block Diagram v2.2

Pin Information

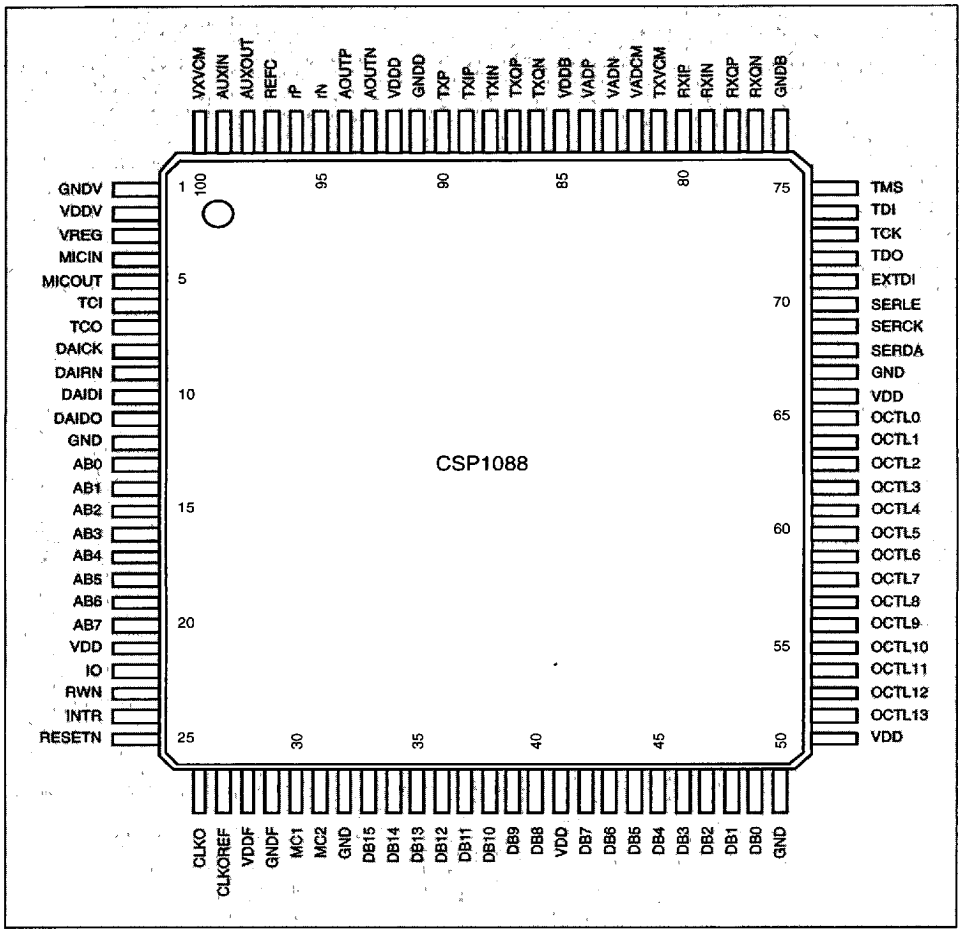


Figure 2. AT&T CSP1088 TQFP Pin Diagram v2.2

Pin Information (continued)

Table 1. Pin Information

100-Pin TQFP	Symbol	Type*	Description
4	MICIN	i, a	Voiceband Microphone Input
5	MICOUT	o, a	Voiceband Microphone Output
99	AUXIN	i, a	Voiceband Auxiliary Input
98	AUXOUT	o, a	Voiceband Auxiliary Output
100	VXVCM	i, a	Voiceband External Bypass Capacitor, Reference
94	AOUTP	o, a	Voiceband Positive Output
93	AOUTN	o, a	Voiceband Negative Output
96	rP	nc	No connect
95	rN	nc	No connect
3	VREG	o, a	Voiceband regulated voltage for electrect cond. microphone
97	REFC	i, a	Voiceband ext. cap. for int. voltage regulator
7	TCO	i, d, PD	Voiceband Digital Audio Interface, Test Control 0
6	TC1	i, d, PD	Voiceband Digital Audio Interface, Test Control 1
9	DAIRN	i, d, PD	Voiceband digital audio interface reset not, active-low
10	DAIDI	i, d, PD	Voiceband digital audio interface data in
11	DAIDO	o, d	Voiceband digital audio interface data out, reset state is low
8	DAICK	o, d	Voiceband digital audio interface clock, reset state is low
89	TXIP	o, a	Baseband Transmit I Component Positive Output
88	TXIN	o, a	Baseband Transmit I Component Negative Output
87	TXQP	o, a	Baseband Transmit Q Component Positive Output
86	TXQN	o, a	Baseband Transmit Q Component Negative Output
90	TXP	o, a	Baseband transmit power control
81	TXVCM	i, a	Baseband transmit external reference. It can set common modes of TXIP,N and TXQP,N
80	RXIP	i, a	Baseband Receive I Component Positive Input
79	RXIN	i, a	Baseband Receive I Component Negative Input
78	RXQP	i, a	Baseband Receive Q Component Positive Input
77	RXQN	i, a	Baseband Receive Q Component Negative Input
82	VADCM	i, a	Baseband 2.4 V analog reference for A/D
84	VADP	i, a	Baseband reference for A/D Positive
83	VADN	i, a	Baseband reference for A/D Negative
30, 31	MC[1:2]	i,d	Small Signal Master Clock Input
33—40	DB[15:8]	i/o, d	Data bus 15—8
42—49	DB[7:0]	i/o, d	Data bus 7—0
20—13	AB[7:0]	i, d	Address bus 7—0
23	RWN	i, d	Read/write not (low = write, high = read)
22	IO	i, d	Chip select to enable data bus I/O
24	INTR	o, d	Interrupt output to DSP, active-high, reset state is low
71	EXTDI	i, d, PD	External digital input, cleared prior to each Rx buffer
25	RESETN	i, d	Reset not, active-low

* i = input, o = output, a = analog, d = digital, pwr = power, gnd = ground, and nc = no connect, PD = on-chip pull-down resistor, PU = on-chip pull-up resistor.

Pin Information (continued)

Table 1. Pin Information (continued)

100-Pin QFP	Symbol	Type*	Description
52—65	OCTL[13:0]	o,d	Output control pins 13 through 0, controlled by state machine, reset state is low
69	SERCK	o,d	Serial clock for Programming External Synthesizer, reset state is low
68	SERDA	o,d	Serial data out for Programming External Synthesizer, reset state is low
70	SERLE	o,d	Serial data latch for Programming External Synthesizer, active-low, reset state is high*
26	CLKO	o,a	Small Signal Clock Output from PLL, reset state is active
27	CLKOREF	o,a	Small Signal Clock Output Reference, low-pass filtered CLKO*
72	TDO	o,d	JTAG Test Data Output, reset state is tri-state*
73	TCK	i,d	JTAG Test Clock
74	TDI	i,d, PU	JTAG Test Data Input
75	TMS	i,d, PU	JTAG Test Mode Select
2	VDDV	pwr	5 V analog supply voiceband
1	GNDV	gnd	0 V analog ground voiceband
28	VDDF	pwr	5 V analog supply PLL
29	GNDF	gnd	Analog ground PLL
85	VDDB	pwr	5 V analog supply baseband
76	GNDB	gnd	Analog ground baseband
92	VDDD	pwr	5 V quiet digital supply
91	GNDD	gnd	Quiet digital ground
21,41,51,66	VDD[3:0]	pwr	3 V digital supply
12,32,50,67	GND[3:0]	gnd	Digital Ground

* I = input, o = output, a = analog, d = digital, pwr = power, gnd = ground, and nc = no connect, PD = on-chip pull-down resistor, PU = on-chip pull-up resistor.

Architectural Information

Figure 1 on page 3 shows a block diagram of the AT&T CSP1088. The AT&T CSP1088 integrates the A/D and D/A functions of the voiceband and baseband channels along with a GMSK modulator, frequency synthesis (PLL), A5 Block Generator, and a timing and control state machine. The timing and control state machine monitors an internal quarter-bit counter and an internal frame counter to control both baseband receive and baseband transmit activity. The state machine can also control up to 14 external elements. The AT&T CSP1088 has a serial output that is designed to program an external frequency synthesizer. The 8-bit address, 16-bit data bus connects easily to the AT&T DSP1600 family.

Event Timing & Control State Machine

Figure 3 on page 8 illustrates the operation of the event timing and control (ETC) state machine by an example. In this example, the state machine has already executed the control word of ETC register 03, and the ETC index register is now pointing to ETC register 04. When the quarter-bit counter (which is currently at 3951) reaches 3984, the control portion of ETC register 04 will be executed. In this example, the AT&T CSP1088 will send a normal burst of 148 bits that are held in the burst data register.

After the match, the ETC index register will automatically be incremented to 05, and the next timing match will occur when the quarter-bit counter reaches 4686. The frame counter will be incremented to 09 when the quarter-bit counter rolls over from 4999 to 0. Depending upon the state of bit 13 of TCNTRL (INCQBCFC) the ETC registers can be programmed in different ways. If INCQBCFC = 0, the ETC index register will increment with every quarter bit counter timing match (the quarter-bit counter equaling the EQN bits from the current ETC register), regardless of the values of the EVEN and ODD bits in the current ETC register. This allows the ETC index register to increment when no event occurs (for example, a timing match occurs and the frame count is 08, but the EVEN/ODD bits are programmed in the current ETC register such that this event only happens on odd frames; therefore, no event occurs). For INCQBCFC = 1, the ETC index register increments only when both the quarter bit timing match occurs and the EVEN/ODD bit criteria is satisfied. In this case, the ETCI register increments only when events occur.

No matter the state of INCQBCFC, the ETC index register is reset to 0 one half 13 MHz cycle after the ETC index register has taken on a value greater than or equal to the value of bits 3 to 0 (DPT [3:0]) in TCNTRL.

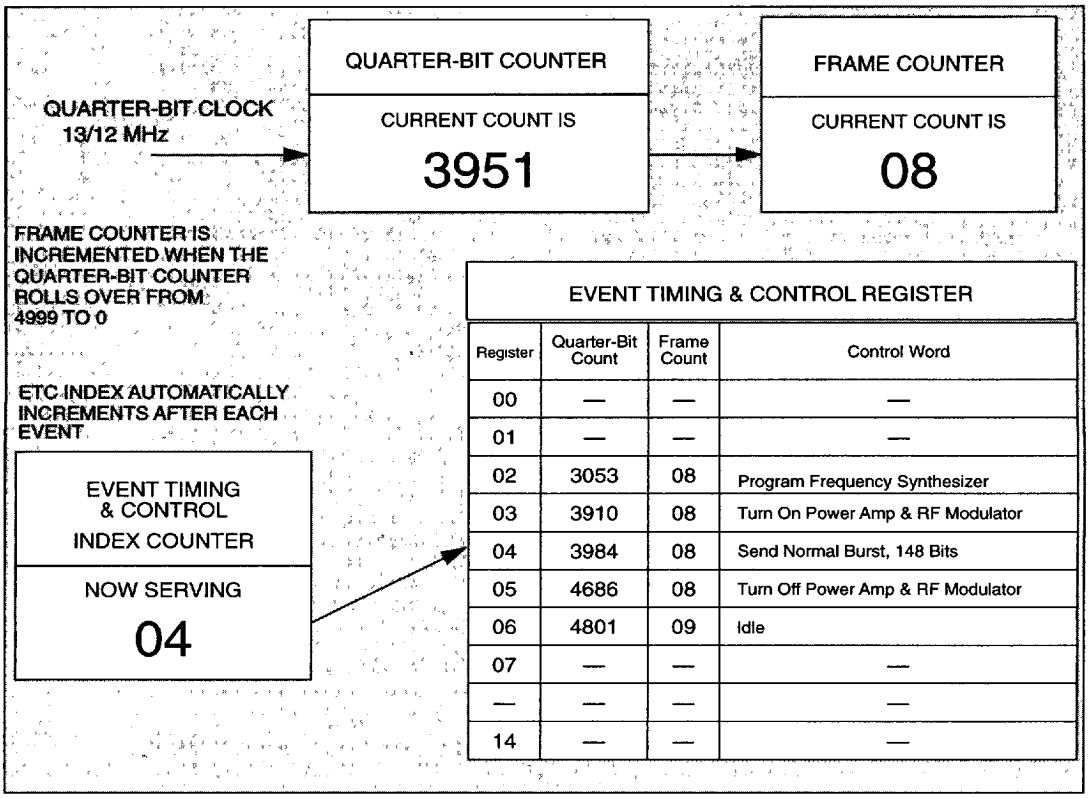
Send Burst Data

As an example of how these components work together, consider how the AT&T CSP1088 sends a normal burst of 148 bits to the RF modulator. The DSP synchronizes the AT&T CSP1088's quarter-bit counter with the base station. The DSP keeps track of exactly when the burst data should arrive at the mobile telephone's RF modulator so that the outgoing data is sent during its assigned time slot. The DSP loads this time into the timing portion of one of the AT&T CSP1088's ETC registers, and it puts the control word for sending a normal data burst into the control portion of that register. The DSP loads the AT&T CSP1088's transmit buffer with148 bits of data.

The AT&T CSP1088 keeps track of the bit count to an eighth-bit accuracy and keeps track of the frame number. When the timing portion of the indexed ETC register matches the bit and frame numbers, the control portion of the register is executed. In the case of a data burst, the control word will cause the AT&T CSP1088's GMSK modulator to process the data held in the transmit buffer. This modulator will convert the data stream into phase information that meets GSM modulation standards. A frequency correction term is added to the phase information, and then the phase is converted into I and Q components. The I and Q components are converted to analog voltages by the baseband D/A converters. The analog output voltages can be connected directly to the I and Q inputs of an RF modulator.

In addition to the I and Q outputs, a power ramp signal is generated to ramp the output power amplifier on and off to avoid frequency spectrum spreading. The power ramp shape is programmable, and the ramping is spread over 9-bit intervals, for both ramp up and ramp down.

Architectural Information (continued)



Register	Quarter-Bit Count	Frame Count	Control Word
00	—	—	—
01	—	—	—
02	3053	08	Program Frequency Synthesizer
03	3910	08	Turn On Power Amp & RF Modulator
04	3984	08	Send Normal Burst, 148 Bits
05	4686	08	Turn Off Power Amp & RF Modulator
06	4801	09	Idle
07	—	—	—
—	—	—	—
14	—	—	—

Figure 3. Event Timing and Control State Machine Example

Receiving Burst Data

The DSP also has to keep track of exactly when its next burst of data will be arriving. The DSP loads a start time into the timing portion of one of the AT&T AT&T CSP1088's ETC registers, and it puts the control word for receiving a burst of data into the control portion of that register. Once this ETC register is indexed, the timing portion of the register is compared to the AT&T CSP1088's internal bit counter and frame counter. When the timing portion of the register matches, the control portion of the register is executed. After the analog dc offset calibration, the baseband A/D converters begin to convert the received I and Q signals into 10-bit digital words.

The AT&T CSP1088 stores the incoming I and Q data pairs in 32 internal double-buffered registers so that the DSP does not have to be interrupted so frequently (each interrupt to the DSP requires some overhead). Once the AT&T CSP1088 receives 16 I and Q data pairs, it issues an interrupt to the DSP to read the data. While the DSP is reading out the 16 I and Q data pairs, the AT&T CSP1088 continues to receive and convert I and Q data pairs which it stores in the other half of the double-buffered registers. The DSP has approximately 59 µs to read the 16 sample pairs before the other half of the double buffer fills.

Architectural Information (continued)

Voiceband Conversion

The voiceband A/D converter generates 16-bit samples at an 8 kHz rate. When a new sample is ready, the AT&T CSP1088 sends an interrupt to the DSP. When the DSP services this interrupt, it should not only read the 16-bit sample from the voiceband input A/D converter, but it should also load a new sample into the voiceband output D/A converter.

The gain of the voiceband output can be lowered in 3 dB steps from 0 dB to –45 dB. The voiceband differential output can be connected directly to a load as low as 15 Ω, such as the earphone of a handset. A digital AUDIO interface is provided for testing. It conforms to GSM specifications.

Programming an External RF Frequency Synthesizer

The AT&T CSP1088 has a serial output port which can be used to program an external frequency synthesizer. The DSP can load frequency information into six different frequency selection registers. The information in the register is sent out the serial port whenever the control portion of an ETC register loads that frequency selection register's address. The serial output can be either 8 bits, 16 bits, or 24 bits, the output rate can be either 1.08 Mbits/s or 0.54 Mbits/s, and the output data direction can be least significant bit or most significant bit first. The output length, output speed, and output data directions are controlled by the timing and control registers.

Output Control Lines

The AT&T CSP1088 has 14 output control pins. These pins are set to logic high or logic low by the control portion of an ETC register when the timing portion of that register matches the internal bit and frame counters. These control lines are typically used to turn on and off external circuits, and to change the gain of programmable amplifiers. They are reset to logic low on RESET. They can also be reset at the end of each TX and/or RX burst.

Ciphering

The AT&T CSP1088 has hardware A5.1 and A5.2 used for ciphering. The transmit burst data buffer is initialized and then the cipher unit generates the output in two blocks under software control.

Frequency Synthesis

An on-chip PLL connects directly to DSP16XX devices using a small signal clock input buffer. Several options are available for activating the PLL including automatic activation via the event timing and control state machine.

Architectural Information (continued)

Frequency Synthesis (continued)

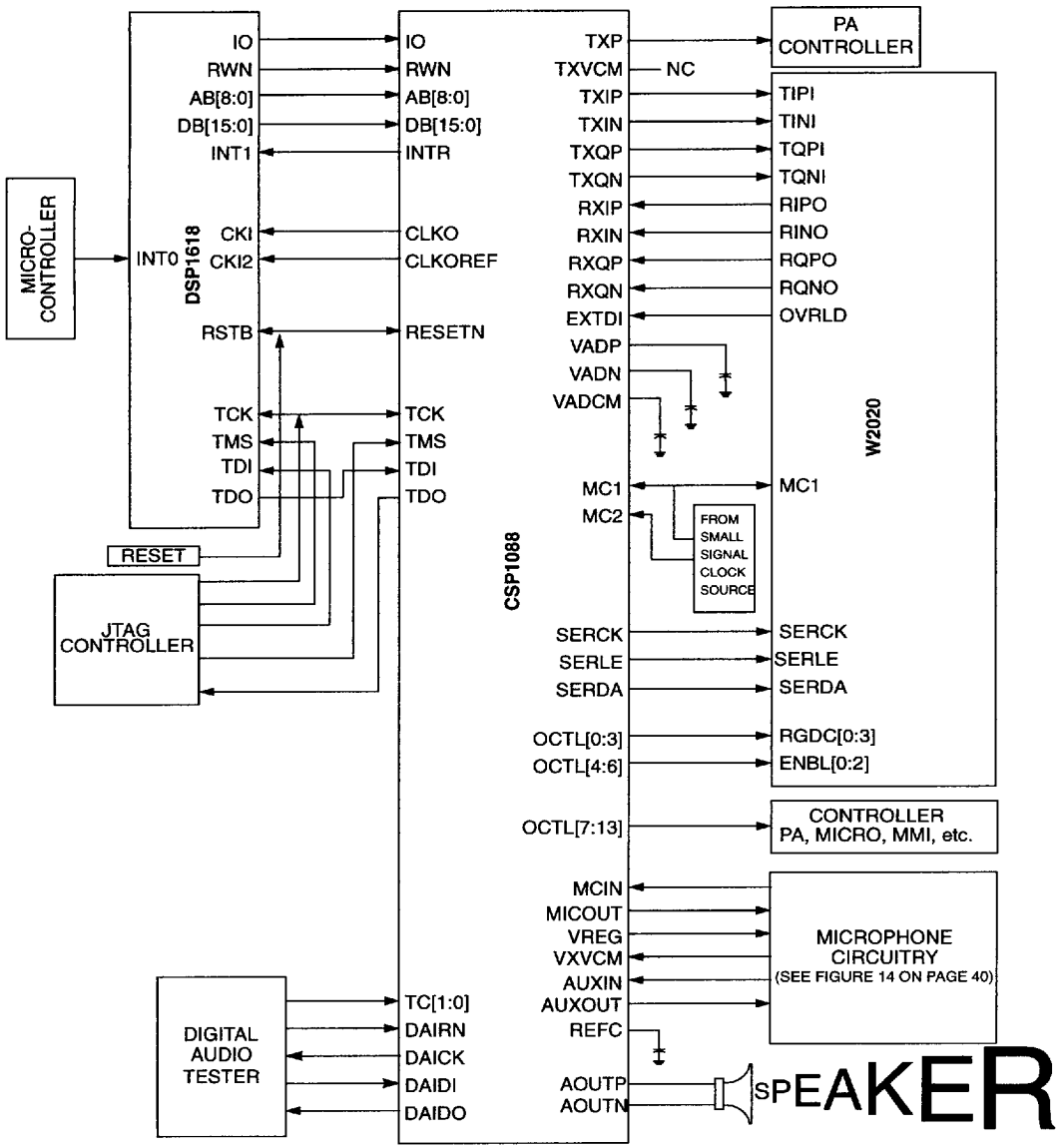


Figure 4. CSP1088 Connection Diagram to DSP1618 and W2020

Register Information

Register Addresses (Memory Map)

WARNING: All unused and reserved register bits must be written with a logic low. Failure to do so may result in damage to the device or erratic behavior.

Table 2. Register Addresses (Memory Map)

Register	Access Method	Hex Address	Value on Reset	Description
INS/INC	R/W	0	0x0000	Interrupt status on read, and interrupt control on write*
CONTROL	R/W	0x1	0x0000	CSP1088 control*
TEST	R/W	0x2	0x0000	Test control*
AUDCONF	R/W	0x4	0x0000	Audio input/output configuration*
AUDIN	R	0x5	X	Audio input data sample
AUDOUT	W	0x6	X	Audio output sample
AUDFCR	R/W	0x7	0x0000	Audio sampling frequency correction*
FC	R/W	0x8	0x0000	Frame counter value*
QBC	R/W	0x9	0x0000	Quarter-bit counter value*
TCNTRL	R/W	0xa	0x0000	Timing and control section control word*
ETCI	R/W	0xb	0x0000	Event timing and control index*
QBCJUMP	W	0xc	0x0000	Quarter-bit jump modification word*
ETC [0:14]	R/W	0x10—0x3c	X	Event time and control word storage
FREQ [0:5]	R/W	0x40—0x4b	X	Frequency word storage
BRSTDATA [0:9]	R/W	0x50—0x59	X	Burst data registers
FCR	W	0x5a	X	Transmit frequency correction register
RAMPLVL	R/W	0x5f	X	Power ramp output nominal level value
RAMPUP [0:15]	R/W	0x60—0x6f	X	Power ramp up values
RXBUFF [0:31]	R	0x70—0x8f	X	Receive data buffer for I, Q values
CLKOCNTL	R/W	0x90	0x0000	Clock output control word
RAMPDN [0:15]	R/W	0xe0—0xef	X	Power ramp down values

* There may be up to three 13 MHz cycles before the register is updated with a write. Back-to-back writes in less time should be avoided.

Interrupt Status and Interrupt Control Register, INS/INC (Address 0x0)

Interrupt status and interrupt control registers are both located at address 0. When this register is read, it is considered the interrupt status register, and Table 3 on page 12 describes the meanings of its 16 bits. When this register is written to, it is considered the interrupt control register, and Table 4 on page 12 describes what happens to each bit during a write operation.

This register is designed such that when the DSP reads the interrupt register, it can write the same word back into the register to reset the serviced interrupt. Typically, the bits 1—7 should be reset to low after they are serviced, so writing a logic high to any of these bits will reset them to a logic low. Writing a logic low to any of these bits will leave them unchanged. Bit 0 does not change after an interrupt, so writing a logic high to this bit will set it high, and writing a logic low to this bit will reset it low.

Register Information (continued)

Interrupt Status and Interrupt Control Register, INS/INC (Address 0x0) (continued)

Table 3. Interrupt Status Register (Read Cycle)

Name	Bit Number	Description
EOTXIES	0	End of transmit interrupt enable status
EOTXI	1	End of transmit interrupt
RXBUFI	2	Receive buffer interrupt
AUDI	3	Audio interrupt
A5I	4	A5 Interrupt
TIMEI	5	Time-out interrupt
EXTOV	6	External overflow indication, cleared when Rx starts, and at the start of each 16 receive pairs
INTOV	7	Internal overflow indication
A5IES	8	A5 interrupt enable status
r	9—15	Reserved

Table 4. Interrupt Control Register (Write Cycle)

Name	Bit Number	Description
EOTXIE	0	End of transmit interrupt enable. Logic high sets; logic low resets
CEOTXI	1	Clear end of transmit interrupt. Logic high resets; logic low leaves unchanged
CRXBUFI	2	Clear receive interrupt. Logic high resets; logic low leaves unchanged
CAUDI	3	Clear audio interrupt. Logic high resets; logic low leaves unchanged
CA5I	4	Clear A5 Interrupt
CTIMEI	5	Clear time-out interrupt. Logic high resets; logic low leaves unchanged
X	6	This bit cannot be changed by an external write
X	7	This bit cannot be changed by an external write
A5IE	8	A5 interrupt enable
r	9—15	Reserved

EOTXIES: End of Transmit Interrupt Enable Status

When set to a logic high, the end of transmit interrupt, EOTXI, is enabled.

EOTXI: End of Transmit Interrupt

EOTXI is set to a logic high at the end of a transmitted burst if enabled by EOTXIES. The transmitted burst is considered ended on the clock cycle that the power ramping finishes on.

RXBUFI: Receive Buffer Interrupt

RXBUFI is set to a logic high when 16 receive I samples and 16 receive Q samples have been stored in the 32 double-buffered receive registers, RXBUFF[31:0]. The values of these registers must be read before the AT&T CSP1088 finishes receiving the next 16 I and 16 Q samples (which takes about 59 µs) or else the information could be overwritten and lost. Whenever a receive interrupt occurs, EXTOV and INTOV interrupt bits are also updated (see description below).

Register Information (continued)

Interrupt Status and Interrupt Control Register, INS/INC (Address 0x0) (continued)

AUDI: Audio Interrupt

AUDI is set to a logic high when a new sample from the audio input is written into the AUDIN register. This sample must be read before the next sample arrives (which is in about 125 µs). The AUDI interrupt is also considered a request for a new audio output sample, and a new audio output sample should be written to the AUDOUT register.

A5I

When logic high, A5I indicates that a block cipher, either BLOCK 1 or BLOCK 2, has finished.

TIMEI: Time-Out Interrupt

There are 15 event timing and control registers, ETC[14:0]. When the timing information of a selected ETC register matches the quarter-bit counter, QBC, and the frame counter, FC, the control portion of the word may set the DSP interrupt bit, DSPI. When DSPI is set to a logic high, an interrupt is issued, and the time-out interrupt bit, TIMEI, is set to a logic high. Also, if CLKO had been disabled, TIMEI asserting will enable CLKO; if CLKO has been enabled, CLKO remains enabled (see Table 43 on page 35).

EXTOV: External Overflow Indication

EXTOV is set to a logic high if an external overload condition occurred anytime during the previous 16-sample receive time period. An external overload condition is sensed whenever a logic high is applied to the EXTDI pin for at least one MC cycle. EXTOV is updated whenever a receive interrupt, RXBUFI, occurs.

INTOV: Internal Overflow Indication

INTOV is set to a logic high if an internal overload of the I or Q receive ADC occurs anytime during the 16-sample receive time period. INTOV is updated whenever a receive interrupt, RXBUFI, occurs.

A5IES

When logic high, the A5 interrupt, A5IE, is enabled (logic high).

EOTXIE: End of Transmit Interrupt Enable

When EOTXIE is set to a logic high, the end of transmit interrupt, EOTXI, is enabled. When EOTXIE is reset to a logic low, the end of transmit interrupt, EOTXI, is disabled.

CEOTXI: Clear End of Transmit Interrupt

When CEOTXI is set to a logic high, the end of transmit interrupt bit, EOTXI, is reset to a logic low (cleared). When CEOTXI is set to a logic low, EOTXI is unchanged.

CRXBUFI: Clear Receive Interrupt

When CRXBUFI is set to a logic high, the receive interrupt bit, RXBUFI, is reset to a logic low (cleared). When CRXBUFI is set to a logic low, RXBUFI is unchanged.

CAUDI: Clear Audio Interrupt

When CAUDI is set to a logic high, the audio interrupt bit, AUDI, is reset to a logic low (cleared). When CAUDI is set to a logic low, AUDI, is unchanged.

CA5I

When CA5I is written logic high, the A5I bit is reset to logic low (cleared). When CA5I is reset to logic low, A5I is unchanged.

CTIMEI: Clear Timing Interrupt

When CTIMEI is set to a logic high, the time-out interrupt bit, TIMEI, is reset to a logic low (cleared). When CTIMEI is set to a logic low, TIMEI is unchanged.

A5IE

When A5IE is set logic high, the A5 interrupt is enabled. After either BLOCK 1 or BLOCK 2 ciphers are generated, and A5IE was set logic high, the INTR pin is asserted, and A5I is set logic high.

Register Information (continued)

CSP1088 Control Register, CONTROL (Address 0x1)

The CONTROL register determines whether the output controls bits are cleared at the end of a transmit burst and/or at the end of a receive burst. The CONTROL register also determines whether the transmit output modulation uses clockwise rotation or counter clockwise rotation, and the order in which I and Q samples are received. Table 5 describes how the CONTROL register regulates output control bits, transmit output modulation, and I and Q sample receiving.

The CONTROL register has additional bits specified for use in A5 block generation, device reset, MC disabling, and receive bandwidth selection.

Table 5. CSP1088 Control Register, CONTROL (Address 0x1)

Name	Bit Number	Description*
CTLCLREOT	0	Logic high, output control bits OCTL[13:0] are reset low after transmit burst Logic low, output control bits OCTL[13:0] are not changed after transmit burst
CTLCLREOR	1	Logic high, output control bits OCTL[13:0] are reset low after receive burst Logic low, output control bits OCTL[13:0] are not changed after receive burst
MODROT	2	Logic high, negative or clockwise modulation rotation Logic low, normal or counterclockwise modulation rotation
RBORD	3	Logic high, receive buffer order first Q then I Logic low, receive buffer order first I then Q
RXDCCAL	4	Logic high, initiates digital RX dc offset calibration
RESET	5	Logic high, generates software reset
MCSTOP	6	Logic high, stops master clock at input pin
r	7	Reserved
RBWS	8	Receive Filter Bandwidth Select: "0" = 75 kHz, "1" = 95 kHz
r	9—10	Reserved
A5ENBL	11	A5 algorithm enabled (start) self resetting
A5TYPE	12	Write logic high, A5.1 algorithm selected Write logic low, A5.2 algorithm selected
A5DIR	13	Write logic low, bits in reverse order to register bits Write logic high, bits in same order to register bits
A5BLOCK	14	Write logic low, BLOCK 1 Write logic high, Generate BLOCK 2
A5STAT	15	Write logic low, no affect Write logic high, clear status to zero when read Read logic high, Block generation complete

* All bits are exactly as described in the AT&T CSP1088 v2.0 data sheet except bit 8.

Register Information (continued)

CSP1088 Control Register, CONTROL (Address 0x1) (continued)

Output Control Bits Clear at End of Transmit, CTLCLREOT

The output control bits are used to control various external circuits such as powering up the receiver, or the power amplifier. If the CTLCLREOT bit is set to a logic high, then the output control bits, OCTL[13:0], are reset to a logic low after the end of a transmit burst. If the CTLCLREOT bit is reset to a logic low, then the OCTL[13:0] are not reset at the end of a transmit burst.

Output Control Bits Clear at End of Receive, CTLCLREOR

The output control bits are used to control various external circuits such as powering up the transceiver, or the power amplifier. If the CTLCLREOR bit is set to a logic high, then the output control bits, OCTL[13:0], are reset to a logic low after the end of a receive burst. If the CTLCLREOR bit is reset to a logic low, then the OCTL[13:0] are not reset at the end of a receive burst.

Modulation Rotation, MODROT

When the modulation rotation bit, MODROT, is set to a logic high, then the rotation of the output phase at TxI and TxQ is clockwise, or negative. When MODROT is reset to a logic low, then the rotation of the output phase is in the normal counterclockwise direction.

Receive Buffer Order, RBORD

Sixteen I and Q sample pairs are stored in 32 double-buffered registers. When the receive buffer order bit, RBORD, is set to a logic high, then the received samples are stored first Q then I such that the lowest address (address 0) is Q0, and the next address (address 1) is I0, and so on until I15 is stored in the highest address (address 31). When RBORD is reset to a logic low, then the received samples are stored in the normal order of first I and then Q.

Receive Digital dc Offset Calibration, RXDCCAL

When the receive dc offset calibration bit, RXDCCAL is set high, both I and Q receive channels perform a dc offset calibration. This **must** be done once before using the receive channel for the first time. It is recommended that it be done prior to any other programming of the AT&T CSP1088. When read, RXDCCAL indicates that the dc offset calibration is completed if logic low, or that calibration is active if logic high.

System Reset, RESET

Setting this bit high resets the AT&T CSP1088. This reset is identical to a reset initiated by the reset pin. This bit clears itself when reset is complete, which requires approximately eight cycles.

Master Clock Stop Bit, MCSTOP

When the master clock stop bit, MCSTOP, is set high, the master clock (MC) is stopped at the input pin. Only the CONTROL register may be written to in this state, usually to turn the clock on again or reset the AT&T CSP1088.

RBWS

Receive bandwidth select (see page 16).

A5 Enable, A5ENBL

When set, A5ENBL enables the A5 algorithm. When reset, A5ENBL will immediately stop and reset the generator. Data should be in the TX buffer before enabling A5. After the BLOCK 2 has been generated, this bit self-resets.

A5 Type, A5TYPE

When set to logic high, A5TYPE selects the A5.1 algorithm generation. When set to logic low, A5TYPE selects A5.2 algorithm generation.

A5 Direction, A5DIR

When set to logic high, A5DIR selects key, count, and block bit ordering as given in Table 33, Table 34, and Table 36. When set logic low, the key, count and block bit ordering is as given in Table 31, Table 32, and Table 35.

A5 BLOCK Select, A5BLOCK

When set logic high, A5BLOCK selects BLOCK 2 generation. When set logic low, this selects BLOCK 1 generation. After the BLOCK 2 has been generated, this bit self-resets.

A5 Status and Control, A5STAT

When written logic high, A5STAT resets itself to logic low. This must be done prior to every block generation. When read, logic high indicates a block generation has completed, and logic low means a block generation has not started or is processing.

Register Information (continued)

CSP1088 Control Register, CONTROL (Address 0x1) (continued)

Receive Bandwidth Selection (RBWS)

The receive digital filter 3 dB bandwidth is selectable from 75 kHz to 95 kHz. When logic 0, RBWS selects 75 kHz bandwidth; logic high selects 95 kHz bandwidth. Figures 5 and 7 illustrate a spectral response, including a passband, for the 75 kHz bandwidth, and Figures 6 and 8 illustrate a spectral response, including a passband, for the 95 kHz bandwidth. Selecting 75 kHz bandwidth attenuates a GSM modulated signal with ±200 kHz center frequency (the adjacent channel) by 20 dB, whereas the 95 kHz bandwidth attenuates that signal by 16 dB.

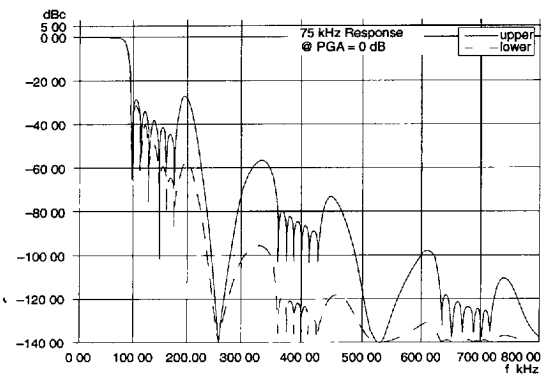


Figure 5. 75 kHz Response

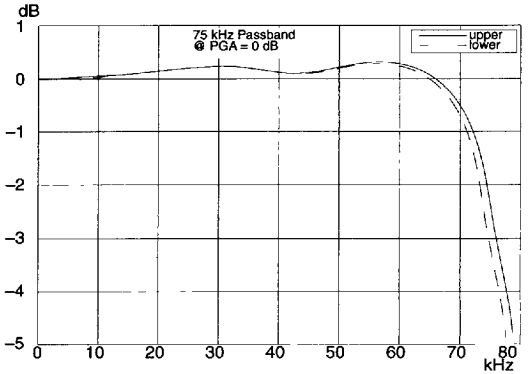


Figure 7. 75 kHz Passband

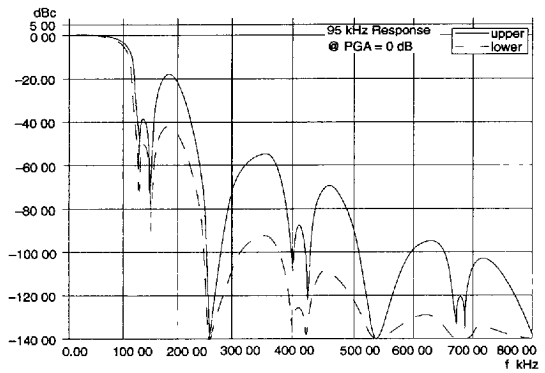


Figure 6. 95 kHz Response

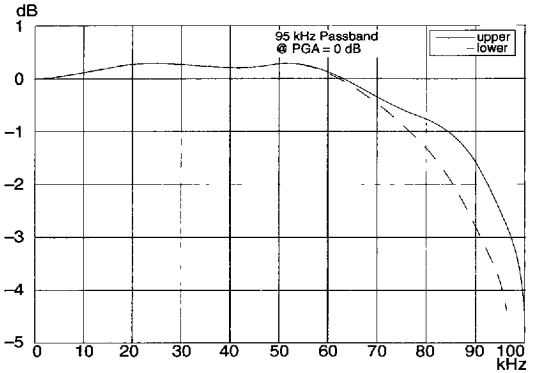


Figure 8. 95 kHz Passband

Register Information (continued)

Test Control Register, TEST (Address 0x2)

The TEST register provides a serial interface for direct access to the audio input and output data streams. This interface is used to test the audio section of the AT&T CSP1088 and has four modes of operation: 1) normal, 2) speech decoder/DTX functions on downlink, 3) speech encoder/DTX functions on uplink, and 4) test of acoustic devices and A/D and D/A functions. The test register, TEST, selects the mode of the digital audio interface. This register also is used to stop continuous receive or transmit and to select the MC frequency.

Table 6. Test Register, TEST, Bit Definitions

Name	Bit Number	Description
TCSOURCE	0	Logic high, test control source is hardware pins TC[0:1] Logic low, test control source is software bits TESTC[0:1]
TESTC[0:1]	1—2	Selects the digital audio interface mode
STOP	3	When the CSP1088 is in a continuous transmit or receive mode, setting this bit to a logic high will stop the transmission or reception of data
r	4—11	Reserved
MCSEL	12	Master clock frequency select
r	13—15	Reserved

Table 7. Test Register, TEST, Bit Definitions

TC 1 or TESTC 1	TC 0 or TESTC 0	Description
0	0	Normal operation of audio circuits
0	1	Output data emulating D/A samples (speech decoding test)
1	0	Input data emulating A/D samples (speech encoding test)
1	1	Test of acoustic devices and A/D and D/A

Test Control Source Bit, TCSOURCE

When the TEST control source bit, TCSOURCE, is set to a logic high, the digital audio interface is controlled by the values at the hardware pins TC[0:1]. When reset to a logic low, the digital audio interface is controlled by the values of bits TESTC[0:1]. Table 6 shows which test states are selected for a given input.

Test Control Bits (TESTC[0:1])

When the TCSOURCE is reset to a logic low, the TESTC[0:1] bits control the digital audio interface. Table 6 describes the different test states.

Continuous Operation Stop Bit, STOP

Setting the STOP bit to a logic high stops the mode of continuous transmitting and continuous receiving. Resetting the STOP bit to a logic low allows the receive and transmit to operate normally. When transmitting, the STOP bit causes the current data symbol to finish, then the ramp down sequence, with guard bits, follows until transmission stops. When receiving, the current 32 sample buffer finishes filling and one last RXBUFI interrupt is generated, then the receive mode stops. This bit is not self-clearing and should be reset to logic low before using RX or TX.

Master Clock Frequency Select Bit, MCSEL

The Master Clock Frequency is selectable between 26 MHz and 13 MHz. Setting MCSEL to logic 0, the reset state configures this device for 13 MHz input. Setting MCSEL to logic 1 configures this device for 26 MHz input.

Register Information (continued)

Audio Input/Output Configuration Register, AUDCONF (Address 0x4)

The AUDCONF register controls the configuration of the voice input and voice output sections of the AT&T CSP1088. For the input section, this register selects the internal gain (18 dB or 8 dB), enables the input or not, and selects between MICIN and AUXIN inputs. For the output section, this register selects the gain from –45 dB to 0 dB in 3 dB steps, enables the audio output or not, selects dithering or not, and mutes the audio output or not. Also, this register can select a loopback mode that takes the digital output of the input A/D converter, and loop it directly back to the digital output section for partial testing.

The Audio Output pins Aoutp and Aoutn support a wide variety of load impedances and power. Three programmable bits define a high or low bias condition and four voltage gains for the output drive stage. This is in addition to the programmable gain output over a 45 dB range.

Table 8. Audio I/O Configuration Register, AUDCONF, Bit Definitions

Name	Bit Number	Description
AUDIE	0	**Audio Input Enable.** Logic high enables audio input. Logic low disables audio input
AUDIG	1	**Audio Input Gain.** Logic low selects 8 dB of internal gain before A/D converter. Logic high selects 18 dB of internal gain
AUDIS	2	**Audio Input Select.** Logic high selects AUXIN. Logic low selects MICIN
AUDCHR	3	**Audio Input Charge.** Charge external reference capacitor
AUDOE	4	**Audio Output Enable.** Logic high enables audio output. Logic low disables audio output
AUDOG[0:3]	5—8	**Audio Output Gain.** Gain of the audio output can be selected from –45 dB (all low) to 0 dB (all high) in 3 dB steps
AUDOM	9	**Audio Output Mute.** Logic low mutes. Logic high unmutes
ADITH	10	**Audio Output Dithering.** Logic low selects dithering to decorrelate periodic modular quantization noise. Logic high selects no dithering
r	11	**Reserved.**
AUDPGA[1:0]	13:12	**Audio PGA.**
AUDHD	14	**Audio High Drive.**
r	15	**Reserved**. Reset to logic low

Register Information (continued)

Audio Input/Output Configuration Register, AUDCONF (Address 0x4) (continued)

Audio Input Enable, AUDIE

When the audio input enable, AUDIE, is set to a logic high, the audio input is enabled. When AUDIE is reset to a logic low, the audio input section is powered down.

Audio Input Gain, AUDIG

When the audio input gain bit, AUDIG, is reset to a logic low the internal gain before the A/D converter is 8 dB, with either MICIN or AUXIN selected. If AUDIG is set to a logic high, the internal gain of the audio input is 18 dB.

Audio Input Select, AUDIS

When the audio input select, AUDIS, is set to a logic high, the AUXIN input is selected. When AUDIS is reset to a logic low, the MICIN input is selected.

Audio Input Charge, AUDCHR

When the audio input charge, AUDCHR, is set to a logic high, the external reference capacitor is charged. When AUDCHR is reset to a logic low, the external reference capacitor is connected to the common mode through a 100 kΩ resistor. This bit should be logic high for 30 ms + 10 R_{IC_I} time constants and then reset before using the voice input section.

Audio Output Enable, AUDOE

When the audio output enable, AUDOE, is set to a logic high, the audio output section is powered on. When AUDOE is set to a logic low, the audio output section is powered down.

Audio Output Gain, (AUDOG[0:3])

The audio output gain bits, AUDOG[0:3], vary the gain of the audio output section from –45 dB to 0 dB in 3 dB steps. Table 9 describes the gain added by each bit when set to a logic high.

Table 9. Audio Output Gain Bit Definition

Bit	Description
AUDOG 0	Logic high adds 3 dB. Logic low adds 0 dB
AUDOG 1	Logic high adds 6 dB. Logic low adds 0 dB
AUDOG 2	Logic high adds 12 dB. Logic low adds 0 dB
AUDOG 3	Logic high adds 24 dB. Logic low adds 0 dB

Register Information (continued)

Audio Input/Output Configuration Register, AUDCONF (Address 0x4) (continued)

Audio Output Mute, AUDOM

When the audio output mute bit, AUDOM, is set to a logic low, the audio outputs, AOUTP and AOUTN, are muted. When AUDOM is set to a logic high, the audio outputs are not muted.

Audio Output Dither, ADITH

When the audio output dither bit, ADITH, is reset to a logic low, dithering is enabled. Dithering decorrelates the periodic modulator quantization noise of the output sigma-delta converter. If ADITH is set to a logic high, dithering is disabled.

Audio Loopback Mode, ALM

When audio loopback mode, ALM, is set to a logic high, the single-bit output of the audio-input sigma-delta A/D converter is looped back into the single-bit input of the audio-output delta-sigma D/A converter. Loopback mode is used for testing. When ALM is reset to logic low, loopback is disabled.

Audio PGA, AUDPGA[1:0]

The audio output analog gain is selected by AUDPGA[1:0]. The differential impedance of the load on pins Aoutp and Aoutn, and the requirement for distortion at the output, determine the settings for these bits. The minimum load depends on the maximum output current.

Table 10. Audio PGA, AUDPGA [2.0], Bit Definition

AUDPGA1	AUDPGA0	Full-Scale Vout rms at AUDOG[3:0]=0 dB Setting	Minimum Load Impedance (Max Distortion=1% for 1 kHz Sine Wave Output)
0	0	1.5	200 Ω
0	1	0.75	80 Ω
1	0	0.375	30 Ω
1	1	0.1875	15 Ω*

* It is recommended that audhd be set to a logic high for this condition.

Audio High Drive, AUDHD

Set to logic high, AUDHD places the audio output driver into high bias, which reduces the analog distortion by about half. When reset logic low, the driver dissipates about 3 mW less quiescent power. We recommend setting AUDHD to logic high for load impedances less than 30 Ω.

Audio Input Double-Buffered Register, AUDIN (Address 0x5)

Audio input is converted into 16-bit 2's complement numbers at an 8 kHz rate. As each 16-bit sample becomes available, it is stored in the double-buffered register AUDIN, an audio interrupt is initiated, and the audio interrupt bit in the interrupt status register, INS, is set to a logic high.

When the DSP reads the audio-input register, it should update the audio-output register, AUDOUT, also.

Table 11. Audio Input Double-Buffered Register, AUDIN

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	AI 15	AI 14	AI 13	AI 12	AI 11	AI 10	AI 9	AI 8	AI 7	AI 6	AI 5	AI 4	AI 3	AI 2	AI 1	AI 0

Register Information (continued)

Audio Output Register, AUDOUT (Address 0x6)

The audio output D/A converter takes linear 16-bit, 2's complement numbers at an 8 kHz rate. Each 16-bit number must be loaded into the audio output register, AUDOUT. The audio output register should be updated whenever an audio interrupt, AUDI, occurs.

Table 12. Audio Output Register, AUDOUT

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	AO 15	AO 14	AO 13	AO 12	AO 11	AO 10	AO 9	AO 8	AO 7	AO 6	AO 5	AO 4	AO 3	AO 2	AO 1	AO 0

Audio Frequency Correction Register, AUDFCR (Address 0x7)

Because the mobile's master clock frequency may differ from the serving cell's, adjustment to the audio sampling rate is necessary to match the serving cell's rate. The audio section's sampling frequency is modified through the AUDFCR register. The parts per million master clock cycles of correction is determined by the following equation:

$$ASFC_{ppm} = \frac{10^6}{13(8192 - MAG[12:0])\,(128 - 112 \cdot SFCR)}$$

Table 13. AUDFCR Register Bit Definition

Bit #	7	6	5	4	3	2	1	0
Label	MAG7	MAG6	MAG5	MAG4	MAG3	MAG2	MAG1	MAG0

Bit #	15	14	13	12	11	10	9	8
Label	ASFCE	ASFCR	ASFCS	MAG12	MAG11	MAG10	MAG9	MAG8

Audio Frequency Correction Magnitude, MAG[12:0]

The magnitude of the correction is determined by the MAG[12:0] bits, ranging from 0 to 8191.

Audio Frequency Correction Sign, ASFCS

The sign of frequency correction is defined by ASFCS. Set logic high, ASFCS makes the nominal 8 kHz sampling frequency lower by ASFCppm. Reset logic low, ASFCS makes the frequency higher.

Audio Frequency Correction Range, ASFCR

There are two ranges of audio frequency correction, high and low, defined by ASFCR. For low ppm correction, ASFCR should be reset logic low. For higher ppm correction, ASFCR should be set logic high.

Audio Frequency Correction Enable, ASFCE

Audio sampling frequency correction is enabled by ASFCE. Set logic high, frequency correction is enabled. If ASFCE is reset logic low, audio frequency correction is disabled, providing a sampling frequency of MC/1625 or MC/3250 depending on MCSEL in the test register.

Audio Sampling Rate Example

The AUDFER register allows adjustments to the audio rate (nominally 8 ks/s) over a range of ±20 ppm with a resolution of less than 0.1 ppm. To cover this range with the indicated resolution, the ASFCR bit should be set to ZERO to make adjustments within the ±7.5 ppm range and set to 1 otherwise. Given the desired ppm adjustment, the decimal value to be programmed into MAG[12:0] is given by:

$$MAG = 8192 - \frac{10^6}{13 \cdot ASFC_{ppm}\,(128 - 112 \cdot ASFCR)}$$

Example, if the desired correction is +1.7 ppm; ASFCR = 0, ASFCppm = 1.7, then Mag is 7838 from the equation above. The AUDFCR register should be programmed to 0x9e9e. If the desired correction had been −1.7 ppm, then the ASFCS bit would have been set to 1and AUDFCR register would have been programmed to 0xbe9e.

Register Information (continued)

Frame Counter Register, FC (Address 0x8)

The frame counter register, FC, is either a modulus 51 counter, or else a modulus 26 counter, depending on the setting of the MFRAME bit in the timing control register, TCNTRL. When MFRAME is set high, the FC counter is modulus 51 (counter cycles 0 through 50 and then back to 0, i.e., frame MOD 51), and when MFRAME is reset low, the FC counter is modulus 26.

FC keeps track of the value of the frame number and can be preset to any number from 0 to decimal 50. FC increments when the quarter-bit counter, QBC, rolls over from 4999 to 0. The value of FC can be read at any time.

Table 14. Frame Counter Register

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	X	X	X	X	X	X	X	X	X	X	FC 5	FC 4	FC 3	FC 2	FC 1	FC 0

Quarter-Bit Counter Register, QBC (Address 0x9)

The quarter-bit counter register is a modulus 5000 counter (cycles from 0 to 4999 and then back to 0) that counts in half-quarter (1/8) bit increments, or at a rate of 13/6 MHz. The counter can be preset to any number from 0 to decimal 4999, and can be read at any time. Note that the counter is written and read with quarter-bit accuracy, and the half-quarter (1/8) bit is only affected by the 13/6 MHz clock, or the INCR/DECR bits in TCNTRL.

Table 15. Quarter-Bit Counter Register Bit Definition

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	X	X	X	QBC 12	QBC 11	QBC 10	QBC 9	QBC 8	QBC 7	QBC 6	QBC 5	QBC 4	QBC 3	QBC 2	QBC 1	QBC 0

QBC Jump, QBCJUMP[12:0] (Address 0xC)

The AT&T CSP1088 supports synchronous QBC offset modification of the QBC register value for large offsets. The QBC register accepts unsigned magnitude values of 0 through 4999. When QBCJUMP is written, the QBC counter will change to its current value plus the QBC Jump value modulus 5000, i.e., (QBC + N) MOD 5000. Thus, if QBCJUMP is written N, then written 5000 – N, the original QBC timeline will remain exactly as if QBC Jump was never written, except for the time between writes. FC, the frame counter, is not affected by QBCJUMP. The delay from RWN rising edge to change in QBC value is no more than two quarter-bit clocks (i.e., half a symbol). The new QBC value is used immediately in the comparisons for time match given that TCNTRL remained constant.

Table 16. QBCJUMP Register Bit Definition

Bit #	7	6	5	4	3	2	1	0
Label	QBCJ7	QBCJ6	QBCJ5	QBCJ4	QBCJ3	QBCJ2	QBCJ1	QBCJ0

Bit #	15	14	13	12	11	10	9	8
Label	r	r	r	QBCJ12	QBCJ11	QBCJ10	QBCJ9	QBCJ8

Register Information (continued)

Timing and Control Register, TCNTRL (Address 0xA)

The timing and control register, TCNTRL, sets the modulus of the ETCI counter and the modulus of the frame counter. It also can reset the quarter-bit and frame counters to 0, and it controls the serial output port. TCNTRL can also be used to increment or decrement the quarter-bit counter in eighth-bit steps.

Table 17. Description of the Timing and Control Register, TCNTRL

Bit #	7	6	5	4	3	2	1	0
Label	SERSPE	SERLEN 1	SERLEN 0	SERDIR	DPT 3	DPT 2	DPT 1	DPT 0

Bit #	15	14	13	12	11	10	9	8
Label	r	r	INCQBCFC	TIMECLK	DECR	INCR	CRESET	MFRAME

Depth (DPT[3:0]) Bits

The event timing and control index counter, ETCI, indexes which one of the 15 event timing and control registers, ETC[14:0], is active. The ETCI counter increments from 0 up to one less than the number specified in the depth bits, DPT[3:0], and then returns to 0 within two 13 MHz clock cycles. The depth bits, therefore, set the modules of the ETCI counter.

In the case of the DPT [3:0] bits all set to a logic low, none of the ETC[14:0] words are ever indexed, and no events are generated.

In the case of the DPT[3:0] bits set to 0001, the ETCI counter will only index Event Timing and Control Register 0 (ETC0). Given a nonmodified (no increment or decrement) quarter-bit counter scenario, a DPT[3:0] = 0001 condition will cause ETC0 to be executed six times when the EQN bit of ETC0 equals the quarter-bit counter. When this is happening, it may not be obvious for most ETC0 values, but when the DSPI bit is set in ETC, the INTR pin of the CSP1088 may behave abnormally, depending on the interrupt servicing latency of the software.

Serial Output Direction Bit, SERDIR

The frequency selection registers, FREQ[5:0], can be used to program an external frequency synthesizer via the serial output pins, SERCK, SERDA, and SERLE. The serial output direction bit, SERDIR, controls whether the data is clocked from LSB to MSB, or from MSB to LSB. When the SERDIR bit is set to a logic high, the data is transmitted from MSB to LSB. When the SERDIR bit is reset to a logic low, the data is clocked from the LSB to the MSB.

Serial Output Length Bits (SERLEN[1:0])

The frequency selection registers, FREQ[5:0], can be used to program an external frequency synthesizer via the serial output pins, SERCK, SERDA, and SERLE. The serial output length bits, SERLEN[1:0], control whether the output is 8 bits, 16 bits, or 24 bits long.

Table 18. Serial Output Length Bit Definition

SERLEN 1	SERLEN 0	Description
0	0	Send first 8 bits (FS[7:0])
0	1	Send first 16 bits (FS[15:0])
1	0	Send first 24 bits (FS[23:0])
1	1	Reserved

Register Information (continued)

Timing and Control Register, TCNTRL (Address 0xA) (continued)

Serial Output Speed Bit, SERSPE

The frequency selection registers, FREQ[5:0], can be used to program an external frequency synthesizer via the serial output pins, SERCK, SERDA, and SERLE. When the serial output speed bit, SERSPE, is set to a logic high, the serial output data rate is 1.08 Mbits/s. When SERSPE is reset to a logic low, the serial output data rate is 0.54 Mbits/s.

Modulus of Frame Counter Bit, MFRAME

When the MFRAME bit is set to a logic high, the frame counter, FC, is a modulus 51 counter (that is, the counter will cycle from 0 to 50 and back to 0 again). When the MFRAME bit is reset to a logic low, the frame counter is a modulus 26 counter and cycles from 0 to 25 and back to 0.

Counter Reset Bit, CRESET

When the counter reset bit CRESET is set from a logic low to a logic high, the frame counter, FC, and quarter bit counter (QBC) are reset to 0. The CRESET bit self-resets to 0, one 13 MHz clock cycle after the logic low to logic high transition has been synchronized to the AT&T CSP1088 internal clock. Resetting the CRESET bit to a logic low does not affect the frame counter or quarter bit counter.

INCR/DECR

The INCR and DECR bits, embedded in the TCNTRL register, adjust the QBC clock by 1/8 symbol. Each logic high write to INCR causes the QBC counter to advance by 1/8 of a symbol time; a logic low write to INCR has no affect on the QBC clock. Each logic high write to DECR causes the QBC counter to delay by 1/8 of a symbol time; a logic low write to DECR has no affect on the QBC clock.

Note that back-to-back writes of the INCR/DECR bits (to quickly increment or delay the QBC counter) need to be separated by two NOPs if the DSP is running at higher than 26 MIPS. For a DSP running at 26 MIPS or lower, back-to-back writes need not be separated by NOPs. (Due to the asynchronous DSP-CSP interface.)

Timer Clock Enable Bit, TIMECLK

When the timer clock enable bit, TIMECLK, is set to a logic high, the clock to the quarter-bit counter is enabled. When reset to a logic low, the clock to the quarter-bit counter is disabled.

ETCI Increment Control Bit, INCQBCFC

When the ETCI increment control bit, INCQBCFC, is set to a logic high, the ETCI increments when both a quarter bit timing match occurs and the criteria defined by the current ETC register's EVEN/ODD bits are met. When reset to a logic low, the ETCI increments only when a quarter bit timing match occurs.

Event Timing and Control Index Register, ETCI (Address 0xB)

The event timing and control index register, ETCI, points to one of 15 event timing and control registers, ETC[14:0]. See page 7, under Event Timing and Control State Machine, for ETCI increment criteria. The ETCI counter is programmable, and the depth that the ETCI counter counts to before resetting to 0 is set in the TCNTRL register.

Event Timing and Control Registers, ETC[14:0] (Address 0x10—0x3C)

There are 15 event timing and control registers, each containing three 16-bit words, ETC0[14:0], ETC1[0:14], and ETC2[14:0]. The ETCI index counter points to which one (if any) of the 15 ETC registers is active. When the timing portion of the indexed register matches the quarter-bit counter, QBC, and the EVEN and ODD bit criteria are met, then the control portion of the indexed ETC register is executed. The ETCI counter is automatically incremented to point to the next ETC register.

Table 19. Event Timing and Control Index Register ETCI

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	X	X	X	X	X	X	X	X	X	X	X	X	ETCI 3	ETCI 2	ETCI 1	ETCI 0

Register Information (continued)

Event Timing and Control Registers, ETC[14:0] (Address 0x10—0x3C) (continued)

Table 20. Event Timing and Control Word 0, ETC0[0:14] Bit Definition

Bit #	7	6	5	4	3	2	1	0
Label	EQN 7	EQN 6	EQN 5	EQN 4	EQN 3	EQN 2	EQN 1	EQN 0
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Label	DSPI	ODD	EVEN	EQN 12	EQN 11	EQN 10	EQN 9	EQN 8

Table 21. Event Timing and Control Word 1, ETC1[14:0] Bit Definition

Bit #	7	6	5	4	3	2	1	0
Label	BOE	BIE	EFN 5	EFN 4	EFN 3	EFN 2	EFN 1	EFN 0
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Label	r	BIG 3	BIG 2	BIG 1	BIG 0	FR 2	FR 1	FR 0

Table 22. Event Timing and Control Word 2, ETC2[14:0] Bit Definition

Bit #	7	6	5	4	3	2	1	0
Label	OCTL 7	OCTL 6	OCTL 5	OCTL 4	OCTL 3	OCTL 2	OCTL 1	OCTL 0
Bit #	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Label	BL 1	BL 0	OCTL 13	OCTL 12	OCTL 11	OCTL 10	OCTL 9	OCTL 8

Event Quarter-Bit Number, EQN[12:0] (Bits 12:0 of ETC0[14:0] registers)

The quarter-bit counter must match this portion of the indexed ETC register for any time match to occur. EQN[12:0] values greater than 4999 are valid, but a time match will never occur because the QBC value cannot be greater than 4999.

EVEN and ODD Bits

Table 23. EVEN and ODD Bit Definition

EVEN	ODD	Description
0	0	Match on frame indicated by EFN bits
0	1	Match on ODD frames only
1	0	Match on EVEN frames only
1	1	Match on all frames

During normal full-rate transmission, the EVEN and ODD bits are usually set to logic high, and a timing match can occur on any frame.

Register Information (continued)

Event Timing and Control Registers, ETC[14:0] (Address 0x10—0x3C) (continued)

Typically used in half-rate transmission, if the ODD bit only is set to a logic high, then a timing match can occur on all odd-numbered frames.

Typically used in half-rate transmission, if the EVEN bit only is set to a logic high, then a timing match can occur on all even-numbered frames.

If both ODD and EVEN bits are set to a logic low, the frame number must match the EFN[5:0] bits for a timing match to occur.

DSP Interrupt (DSPI) Bit (Bit 15 of ETCO[14:0] Registers)

When a timing match occurs and this bit is set to a logic high, a time-out interrupt is issued, and the TIMEI bit of the interrupt status register, INS, is set to a logic high. Additionally, if the Clock Output buffer was disabled, this time-out interrupt enables the Clock Output with the previously selected frequency.

Event Frame Number (EFN[5:0]) Bits

When the EVEN and ODD bits of the indexed ETC register are reset to a logic low, the frame number counter must match this portion of the indexed ETC register for a timing match to occur. The quarter-bit counter must also match the number in the EQN[12:0] bits.

Baseband Input Enable (BIE) Bit

When the baseband input enable bit is set to a logic high, the baseband input section is first initialized to correct the dc offset voltages of the programmable-gain amplifier, the antialiasing filter, and the dc offset of the external transceiver amplifier. After the initialization, the RxI and RxQ A/D converters begin converting the baseband input. The time delay from when the BIE bit is set to when the first RxI or RxQ sample is written into the double buffer is 144 symbol times (531.7 μs).

After 16 samples of RxI and RxQ each are written into the first half of the double-buffered register, an interrupt is issued, and the RXBUFI bit of the interrupt status register, INS, is set to a logic high. The 16 RxI and 16 RxQ samples must be read before the other half of the double buffer is filled (which takes about 59 μs). Normally, this process continues until ten interrupts have been issued (that is, until 160 bits have been received).

If the burst length bits BL[1] and BL[0] are both set to a logic high, then the sampling and buffering process will continue until the STOP bit of the TEST register is set to logic high.

Baseband Output Enable (BOE)

When the baseband output enable, BOE, bit is set to a logic high, there is a delay of 56 quarter-bit cycles before the power ramp at the TXP output starts (see start in Figure 9). 2.5 symbols after this start, the modulator begins sending a preamble. The delay from setting the BOE bit to the start of the preamble is 66 quarter-bit cycles. After the 4-bit preamble, the modulator begins sending the data stored in the burst data registers, BRSTDATA[9:0]. The BRSTDATA registers must be completely loaded before the preamble starts.

Register Information (continued)

Event Timing and Control Registers, ETC[14:0] (Address 0x10—0x3C) (continued)

Frequency Register (FR[5:0]) Bits

The frequency register bits select which one, if any, of the six frequency selection registers, FREQ[5:0], is used to program the external frequency synthesizer via the serial output section. The timing and control register, TCNTRL, sets the output length, rate, and direction of the serial output.

Table 24. Description of Frequency Register Bits, FR[2:0]

FR[2]	FR[1]	FR[0]	Description
0	0	0	No serial output
0	0	1	Use Frequency Selection Register FREQ[0]
0	1	0	Use Frequency Selection Register FREQ[1]
0	1	1	Use Frequency Selection Register FREQ[2]
1	0	0	Use Frequency Selection Register FREQ[3]
1	0	1	Use Frequency Selection Register FREQ[4]
1	1	0	Use Frequency Selection Register FREQ[5]
1	1	1	No serial output

Baseband Input Gain (BIG[3:0]) Bits

The four baseband input gain bits define the baseband input gain in 2 dB steps ranging from 0 dB gain to 18 dB gain. BIG[0] is the LSB, and BIG[3] is the MSB.

Table 25. Description of Baseband Input Gain Bits, BIG[3:0]

BIG[3]	BIG[2]	BIG[1]	BIG[0]	Gain
0	0	0	0	0 dB
0	0	0	1	2 dB
0	0	1	0	4 dB
0	0	1	1	6 dB
0	1	0	0	8 dB
0	1	0	1	10 dB
0	1	1	0	12 dB
0	1	1	1	14 dB
1	0	0	0	16 dB
1	0	0	1	18 dB
1	0	1	0	reserved
1	0	1	1	reserved
1	1	0	0	reserved
1	1	0	1	reserved
1	1	1	0	reserved
1	1	1	1	reserved

Register Information (continued)

Event Timing and Control Registers, ETC[14:0] (Address 0x10—0x3C) (continued)

External Control (OCTL[13:0]) Bits

The external control OCTL[13:0] bits set the values to the output control pins, OCTL[13:0]. These 14 outputs can be used to control external components such as powering on/off the external transceiver amplifiers or frequency synthesizer.

Burst Length (BL[1:0]) Bits

Table 26. Burst Length Bit Definition

BL 1	BL 0	Description
0	0	No transmit or receive
0	1	Transmit normal burst (148 bits) Receive normal burst (160 bits)
1	0	Transmit access burst (88 bits) Receive normal burst (160 bits)
1	1	Continuous transmit if BOE is set Continuous receive if BIE is set

Frequency Selection Registers, FREQ[5:0] (Address 0x40—0x4B)

The frequency selection registers, FREQ[5:0], can be used to program an external frequency synthesizer via the serial output pins, SERCK, SERDA, and SERLE. The output can be either 8 bits, 16 bits, or 24 bits long. Because the output can be as long as 24 bits, each register uses two 16-bit words, FREQW0[5:0] and FREQW1[5:0]. Word FREQW0 will be the lower address in a frequency register. The event timing and control word 1 selects which one of the six FREQ[5:0] registers is used.

The timing and control register, TCNTRL, controls whether the output is 8 bits, 16 bits, or 24 bits, whether the output rate is 1.08 Mbits/s or 0.54 Mbits/s, and whether the output is written from LSB to MSB or from MSB to LSB.

Table 27. Frequency Selection Word 1 (Lower Address), FREQW0[5:0] Bit Definition

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	FS 15	FS 14	FS 13	FS 12	FS 11	FS 10	FS 9	FS 8	FS 7	FS 6	FS 5	FS 4	FS 3	FS 2	FS 1	FS 0

Table 28. Frequency Selection Word 2 (Upper Address), FREQW1[5:0] Bit Definition

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	X	X	X	X	X	X	X	X	FS 23	FS 22	FS 21	FS 20	FS 19	FS 18	FS 17	FS 16

Register Information (continued)

Frequency Selection Registers, FREQ[5:0] (Address 0x40—0x4B) (continued)

Table 29. Frequency Selection Word Addresses

Frequency Selection Register	Frequency Selection Word	Address (hex)
FREQ[0]	FREQW0[0]	0x40
	FREQW1[0]	0x41
FREQ[1]	FREQW0[1]	0x42
	FREQW1[1]	0x43
FREQ[2]	FREQW0[2]	0x44
	FREQW1[2]	0x45
FREQ[3]	FREQW0[3]	0x46
	FREQW1[3]	0x47
FREQ[4]	FREQW0[4]	0x48
	FREQW1[4]	0x49
FREQ[5]	FREQW0[5]	0x4A
	FREQW1[5]	0x4B

Table 30. Burst Data Bit Locations

Memory Addresses	MSB	Middle Bits													LSB
BRSTDATA[0]	Bit 15	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 0
BRSTDATA[1]	Bit 31	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 16
BRSTDATA[2]	Bit 47	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 32
BRSTDATA[3]	Bit 63	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 48
BRSTDATA[4]	Bit 79	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 64
BRSTDATA[5]	Bit 95	—	—	—	—	—	—	—	87	—	—	—	—	—	Bit 80
BRSTDATA[6]	Bit 111	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 96
BRSTDATA[7]	Bit 127	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 112
BRSTDATA(8)	Bit 143	—	—	—	—	—	—	—	—	—	—	—	—	—	Bit 128
BRSTDATA[9]	Bit 159	—	—	—	—	—	—	—	—	—	—	Bit 147	Bit 146	Bit 145	Bit 144

Burst Data Registers, BRSTDATA[9:0] (Address 0x50—0x59)

The burst data registers store up to 160 bits of data in ten 16-bit registers. Data has to be already loaded into these registers before the start of a burst. The burst data is transmitted in ascending order starting with bit 0. The length of the burst is either 88 bits for an access burst or 148 bits for a normal burst. Which burst length is used is set by the burst length bits, BL[1:0], of the event timing and control word 2, ETCW2. When the burst length bits, BL[1:0], select the continuous mode, all 160 bits are transmitted repeatedly in a cyclic manner.

Ciphering

The burst data registers also serve to support the A5 ciphering.

The AT&T CSP1088 generates, through mask options and software interface, the cipher blocks A5.1 and A5.2. To generate the BLOCK 1 and BLOCK 2 ciphers, write Kc, the key bits, and Count, and the TDMA frame number, into the BRSTDATA registers (see Table 32 on page 30); start BLOCK 1 generation by using the control register; read the BLOCK 1 cipher from the BRSTDATA registers; start BLOCK 2 generation by using the CONTROL register; and read the BLOCK 2 cipher from the BRSTDATA. The block generation function uses the BRSTDATA buffer to store each block as it is generated. Thus, the A5 block generation must be used prior to loading the transmit burst data. The A5 status may be polled in the CONTROL register, or an interrupt can be enabled by the INS and INC registers. When enabled, it takes approximately 350 13 MHz cycles to generate BLOCK 1 data. When BLOCK 2 is enabled, it takes approximately 150 13 MHz cycles to generate BLOCK 2 data.

Register Information (continued)

Ciphering (continued)

Table 31. A5 Kc Data Bit Definition for A5DIR=0

Register Word	Register Bit #															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BRSTDATA1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
BRSTDATA2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
BRSTDATA3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63

Table 32. A5 Count Data Bit Definition for A5DIR = 0

Register Word	Register Bit #															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA4	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BRSTDATA5	16	17	18	19	20	21	r	r	r	r	r	r	r	r	r	r

Table 33. A5 Kc Data Bit Definition for A5DIR = 1

Register Word	Register Bit #															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BRSTDATA2	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
BRSTDATA3	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48

Table 34. A5 Count Data Bit Definition for A5DIR = 1

Register Word	Register Bit #															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA4	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA5	r	r	r	r	r	r	r	r	r	r	21	20	19	18	17	16

Note: r = reserved, must be zero.

Register Information (continued)

Ciphering (continued)

Table 35. BLOCK 1 and BLOCK 2 Data Bit Definition for A5DIR = 0

Register Word	Register Bit #															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
BRSTDATA3	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
BRSTDATA4	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
BRSTDATA5	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
BRSTDATA6	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
BRSTDATA7	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
BRSTDATA8	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
BRSTDATA9	112	113	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Table 36. BLOCK 1 and BLOCK 2 Data Bit Definition for A5DIR = 1

Register Word	Register Bit #															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BRSTDATA3	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BRSTDATA4	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
BRSTDATA5	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
BRSTDATA6	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
BRSTDATA7	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
BRSTDATA8	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
BRSTDATA9	r	r	r	r	r	r	r	r	r	r	r	r	r	r	113	112

Frequency Correction Register, FCR (Address 0x5A)

The AT&T CSP1088's modulation section uses the contents of the frequency correction register, FCR, to compensate for broadcast frequency deviations of the mobile. It accomplishes this by modifying the effective frequency of the transmitted data. The DSP should calculate the difference between the base station frequency and that of the mobile from the received data stream, and then write the difference into the FCR prior to the next transmit burst.

The frequency correction word is a 13-bit, 2's complement number. The MSB is equal to π radians, and the LSB is equal to $\pi / 2^{12}$ radians per symbol. Also, the LSB is equal to 270,833.33 divided by 2^{13}, or 33.06 Hz. When writing the FCR, 13-bit values should be sign-extended to 16 bits.

Register Information (continued)

Frequency Correction Register, FCR (Address 0x5A) (continued)

Table 37. Frequency Correction Register Bit Definition

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	FCR 12	FCR 12	FCR 12	FCR 12	FCR 11	FCR 10	FCR 9	FCR 8	FCR 7	FCR 6	FCR 5	FCR 4	FCR 3	FCR 2	FCR 1	FCR 0

Ramp Level Register, RAMPLVL (Address 0x5F)

The function of the transmit power level output, TXP, is to turn on and turn off the output of the power amplifier with a controlled waveshape that limits the frequency spectrum spreading caused by burst modulation. The ramp level register, RAMPLVL, sets the amplitude of TXP during the burst. When TXP is first enabled, its dc level will start at about 0.5 V. From there, TXP can ramp up to as much as 2.25 V, which is full scale. The output level is generated by a 9-bit D/A converter (0—511).

Table 38. Ramp Level Register, RAMPLVL, Bit Definitions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	X	X	X	X	X	X	X	RL 8	RL 7	RL 6	RL 5	RL 4	RL 3	RL 2	RL 1	RL 0

Ramp Up and Ramp Down Levels Registers, RAMPUP[15:0] (Address 0x60—0x6F); RAMPDN[15:0] (Address 0xE0—0xEF)

The function of the transmit power level output, TXP, is to turn on and turn off the output of the power amplifier with a controlled waveshape that limits the frequency spectrum spreading caused by burst modulation. During the first symbol intervals during ramp up, the magnitude of TXP is incremented to the values held in RAMPUP[0] through RAMPUP[15], sequentially, then from RAMPUP[15] to RAMPLVL. When TXP is first enabled, its dc level will start at about 0.5 V. From there, TXP can ramp up to as much as 2.25 V, which is full scale. The output level is generated by a 9-bit unsigned integer (0—511) D/A converter. After the ramp up interval, the output level is set by the contents of the ramp level register, RAMPLVL. The ramp down sequence is a mirror image of the ramp up sequence, and uses the values held in the RAMPDN[0] through RAMPDN[15] registers.

When the transmitter is operating in the continuous mode (burst length bits BL[1:0] = 0x3), the output level of TXP after the ramp up interval and before the ramp down interval, can be modified by writing the value of the desired output to RAMPLVL.

Table 39. Ramp Up and Ramp Down Levels Registers, RAMPUP[15:0] and RAMPDN[15:0] Bit Definitions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	X	X	X	X	X	X	X	RM 8	RM 7	RM 6	RM 5	RM 4	RM 3	RM 2	RM 1	RM 0

Double-Buffered, 32-Sample I & Q Registers, RXBUFF[31:0] (Address 0x70—0x8F)

RXBUFF[31:0] is a double-buffered, 32-sample register that stores I & Q sample pairs. After a group of 16 I & Q sample pairs fills the first half of the double buffer, an RXBUFI interrupt is issued. The data in the buffer needs to be read within 59 µs, before the other half of the buffer fills and issues the next RXBUFI interrupt.

Register Information (continued)

Double-Buffered, 32-Sample I & Q Registers, RXBUFF[31:0] (Address 0x70—0x8F) (continued)

Each sample is a 10-bit, 2's complement word that is sign extended to provide a 16-bit 2's complement representation.

For a normal burst receive mode, the read process will continue until 10 groups of 16 sample pairs have been collected. The normal burst receive mode is set by the burst length bits BL[1:0] of the event timing and control word 2 (ETCW2). The DSP has approximately 59 µs to read each buffer of 16 I/Q samples sample pairs.

The first I-Q sample is written into the lowest addresses RXBUFF[0] and RXBUFF[1], and successive samples are written into succeeding higher addresses. The sixteenth and final sample pair is written into the highest addresses RXBUFF[30], and RXBUFF[31]. When the RBORD bit of the CONTROL register is set to a logic low, the sample pairs are read in first I and then Q. When RBORD is set to a logic high, the sample pairs are read in first Q and then I.

Table 40. RXBUFF Bit Definition

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Label	IQ 9	IQ 9	IQ 9	IQ 9	IQ 9	IQ 9	IQ 9	IQ 8	IQ 7	IQ 6	IQ 5	IQ 4	IQ 3	IQ 2	IQ 1	IQ 0

Register Information (continued)

Double-Buffered, 32-Sample I & Q Registers, RXBUFF[31:0] (Address 0x70—0x8F) (continued)

Table 41. RXBUFF I/Q Sample Locations

RXBUFF Register Address	Contents of Registers when RBORD = Low	Contents of Registers when RBORD = High
RXBUFF[0]	I0	Q0
RXBUFF[1]	Q0	I0
RXBUFF[2]	I1	Q1
RXBUFF[3]	Q1	I1
RXBUFF[4]	I2	Q2
RXBUFF[5]	Q2	I2
RXBUFF[6]	I3	Q3
RXBUFF[7]	Q3	I3
RXBUFF[8]	I4	Q4
RXBUFF[9]	Q4	I4
RXBUFF[10]	I5	Q5
RXBUFF[11]	Q5	I5
RXBUFF[12]	I6	Q6
RXBUFF[13]	Q6	I6
RXBUFF[14]	I7	Q7
RXBUFF[15]	Q7	I7
RXBUFF[16]	I8	Q8
RXBUFF[17]	Q8	I8
RXBUFF[18]	I9	Q9
RXBUFF[19]	Q9	I9
RXBUFF[20]	I10	Q10
RXBUFF[21]	Q10	I10
RXBUFF[22]	I11	Q11
RXBUFF[23]	Q11	I11
RXBUFF[24]	I12	Q12
RXBUFF[25]	Q12	I12
RXBUFF[26]	I13	Q13
RXBUFF[27]	Q13	I13
RXBUFF[28]	I14	Q15
RXBUFF[29]	Q14	I14
RXBUFF[30]	I15	Q15
RXBUFF[31]	Q15	I15

Register Information (continued)

Clock Output Control, CLKOCNTL (Address 0x90)

The clock output takes the internal 13 MHz clock and provides a variety of clock output options with which to drive a companion DSP16XX device. After reset, the contents of this register are 0.

Table 42. PLL Register Bit Definitions

Name	Bit #	Description
PLLENBL	0	PLL enable
r	1	Reserved, reset to 0
r	2	Reserved, set to 1
r	3	Reserved, reset to 0
r	4	Reserved, set to 1
PCNTL[1:0]	6—5	PLL control
r	9—7	Reserved, reset to 0
PFBDIV[4:0]	14—10	PLL feedback divide ratio
PLLACQ	15	PLL acquire (lock) status

PLL Enable (PLLENBL) Bit

When set to logic high, PLLENBL activates the PLL. The PLL requires a finite time (see PLLACQ) to lock to the final frequency, determined by the PFBDIV[4:0] bits. When locked, PLLACQ will set to logic high. The CLKO output will not switch to the PLL frequency until PLLACQ is logic high. When set to logic low, PLLENBL turns off the PLL if it was on, or does not affect operation if this bit was previously low.

PLL Control (PCNTL[1:0])Bits

Table 43. PCNTL[1:0] Bit Definition

PCNTL1	PCNTL0	Output Frequency, MHz
0	0	13 MHz (no PLL required)
0	1	13 MHz (no PLL required)
1	0	PLL frequency determined by PFBDIV[4:0]
1	1	CLKO, output disabled (D.C.)

When selecting the PLL output, PCNTL1:PCNTL0 = 1:0, the output frequency will not change to the new PLL frequency until PLLACQ is logic high. Therefore, if PLLENBL is not set logic high, the CLKO outputs will remain at the prior frequency. For example, writing the words 0xXX14 then 0xXX55 in sequence will first make the output 13 MHz; the second word starts the PLL and after the PLL has acquired (see PLLACQ for time delay) the output will change to the frequency programmed by PFBDIV[4:0].

When selecting CLKO output disabled, the CLKO and the CLKOREF pins both become about equal to Vss independent of all other settings in this register. When the DSP then writes to PCNTL[1:0] other than PCNTL1:PCNTL0 = 1:1, the new mode is activated. If the TIMEI interrupt asserts any time that PCNTL1:PCNTL0 = 1:1, then the CLKO outputs are activated to the setting prior to entering the CLKO output disable mode. Thus, the DSP must set CLKO to the desired wakeup setting prior to disabling CLKO if the TIMEI interrupt will be used to wake up CLKO and CLKOREF.

Example:To generate a 26 MHz output clock:

CLKOCNTL = 0x3c55

PLL Feedback Divide (FBDIV[4:0]) Bits

The PLL feedback divide ratio, M, is set by the PFBDIV[4:0] bits. The CLKO output frequency is given as Fclko = 13*(M+1)/8, where M denotes the decimal value of PFBDIV[4:0], M = 8 through 31. M = 0 through M = 7 is a reserved state.

PLL Acquire Status (PLLACQ) Bit

The PLL acquisition, or lock status is indicated in the PLLACQ bit. Reading a logic low from PLLACQ indicates that the PLL is not locked or is off. Reading a logic high from PLLACQ indicates that the PLL is on and the output frequency is phase-locked. The time from PLL enabled to PLL lock is 315 µs. **Only a logic low write to this bit is allowed.**

Baseband Input Section

Figure 9 shows a block diagram of the baseband input section. The baseband input section has an I channel and a Q channel, each channel with a 10-bit A/D converter. As incoming I and Q samples are converted, the samples are stored in an internal 32-register double buffer. After 16 I and 16 Q sample pairs are stored in the first half of the double buffer, the AT&T CSP1088 issues an interrupt and continues storing I and Q samples in the other half of the double buffer. The DSP has about 59 µs to read the data out of the first half of the buffer before the next 16 sample pairs are received.

The RF demodulator and the baseband receive channel have dc offsets that vary with AGC and PGA gain setting. Before the start of each receive burst, the dc offset for both the RF demodulator and the baseband receive channels are stored in the baseband channel.

The offsets that are stored during this offset storage cycle are used to cancel the dc offset present in the channel during burst reception. The dc offset storage takes approximately 450 µs. The stored dc offset decays at a rate specified in Table 54. Since the offsets in the receive channel (RF+ baseband) change with gain setting and the stored offsets decay over time, the offset storage cycle must be repeated prior to every burst.

In addition to the dc offset correction cycle that occurs with each burst, a one time digital dc offset calibration must be done before using the baseband receive channel. This calibration corrects the A/D offset. The RXDC-CAL bit in the control register must be set once after powerup to complete this calibration.

The input section has a programmable gain amplifier, PGA, whose gain can be varied from 0 dB to +18 dB in 2 dB steps. When the PGA is set to 0 dB, the full-scale input is 1 $V_{peak\text{-}peak}$ differential.

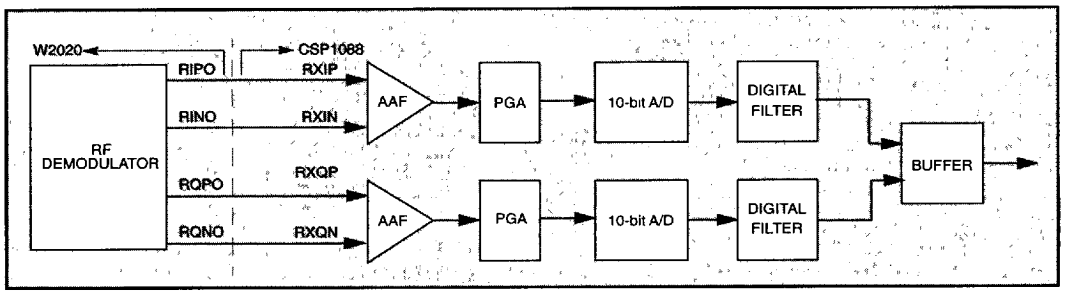


Figure 9. Block Diagram Showing the Baseband Input Section

The input A/D converter uses three external references during the conversion process: VADP, VADN, and VADCM. Each reference must be connected to a 1.0 µF ceramic bypass capacitor as shown in Figure 11. These capacitors should be located as close as practical to the pin. Before using or calibrating the receive channel, the first time after powering up the CSP1088, the receiver should be turned on for a minimum of 7.0 ms to charge these capacitors.

A timing diagram for the receive channel is shown in Figure 10. It illustrates the timing for a 148 (160) bit burst. RF dc offset correction is performed for the first 130 symbol times.

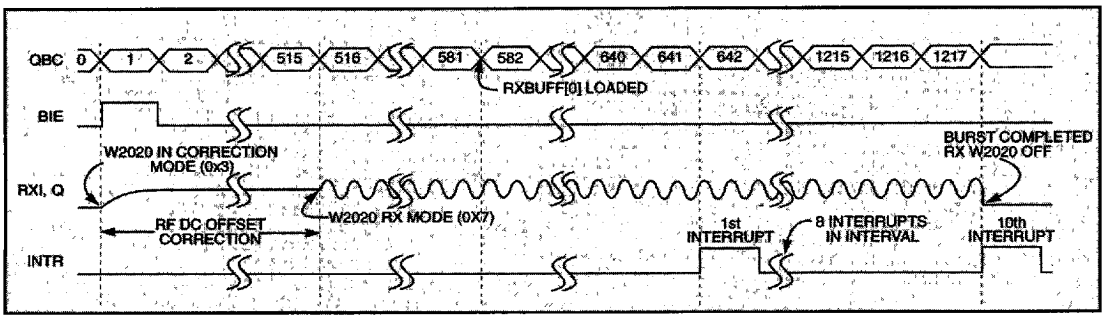


Figure 10. Baseband Input Timing Diagram

Baseband Input Section (continued)

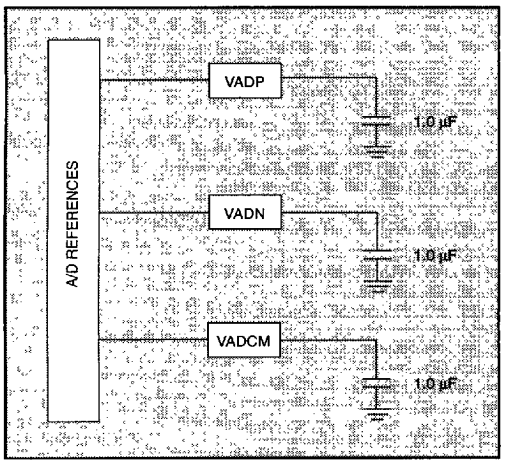


Figure 11. External Reference Connection

Baseband Output and GMSK Modulation

Figure 12 shows a block diagram of the baseband output section of the AT&T CSP1088. The baseband output consists of 1) a transmit buffer, BRSTDATA, that holds up to 160 bits of data, 2) a GMSK modulator section that modulates the data to GSM specifications, 3) D/A converters and filters to convert the modulated data into analog output signals, and 4) a power ramp output, TXP, which is used to ramp on and off the power amplifier with a well-controlled waveform.

When one of the event timing and control registers, ETC[14:0], sets the baseband output enable bit, BOE, to a logic high, it activates the baseband output section which performs a dc offset calibration prior to initiating a burst. For a normal burst, 148 bits of data from the burst data registers, BRSTDATA[9:0], are sent to the modulator section, and for an access burst, 88 bits of data are sent. The continuous cycle mode, which is used primarily for testing, cycles all 160 bits of data from the BRSTDATA[9:0] registers in a continuous loop until the STOP bit in the test register is set to a logic high.

The modulator adds four preamble bits, all 1s, and four postamble bits, also all 1s, to the data, and then differentially encodes the data stream before GMSK modulating it. The tables below show the differentially encoded data streams for normal, access, and continuous cycle modes.

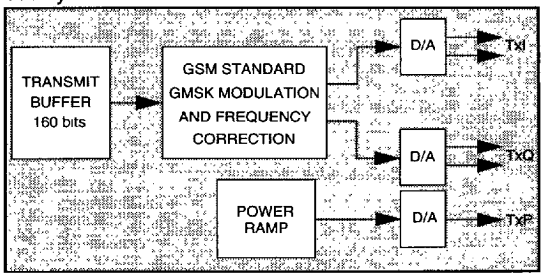


Figure 12. Baseband Output Block Diagram

Table 44. Normal Burst Differentially Encoded Data (B0—B147)

1 ⊕ 1	1 ⊕ 1	1 ⊕ 1	1 ⊕ 1	B0 ⊕ 1	B1 ⊕ B0	B2 ⊕ B1	B3 ⊕ B2	•	•	• ...	
... •	•	•	B146 ⊕ B145	B147 ⊕ B146	1 ⊕ B147	1 ⊕ 1	1 ⊕ 1	1 ⊕ 1			

Table 45. Access Burst Differentially Encoded Data (B0—B87)

1 ⊕ 1	1 ⊕ 1	1 ⊕ 1	1 ⊕ 1	B0 ⊕ 1	B1 ⊕ B0	B2 ⊕ B1	B3 ⊕ B2	•	•	• ...	
... •	•	•	B86 ⊕ B85	B87 ⊕ B86	1 ⊕ B87	1 ⊕ 1	1 ⊕ 1	1 ⊕ 1			

Table 46. Continuously Cycled Encoded Data (B0—B159)

1 ⊕ 1	1 ⊕ 1	1 ⊕ 1	1 ⊕ 1	B0 ⊕ 1	B1 ⊕ B0	B2 ⊕ B1	B3 ⊕ B2	•	•	• ...	
... •	•	•	B158 ⊕ B157	B159 ⊕ B158	B0 ⊕ B159	B1 ⊕ B0	•	•	• ...		
... •	•	•	Bn ⊕ Bn-1	1 ⊕ Bn	1 ⊕ 1	1 ⊕ 1	1 ⊕ 1				

Baseband Output and GMSK Modulation (continued)

Modulator Section

Figure 13 shows a block diagram of the modulator section. Data from the BRSTDATA[9:0] registers (B0, B1, B2, . . .) are differentially encoded with an exclusive OR function. After that, the data are GMSK modulated to GSM standards. The output of the GMSK modulator is phase angle, and to this phase angle, a frequency correction term is added from the frequency correction accumulator. The values of the I and Q outputs are generated from the phase angle. If the MODROT bit of the CONTROL register is set to a logic high, then the rotation of the output is reversed from the normal counterclockwise rotation to a clockwise rotation.

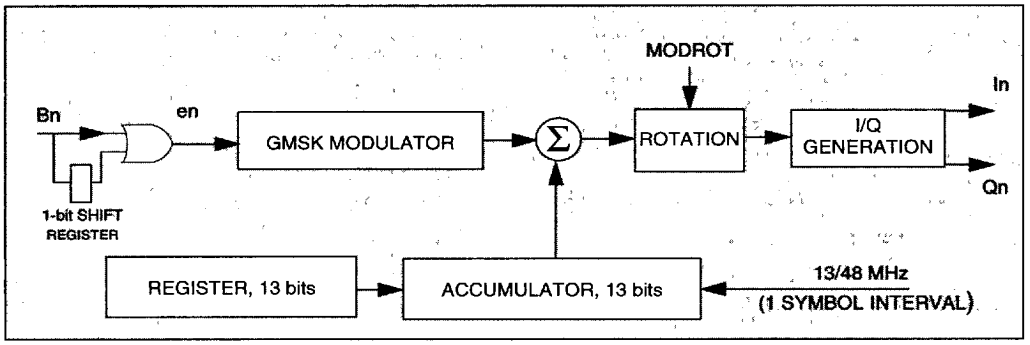


Figure 13. GMSK Modulator Block Diagram

Frequency Correction

The mobile corrects its output frequency by adding a correction phase to each output symbol. For example, if a correction of 0.1° is added to the first symbol, then 0.2° is added to the second symbol, 0.3° to the third symbol, and so on. With the symbols being broadcast at about 270.8 Kbits/s, advancing the phase 0.1° at each symbol increases the output frequency by about 75 Hz.

The difference between the base station's reference frequency and the mobile's reference can be calculated from the received burst by the DSP. The difference can include frequency shifts due to the mobile moving, such as if the mobile is in a moving car. When the DSP calculates the difference, it can load a correction phase into the frequency correction register, FCR. This register is 13 bits wide and is scaled to 360°. Therefore, one LSB is $360°/2^{13}$ or approximately 43.945×10^{-3}, which at 270.8 Kbits/s represents about 33.06 Hz of frequency correction.

The frequency correction accumulator, FCA, adds the contents of the frequency correction register to itself at every symbol interval. The accumulator contains the net phase correction for each symbol and is added to the modulator output. Because the accumulator is scaled to 360°, it is cyclic and overflow can be ignored.

Baseband Output and GMSK Modulation (continued)

Output Timing and Power Ramp

The function of the transmit power level output, TXP, is to turn on and turn off the output of the power amplifier with a controlled waveshape that limits the frequency spectrum spreading caused by burst modulation.

Figure 14 shows the timing of the power ramp relative to the output symbols. The shape of the power ramp is controlled by the values held in the registers RAMPUP[15:0] and RAMPDN[15:0]. The values from RAMPUP[15:0] load sequentially into the 9-bit ramping control at one half the symbol rate. These values are interpolated once to provide four values per symbol; the values inserted between programmed values is the linear interpolation between any two. The value in RAMPLVL register sets the final D.C. level for the normal part of the burst. Note that the time 0 in Figure 14 is 56 quarter bit counts after BOE went active.

See Figure 14 for a detailed description of the ramp timing. The 4 bits of preamble are modulated during the powerup ramp, where the start of the TXI and TXQ-modulation for m0 corresponds to the TxP D/A converter having the value of RAMPUP[5].

The values held in the registers RAMPDN[15:0] control the shape of the post modulation power. These values are loaded into the ramping control at one half the symbol rate, and are interpolated once, providing four values per symbol similarly to the ramp up sequence. Typically, the shape of the ramp down is programmed similarly to the ramp up.

Output Common Mode

Input pin TXVCM allows the user to change the common-mode voltage at the TXIP,N and TXQP,N outputs from its default value of 1.575 V. The common-mode voltage at these outputs is defined as (TXIP + TXIN)/2 and/or (TXQP + TXQN)/2. TXVCM has an input resistance range of 15 kΩ to 45 kΩ. Although this input voltage is filtered on chip, the user should supply a quiet, well-regulated voltage source to minimize noise on this pin. If TXVCM is unused, it should be unconnected. The acceptable input voltage range for TXVCM is shown in Table 56.

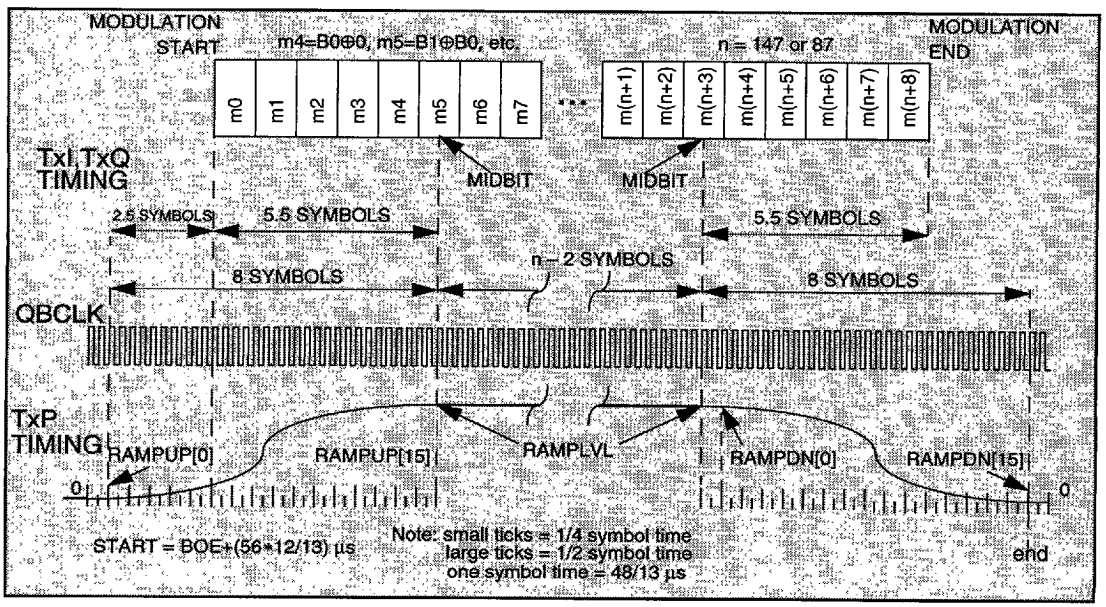


Figure 14. Power Ramp timing

Voiceband Input

Analog Input Section

Figure 15 shows a block diagram of the voiceband inputs to the A/D converter. The AT&T CSP1088 can switch between a microphone input, MICIN, and an auxiliary input AUXIN. The MICIN input is selected when the audio input select bit, AUDIS, of the AUDCONF register is reset to a logic low. The AUXIN input is selected when AUDIS is set to a logic high.

These two input amplifiers are standard, low-noise op amps with external feedback resistors so that the gain of the input stage can be matched to the sensitivity of the microphone. Their outputs are at full-scale when they are 88 mV_{rms}.

As an example, if the full-scale output of a microphone is 1 mV_{rms}, then the input amplifier should have a closed-loop gain of 88. One feedback resistor combination that gives a gain of 88 is R_f = 1 MΩ, and R_i = 11.4 kΩ, where R_i includes the source impedance. An electret microphone, for example, might have a source impedance of about 1.6 kΩ. In that case, the input resistor, R_i, would actually be 9.8 kΩ to set the gain at 88. The input capacitors (C_{I1}, C_{I2}) should be chosen such that $R_IC_I > 3.4$ µs.

Following the input stage and input multiplexer is the additional gain of 8 (about +18 dB), and a 4.0 kHz low-pass antialiasing filter. The output of the antialiasing filter is clamped at ± 1.0 V_{peak} to keep from overdriving the A/D converter which has a full-scale input of 707 mV_{rms}.

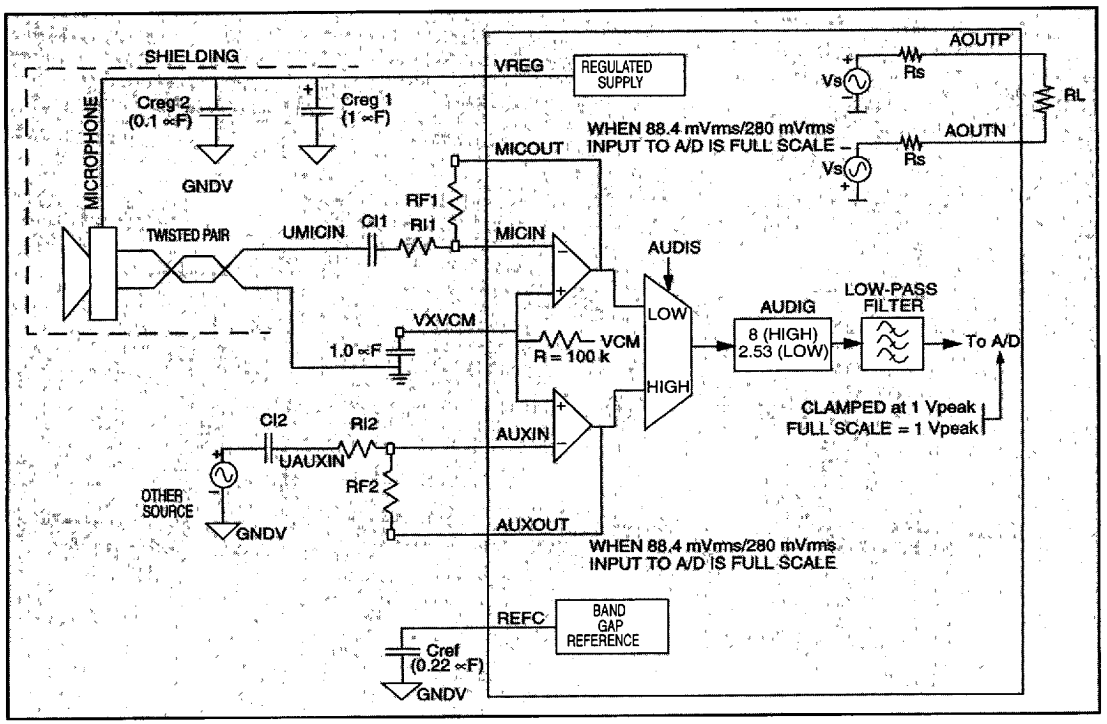


Figure 15. Analog External Configuration

Voiceband Input (continued)

Analog Input Section (continued)

The gain of the input section can be reduced –10 dB by setting the audio input gain bit, AUDIG, to a logic low. When AUDIG is set to a logic low, the internal gain is reduced from 8 to about 2.53.

The AT&T CSP1088 supplies a 3 V ± 10% reference to bias an electret condenser microphone. The output can supply at least 250 µA of current. VREG must be stabilized with external bypass capacitors, typically 0.1 µF and 40 µF, and has less than 100 µV of random noise (typically about 40 µV at room temperature) over the input frequency range. If the reference is not used, a stabilization capacitor must be connected, or the reference may oscillate.

REFC must be bypassed with a 0.22 µF capacitor and VXVCM with a 1.0 µF capacitor. Before activating the voiceband input section, the AUDCHR bit in the AUDCONF register must be set to logic high for 30 ms + 10 R_{ICI} time constants and then set to logic low. This charges all input nodes to the appropriate levels.

A/D Modulator and Digital Filters

The audio input A/D converter converts the incoming signal to 16-bit two's complement linear PCM words at an 8 kHz rate. Following the A/D converter, the signal is digitally filtered, both high-pass and low-pass. Because the filtering is done digitally, the filter response is invariant with processing.

Voiceband Output

The AT&T CSP1088 has a differential voiceband output, pins AOUTP and AOUTN, and with a full-scale PCM input, the output is 1.5 V_{RMS}. For load resistances less than 200 Ω, the full-scale output needs to be reduced using the AUDPGA register. (see Table 10 on page 20.)

The gain of the output stage can be adjusted from 0 dB to –45 dB in –3 dB steps. The audio output gain bits, AUDOG[3:0], of the AUDCONF register set the gain.

The audio output mute bit, AUDOM, of the AUDCONF register, when set to a logic low will mute the output. When data is not being outputted through the DIA, it is recommended that AUDOM = 0. The audio output enable bit, AUDOE, when reset to a logic low, will power down the output section altogether, and if AUDOE is set to a logic high, it will come on.

The AT&T CSP1088 has a dithering scheme which decorrelates the periodic quantization noise of the sigma-delta D/A converter to make it white noise. Without dithering, the low-level periodic noise due to the quantization noise of the sigma-delta converter can be objectionable. Dithering is enabled (the normal state) by resetting the audio output dithering bit, ADITH, of the AUDCONF register to a logic low. For applications other than audio, such as data communications, the dithering can be disabled by setting the ADITH bit to a logic high and the signal-to-noise ratio will be approximately 2 dB better.

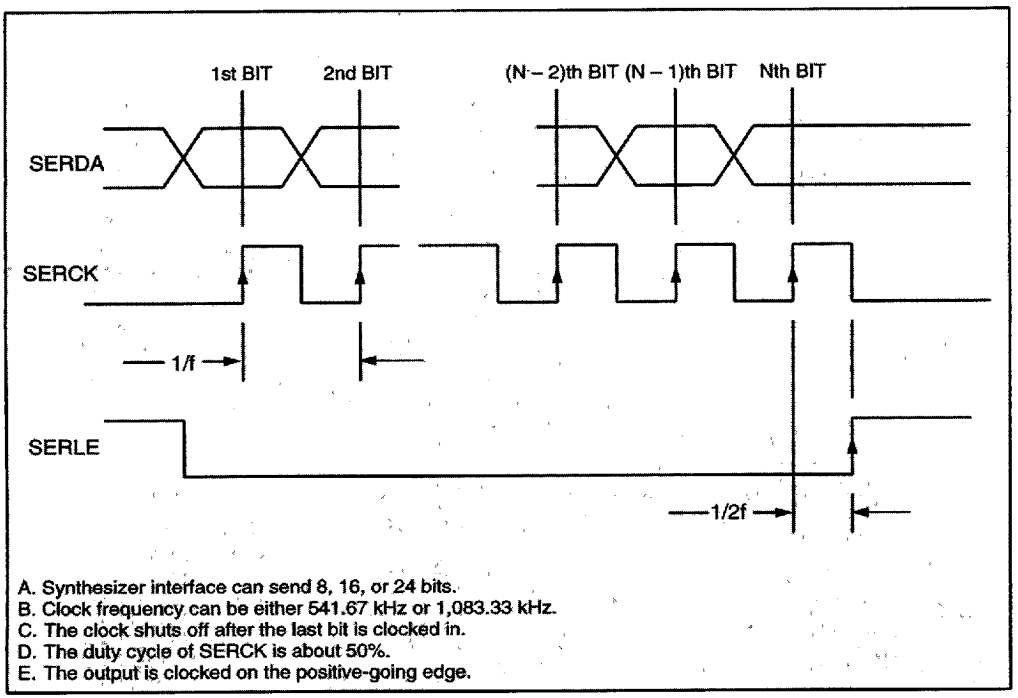
Programming an External RF Frequency Synthesizer

The AT&T CSP1088 has a serial output port for programming an external frequency synthesizer. The serial port has three output leads: SERDA (data), SERCK (clock), SERLE (latch enable). Figure 16 shows a timing diagram. The timing and control register, TCNTRL, controls whether the output is 8 bits, 16 bits, or 24 bits long, whether the output rate is 1.08 Mbits/s or 0.54 Mbits/s, and whether the output is from LSB to MSB or from MSB to LSB.

The DSP can load data into any of six frequency selection registers. Output is started whenever an event timing and control register selects the address of one of these six registers.

The timing diagram shows that the latch enable lead, SERLE, goes to a logic low at the start. One half cycle later, the SERCK output lead goes to a logic high which clocks the first data bit into the frequency synthesizer. The AT&T CSP1088 continues clocking data into the frequency synthesizer until all 8 bits, 16 bits, or 24 bits are sent. One half cycle later, the SERLE goes high which latches the data into the frequency synthesizer.

Programming an External RI Frequency Synthesizer (continued)



A. Synthesizer interface can send 8, 16, or 24 bits.
B. Clock frequency can be either 541.67 kHz or 1,083.33 kHz.
C. The clock shuts off after the last bit is clocked in.
D. The duty cycle of SERCK is about 50%.
E. The output is clocked on the positive-going edge.

Figure 16. Serial Port Timing Diagram

JTAG

The TAP controller is a 16-state sequential circuit which generates the control signals for the JTAG. The state assignments are defined by the standard and are shown in Figure 18. The TMS input increments the state machine and is latched on the rising edge of TCK.

The CSP1088 also contains a boundary-scan register for all digital I/O.

Boundary-Scan Conformance

All Boundary-Scan logic is verified for conformance to the 1149.1 standard by vectors generated by the conformance vector generator, *TAPDANCE* ®.

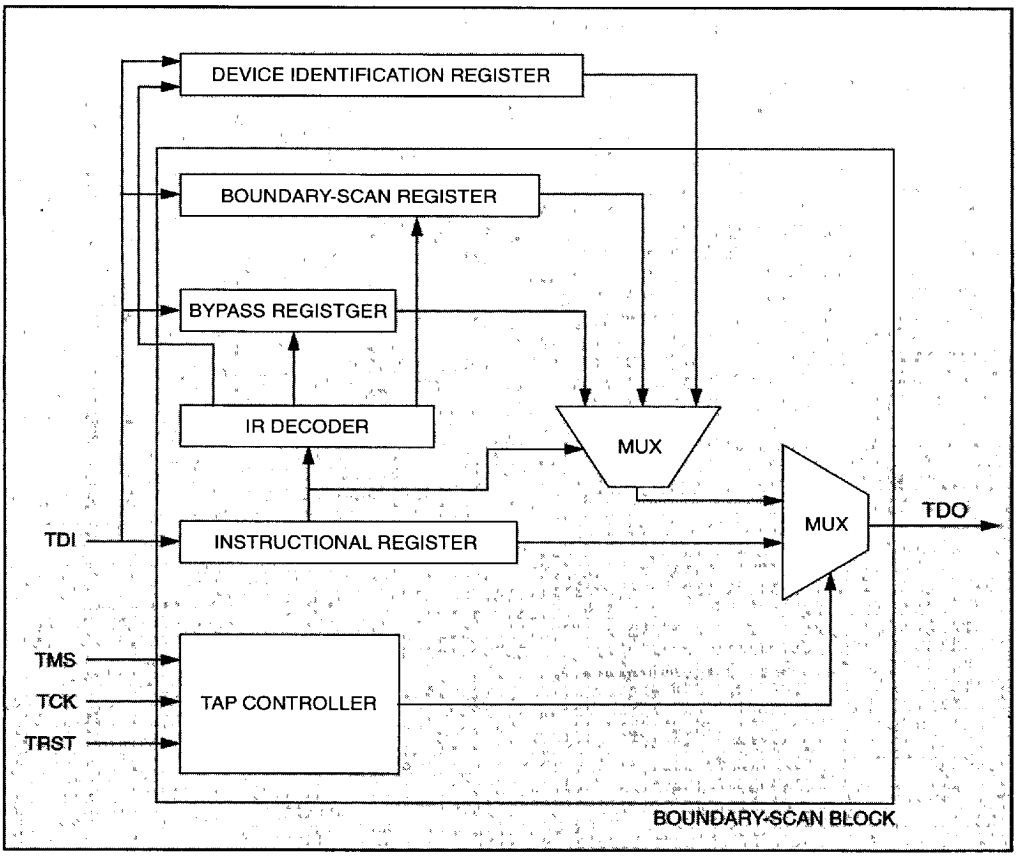
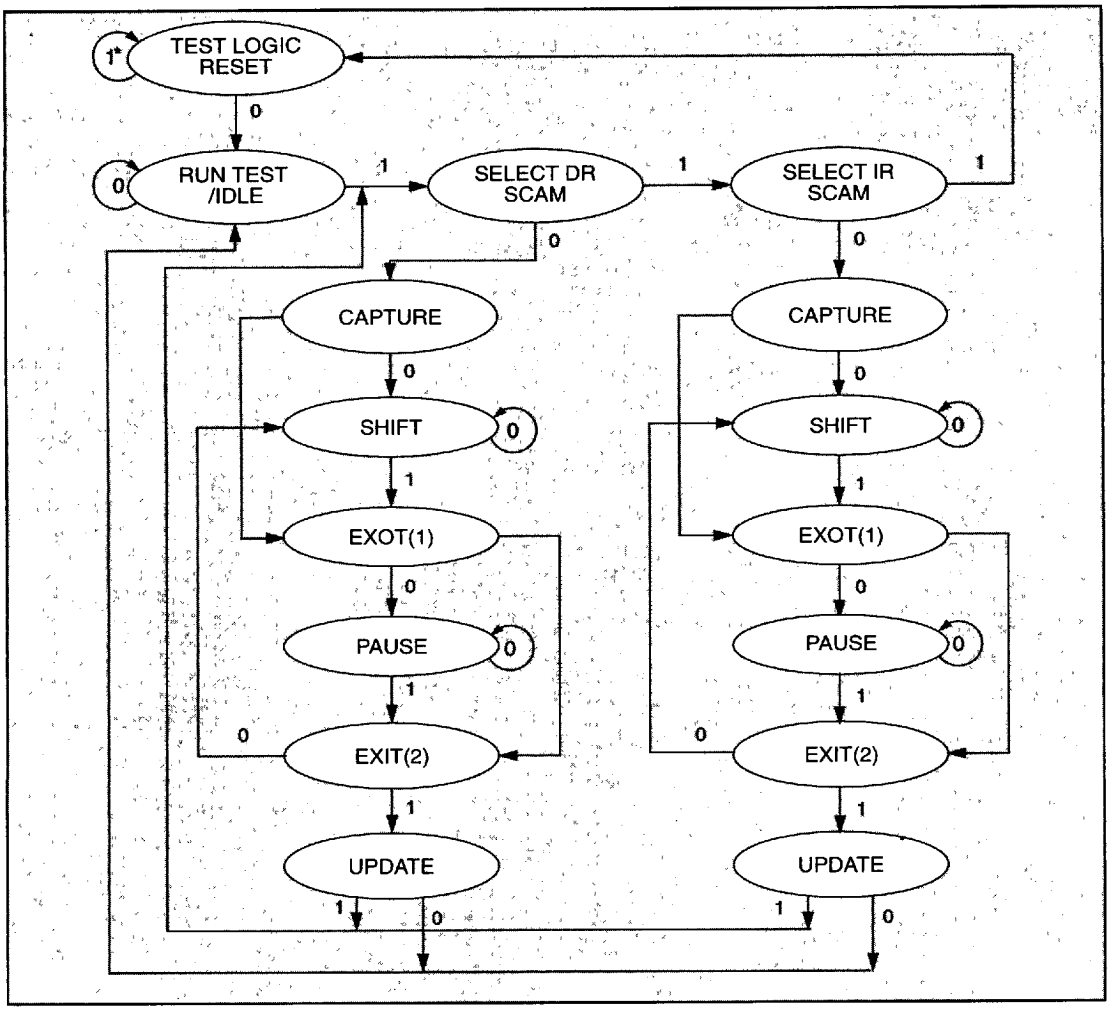


Figure 17. Boundary-Scan Block Diagram

JTAG (continued)

Boundary-Scan Conformance (continued)



*The logic value adjacent to a state-transition arc corresponds to the value of TMS.

Figure 18. TAP Controller State Diagram

JTAG (continued)

Boundary-Scan Conformance (continued)

JTAG is an *IEEE* 1149.1 (see Figure 18 for the state diagram) compatible test access port controller. State assignments used are from the 1149.1 specifications and are generated in the JTAG subnetwork. It also includes the bypass register, 2-bit instruction register, instruction decoder, and data MUX. This block has the additional logic to support the device identification register. The instruction decoder is wired to the following OP codes. (See Table 47.)

Table 47. OP Code Listing

OP Code	Instruction
00	EXTEST (Mandated By Standard)
01	SAMPLE
10	DEVICE ID (Selected Up Reset)
11	BYPASS (Mandated By Standard)

JTAG Test Port

The CSP1088 uses a JTAG/IEEE 1149.1 standard four-wire test port; there is no separate TRST input pin.

An instruction register, a boundary-scan register, a bypass register, and a device identification register have been implemented. The device identification register coding for the CSP1088 is shown in Table 50. The instruction register (IR) is 2 bits long. The instruction for accessing the device ID is 0xE (1110).

Table 48. JTAG Instruction Register

IR Cell #:	3	2	1	0
parallel input ?	Y	Y	N	N
always logic 1 ?	N	N	N	Y
always logic 0 ?	N	N	Y	N

The first line shows the cells in the IR that capture from a parallel input in the capture-IR controller state. The second line shows the cells that always load a logic 1 in the capture-IR controller state. The third line shows the cells that always load a logic 0 in the capture-IR controller state. Cell 3 (MSB of IR) is tied to status signal PINT, and cell 2 is tied to status signal JINT. The state of these signals can therefore be captured during capture-IR and shifted out during SHIFT-IR controller states.

The behavior of the instruction register is summarized in Table 49. Cell 0 is the LSB (closest to TDO).

- I = input cell
- O = 3-state output cell
- B = bidirectional (I/O) cell
- DC = bidirectional control cell

Table 49. JTAG Boundary-Scan Register

Cell	Type	Signal Name/Function
0	I	TC1
1	I	TC0
2	O	DAICK
3	I	DAIRN
4	I	DAIDI
5	O	DAIDO
6—13	I	AB[7:0]
14	I	I/O
15	I	RWN
16	O	INTR
17	I	RESETN
18	I	MC1
19—26	B	DB[15:8]
27	DC	Control Cell
28—35	B	DB[7:0]
36	I	EXTDI
37	O	SERLE
38	O	SERCK
39	O	SERDA
40—53	0	OCTL[13:0]

Table 50. CSP1088 32-bit JTAG ID Register

Bit	31—28	27—19	18—12	11—0
Field	0011	0x01	111000	0x03B

DSP1600 Programming Examples

The following examples contain DSP1600 program fragments for common interactions with AT&T CSP1088.

Typically, the following sequence of events is used to program and initialize the AT&T CSP1088:

1. Perform system self-test by writing/reading an AT&T CSP1088 register(s), set up interrupt service routines, initialize Mwait, etc.
2. Power up receiver for 7.0 ms to charge external reference capacitors.
3. Perform receiver dc offset calibration.
4. Program event timing and control, but leave inactive.
5. Program RAMPUP[15:0], RAMPDN[15:0], and RAMPLVL with power ramping profile.
6. If AUDIO conversion is needed, activate the AUDCHAR bit in AUDCONF to initialize AUDIO converters, then deactivate.
7. Activate event timing and control unit.
8. Process interrupts, perform frequency correction, adjust QBC timing, etc.

Example 1. Wait-States

When DSP1600 is operated at 26 MIPS, two wait-states are required when accessing AT&T CSP1088. Typically, AT&T CSP1088 is connected to the IO memory space of DSP1600. Thus, the following instruction would be required before accessing AT&T CSP1088:

```
mwait = 0x0020          /* 2 wait-states for IO space ERAM accesses          */
```

Example 2. dc Offset Calibration and Software Reset

A dc offset calibration must be done at powerup. It is also suggested that calibration be done after extended periods of inactivity. The following code fragment shows how to perform dc offset calibration for the AT&T CSP1088. Software reset is activated in an analogous manner. Note that receiver must have been powered up (using BIE in ETC word 1) for 7.0 ms to change reference caps, before running dc offset calibration.

```
/* CSP1088 dc Offset Calibration                                          */

      dc_offset:
            a0 = a0^a0                  /* clear a0                      */
            a0 = DC_OFFSET_BIT          /* set dc offset calibration bit */
            r0 = CONTROL_ADDRESS        /* CSP1088 CONTROL REG. Address  */
            *r0 = a0                    /* start calibration             */

      offset_cal:
            a0 = *r0                    /* check CONTROL register to     */
            a0 = a0h & DC_OFFSET_BIT    /* determine if dc offset        */
            if (gt) goto offset_cal     /* calibration is completed      */
```

DSP1600 Programming Examples (continued)

Example 3. Receive Buffer Data Move

Moving data from AT&T CSP1088 into the DSP can require a significant number of processor cycles. The next two examples show how to do this in a minimum number of cycles.

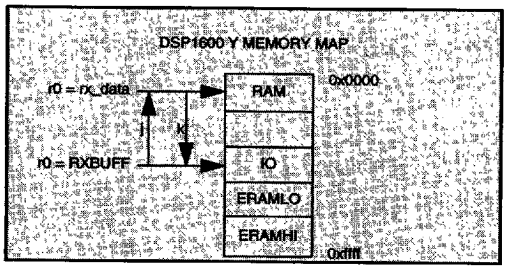


Figure 19. DSP1600 Memory Maps and Pointers

The DSP1600 Y memory map and pointers are shown in Figure 19. Compound addressing is used to efficiently move the data. The j increment is used as a decrement into internal RAM, and the k increment is used to get the next receive data word (effectively RXBUFF++). In receive mode, it is assumed that ten interrupts will be taken to read in an entire receive burst. This implies that the rx_data pointer will be changing versus RXBUFF which is a constant. This means it is necessary to calculate the j decrement value and the k increment value on an interrupt by interrupt basis. This calculation is not shown in the code fragment since it is dependent on main program's operation. This value is represented by "Decrement" in the code fragment. The following code fragment shows how the DSP1600 can move the data in four cycles per 16-bit word.

```
/* CSP1088 Receive buffer data move                                    */

      /* NOTE: Decrement is not an ADDRESS or a constant. It should be  */
      /*          calculated based on the current number (out of 320 for */
      /*          a complete RX burst) of words read.                   */

      rx_burst:
            j =   Decrement          /* RXBUFF - current rx_data pointer  */
            k = -(Decrement - 1)     /* increment to next CSP1088 RX word */
            r0 = RXBUFF              /* point to CSP1088 RX buffer        */

            a1 = *r0++               /* get first value                   */
            *r0jk:a1                 /* move 32 values into internal RAM  */
            *r0jk:a1                 /* buffer. 4 cycles total, including */
            *r0jk:a1                 /* 2 wait-states                     */
               .
               .
               .
            (total 32 r0jk:a1)
```

DSP1600 Programming Examples (continued)

Example 4. Transmit Buffer Data Move

Transmit data can be moved into AT&T CSP1088 in a manner similar to the receive buffer

```
/* CSP1088 Transmit Buffer Data Move                                    */

      tx_burst:
            /* use compound addressing to move 148 (160) bits         */
            /* from internal RAM to CSP1088                           */
            r0 = tx_data

            /* NOTE: BRSTDATA_ADDR is a constant, so the next         */
            /*       2 statements only contain 1 label.               */
            /*       This makes them relocatable instead of           */
            /*       absolute when linking.                           */
            /*       This is possible because the TX burst            */
            /*       is serviced by a single interrupt.               */

            /* 1st increment to BURST data buffer                     */
            j =   (BRSTDATA_ADDR - (tx_data + 1))
            /* Second decrement back to NEXT TX word                  */
            k = -(BRSTDATA_ADDR - (tx_data + 1)) + 1

            a1 = *r0++              /* get first value                */
            *r0jk:a1                /* move 32 values into internal RAM */
            *r0jk:a1                /* buffer. 4 cycles total, including */
            *r0jk:a1                /* 2 wait-states                  */
               .
               .
               .
            (total 10 r0jk:a1)
```

Example 5. Ciphering

The following code fragment illustrates how A5 ciphering is used in a polling mode. It can also be used with interrupts, and compound addressing can be used for more efficient data moves.

```
/* CSP1088 A51 encryption                                               */
      a51_enc:
            a0l = 0
            a1l = 0
            yl = 0
      kc_wr:
            r0 = kc_data
            r1 = BRSTDATA_ADDR
            do 4 {              /* move cypher key into               */
                  a0 = *r0++    /* BRSTDATA[3:0]                      */
                  *r1++ = a0
            }
```

DSP1600 Programming Examples (continued)

Example 5. Ciphering (continue)

```
tdma_wr:
      r0 = tdma_data
      do 2 {                    /* move tdma frame number into          */
           a0 = *r0++           /* BRSTDATA[4:5]                        */
           *r1++ = a0
      }
      /* start A51 encryption                                           */
      /* Note: A5ENBL must remain high until block 2                    */
      /*         generation is complete                                 */
      r0 = CONTROL_ADDRESS
      a0 = 0x1800               /* A5ENBL = 1, A5TYPE = 1               */
      *r0 = a0
blk1_gen:                       /* wait for block 1 completion          */
      y = *r0
      a1 = a0 - y
      if eq goto blk1_gen
blk1_rd:
      r0 = blk1out
      r1 = BRSTDATA2
      do 8  {                   /* move block 1 from BRSTDATA           */
           a0 = *r1++           /* starting at BRSTDATA[2] and          */
           *r0++ = a0           /* store in RAM at blk1out              */
      }
      /* clear status bit and start block2 generation                   */
      r0 = CONTROL_ADDRESS
      a0 = 0xd800               /* A5ENBL = 1, A5TYPE = 1               */
      *r0 = a0                  /* A5BLOCK = 1, A5STAT = 1              */
      a0 = 0x5800
blk2_gen:                       /* wait for block2 completion           */
      y = *r0
      a1 = a0 - y
      if eq goto blk2_gen
blk2_rd:
      r0 = blk2out
      r1 = BRSTDATA2
      do 8   {                  /* move block 2 from BRSTDATA           */
           a0 = *r1++           /* starting at BRSTDATA[2]              */
           *r0++ = a0           /* store in RAM at blk2out              */
      }
      /* clear status bit and control signals                           */
      r0 = CONTROL_ADDRESS
      a0 = 0x8000               /* A5STAT = 1                           */
      *r0 = a0
```

Device Characteristics

Absolute Maximum Ratings

The AT&T CSP1088 can be damaged if its absolute maximum ratings are exceeded, and prolonged exposure to the absolute maximum rating will degrade its reliability. Absolute maximum ratings are different from the recommended operating conditions which are specified in Table 51.

External leads can be bonded and soldered safely at temperatures of up to 300 °C in approximately 10 s.

Voltage Range on any Pin ..... V_{SS} – 0.5 V to V_{DD} + 0.5 V
Power Dissipation ..... 1 W
Ambient Temperature Range ..... –40 °C to + 85 °C
Storage Temperature Range ..... –65 °C to + 150 °C

Handling Precautions

Although the inputs are protected, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. AT&T employs a human-body model for ESD testing of 100 pF and 1500 Ω. The breakdown voltage for the AT&T CSP1088 is greater than 500 V.

Recommended Operating Conditions

Table 51. Recommended Operating Conditions

Clock Speed	Package	Digital Supply Voltage V_{DD} (V)		Analog Supply Voltage V_{DDD}, V_{DDB}, V_{DDV}		Ambient Temperature T_A	
		Min	Max	Min	Max	Min	Max
76.9 ns	TQFP	2.7 V	5.25 V	4.75 V	5.25 V	–40 °C	85 °C

Package Thermal Considerations

The recommended operating temperature range is based on standard industrial specifications. The temperature of the chip, T_J, can be calculated from:

$$T_J = T_A + (P \times \Theta_{JA})$$

where T_A is the ambient temperature, P is the power dissipation, and Θ_{JA} is the thermal impedance of the package.

Maximum Junction Temperature (T_J) in 100-Pin TQFP ..... 125 °C
100-pin TQFP Maximum Thermal Resistance in Still-Air-Ambient (Θ_{JA}) ..... 110 °C/W

WARNING: The user should be careful that the maximum junction temperature does not exceed 125 °C in any application.

Electrical Characteristics

Voiceband Input

Table 52 summarizes the electrical characteristics of the voiceband input section of the AT&T CSP1088.

Table 52. Audio Input Electrical Specifications (MICIN & AUXIN)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Input Gain Accuracy	—	—	–1.0	—	1.0	dB
V_{reg} Output Voltage	—	40 µF capacitor	2.7	3.0	3.3	V
V_{reg} Output Current	—	40 µF capacitor	250	—	—	µA
V_{reg} Output Noise	—	40 µF capacitor	—	45	100	μV_{RMS}
Full Scale at MICOUT	—	18 dB gain setting	—	88.4	—	mV_{RMS}
Full Scale at MICOUT	—	8 dB gain setting	—	280	—	mV_{RMS}
Signal-to-distortion Plus Noise Ratio	SDNR	0 dBm0	50	—	—	—
	SDNR	–10 dBm0	40	—	—	dB
	SDNR	–30 dBm0	35	—	—	dB
	SDNR	–40 dBm0	29	—	—	dB
	SDNR	–45 dBm0	24	—	—	dB
Gain Tracking, Relative to 0 dBm0, 18 dB Gain Setting	—	+3 dBm0 to –35 dBm0	0.5	—	0.5	dB
Frequency Response	—	100 Hz	–34	—	–18	dB
	—	200 Hz	–12	—	0	dB
	—	300 Hz	–0.25	—	0.25	dB
	—	1000 Hz	–0.25	—	0.25	dB
	—	3000 Hz	–0.25	—	0.25	dB
	—	3400 Hz	–0.9	—	0.25	dB
	—	4000 Hz	—	—	–6	dB
	—	4600 Hz	—	—	–35	dB
	—	8000 Hz	—	—	–45	dB
Power Supply Rejection	PSRR	3 kHz	35	—	—	dB
Idle Channel Noise	—	AUDIN register at 18 dB or 8 dB BW = 4 kHz	—	—	–65	dBm0
Crosstalk from D/A	—	—	—	—	–65	dB
Filter Group Delay	—	<800 Hz	—	—	2.8	ms
Filter Group Delay	—	≥800 Hz	—	—	0.8	ms
Response Time	—	Change AUDIG or AUDIS	—	—	100	ms

Electrical Characteristics (continued)

Voiceband Input (continued)

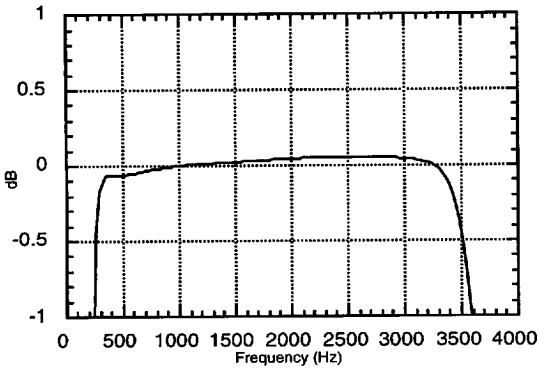


Figure 20. V x A/D Response BW = 4 kHz

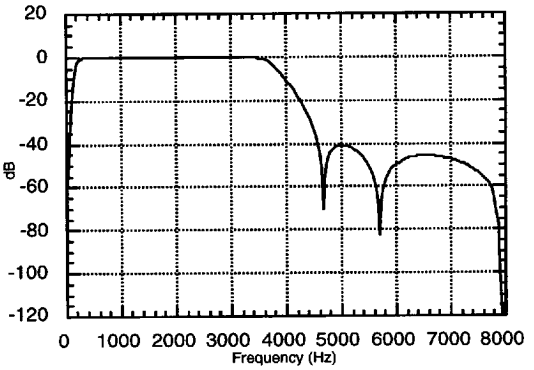


Figure 21. V x A/D Response BW = 8 kHz

Voiceband Output

Table 53 summarizes the electrical characteristics of the voiceband output section of the AT&T CSP1088.

Table 53. Audio Output Electrical Specifications

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Differential Load	RL	VOUT = 1.5 VRMS	200	—	—	Ω
	RL	VOUT = 0.75 VRMS	80	—	—	Ω
	RL	VOUT = 0.375 VRMS	30	—	—	Ω
	RL	VOUT = 0.188 VRMS	15	—	—	Ω
Differential Swing	—	RL = 600 Ω	—	—	1.5	Vrms
Idle Channel Noise	—	—	—	—	300	μVrms
Power Supply Rejection	PSRR	3 kHz, RL = 0.6 kΩ	35	—	—	dB
Image Frequency Attenuation	—	>4600 Hz	35	—	—	dB
Response Time AUDOG	—	—	—	—	100	ms
Signal-to-noise Plus Distortion	SNDR	0 dBm0	50	—	—	dB
	SNDR	–10 dBm0	40	—	—	dB
	SNDR	–30 dBm0	35	—	—	dB
	SNDR	–40 dBm0	29	—	—	dB
	SNDR	–45 dBm0	24	—	—	dB
Gain Tracking, Relative to 0 dBm0, 18 dB Gain Setting	—	+3 dBm0 to –40 dBm0	–0.5	—	0.5	dB
	—	–40 dBm0 to –50 dBm0	–0.8	—	0.8	dB
	—	–50 dBm0 to –55 dBm0	–1.2	—	1.2	dB

Electrical Characteristics (continued)

Voiceband Output (continued)

Table 53. Audio Output Electrical Specifications (continued)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Frequency Response	—	100 Hz	–34	—	–18	dB
	—	200 Hz	–12	—	0	dB
	—	300 Hz	–0.25	—	0.25	dB
	—	1000 Hz	–0.25	—	0.25	dB
	—	3000 Hz	–0.25	—	0.25	dB
	—	3400 Hz	–0.9	—	0.25	dB
	—	4000 Hz	—	—	–6	dB
	—	4600 Hz	—	—	–35	dB
	—	8000 Hz	—	—	–45	dB
Allowable CLK Input Jitter, Peak	—	—	—	—	5	ns
Filter Group Delay	—	<800 Hz	—	—	2.8	ms
Filter Group Delay	—	≥800 Hz	—	—	0.8	ms
Output Gain	—	0 dB setting	–0.5	—	0.5	dB
	—	–3 dB setting	–3.51	–3.01	–2.51	dB
	—	–6 dB setting	–6.52	–6.02	–5.52	dB
	—	⋮	⋮	⋮	⋮	⋮
	—	–45 dB setting	–45.65	–45.15	–44.65	dB

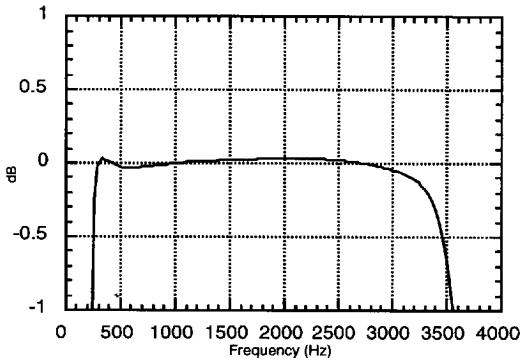


Figure 22. V x D/A Response BW = 4 kHz

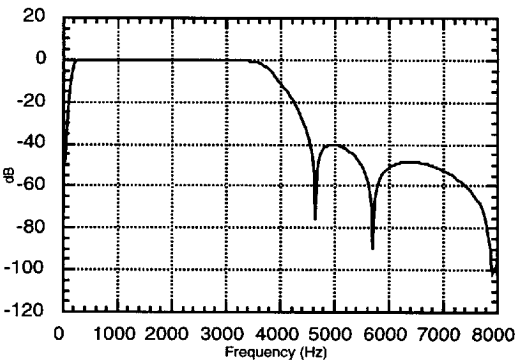


Figure 23. V x D/A Response BW = 8 kHz

Electrical Characteristics (continued)

Baseband Receive Channel

Table 54 summarizes the electrical characteristics of the baseband receive channel of the AT&T CSP1088.

Table 54. Baseband Receive Channel Electrical Characteristics (RxI & RxQ)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Word Length	—	—	—	10	—	bits
Output Word Rate per Channel	—	—	—	270.83	—	kHz
Sampling Mismatch	—	—	—	—	20	ns
Relative Gain Error	—	—	–0.4	—	0.4	dB
Absolute Gain Error	—	—	–1.0	—	1.0	dB
Gain Match I to Q	—	—	—	—	0.4	dB
Signal-to-noise + Distortion Ratio	SNDR	PGA = 0 dB, 1.0 Vpp 10 kHz Input	56	59	—	dB
dc Offset with Correction	—	PGA = 18 dB Voffset_RXIN* = ±30 mV	–3	—	3	LSB
Offset Correction Decay Rate		PGA = 18 dB Voffset_RXIN* = ±30 mV t ≤ 51 ms		0.025	—	LSB/ms
Rx Powerup Time		From V_{DDB} = 0, RxPD = 0			7.0	ms
Common-mode Input Range	—	V_{DD} = 5	1.3	—	3.5	V
Common-mode Input Resistance	—	—	40	—	—	kΩ
Differential Input Resistance	—	—	20	—	—	kΩ
Differential Input Voltage	—	PGA = 0 dB	—	—	1.0	Vp-p

* Voffset_RXIN = Maximum dc input offset voltage present at baseband receiver differential inputs (RXIP – RXIN, RXQP – RXQN).

Electrical Characteristics (continued)

Baseband Receive Channel (continued)

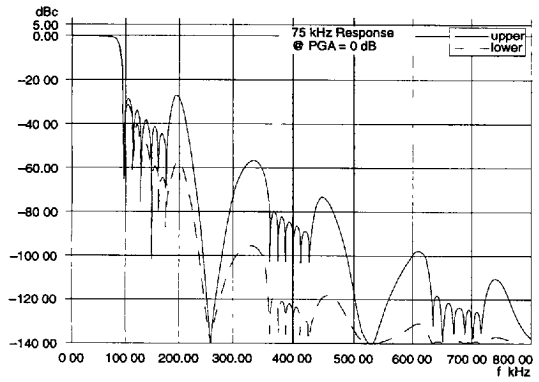


Figure 24. 75 kHz Response

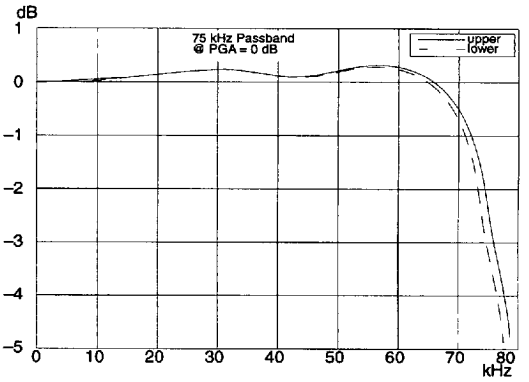


Figure 26. 75 kHz Passband

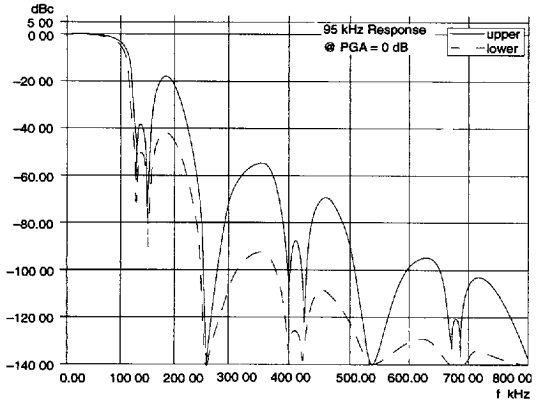


Figure 25. 95 kHz Response

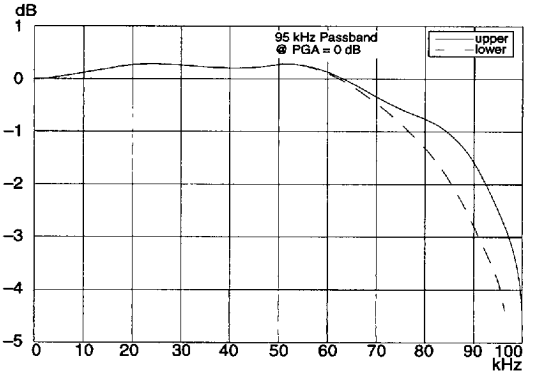


Figure 27. 95 kHz Passband

Electrical Characteristics (continued)

Transmit Power Control

Table 55 summarizes the electrical characteristics of the transmit power control channel (T x P).

Table 55. Electrical Characteristics of the Transmit Power Control Channel (T x P)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Word Length	—	—	—	—	9	bits
Min. Output Voltage	Vmin	T x P = 0	0.25	0.40	0.55	V
Max. Output Voltage	Vmax	T x P = 511	3.97	4.25	4.52	V
Voltage Swing	Vp-p	Full-Scale Amplitude	3.58	3.85	4.15	V
Differential Nonlinearity	DNL	—	–1	—	1	LSB
Integral Nonlinearity	INL	—	–1	±0.5	1	LSB
Sample Rate	—	—	—	13/12	—	MHz
Temp. Coefficient	Tc	T x P = 255	—	50	—	PPM/°C
Temp. Tracking w/TX	VCM	T x P = 0		30	—	mV
Load R	R_L	—	10			kΩ
Load C	C_L	—			25	pF

Baseband Transmit Channel

Table 56 summarizes the electrical characteristics of the baseband transmit channel of the AT&T CSP1088.

Table 56. Baseband Transmit Channel Electrical Specifications (TxI & TxQ)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Word Length	—	—	—	—	9	bits
I and Q Channel Mismatch	—	Full-Scale Amplitude	—	0.2	0.3	dB
Differential Output Voltage Range	—	TXVCM = 1.575 V Full-Scale Amplitude	0.9	1	1.1	Vp-p
Differential Offset: TxIp to TxIn, or TxQp to TxQn	—	With dc Offset Correction TXVCM = 1.575 V	–5	—	+5	mV
Passband Bandwidth	—	–3 dB	150	275	500	kHz
Passband Ripple	—	—	–1	—	1	dB
Passband Delay Distortion	—	—	—	—	2.5	µs
Differential Nonlinearity	DNL	—	–1	—	1	LSB
Integral Nonlinearity	INL	—	–1	±0.5	1	LSB
Sample Rate	—	—	—	13/6	—	MHz
I and Q Sampling Mismatch	—	—	—	—	20	ns
Load Resistance	R_L	dc coupled	10	—	—	kΩ
Load Capacitance	C_L	—	—	—	50	pF
Common-Mode dc	—	—	1.5	1.575	1.65	V
Tx Common-Mode dc Range	TXVCM	—	1.5	—	2.75	V
TXVCM Output Resistance During Powerdown	—	TXPD = 1	—	100	—	kΩ

Electrical Characteristics Voiceband Section (continued)

Baseband Transmit Channel (continued)

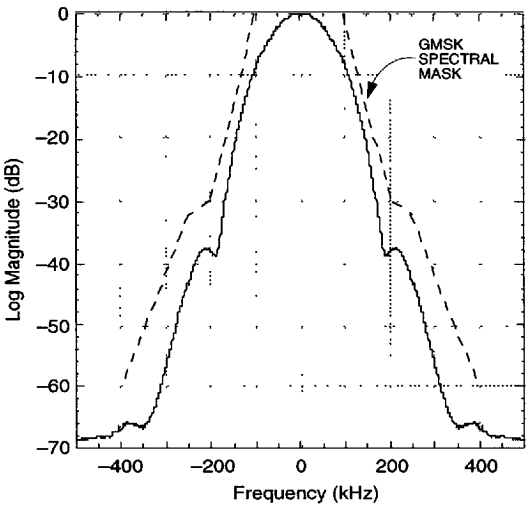


Figure 28. Typical Passband Spectrum When Transmitting Random Data

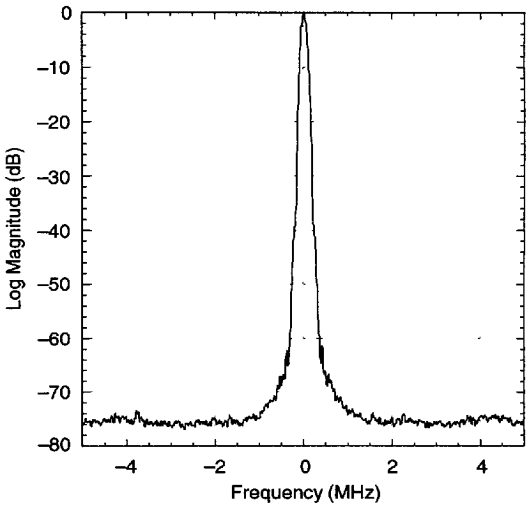


Figure 30. Typical Spectrum When Transmitting Random Data

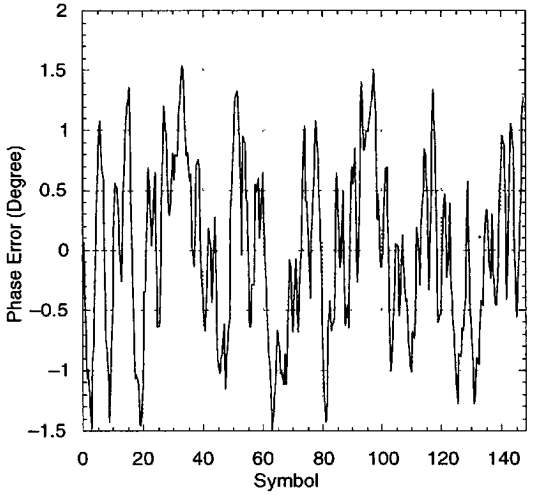


Figure 29. Typical Phase Error When Transmitting Random Data

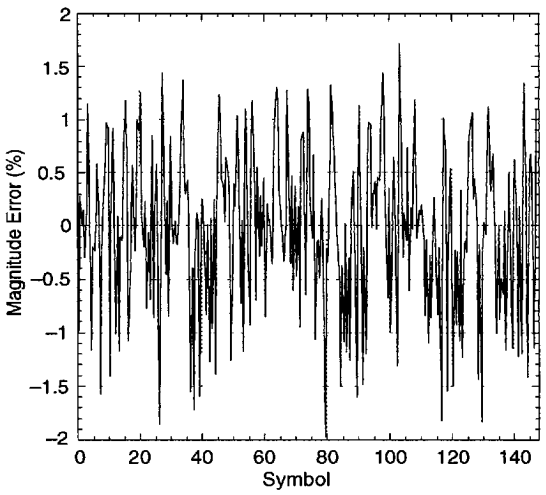


Figure 31. Typical Magnitude Error When Transmitting Random Data

Electrical Characteristics (continued)

The electrical characteristics in Table 57 are preliminary and are subject to change. Electrical characteristics refer to the behavior of the device under specified conditions. Electrical requirements refer to conditions imposed on the user for proper operation of the device. The parameters below are valid for the conditions described in the Recommended Operating Conditions section.

Table 57. Electrical Characteristics and Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input Voltage:						
Low	V_{IL}	—	—	0.3	V_{DD}	
High	V_{IH}	0.7	—	—	V_{DD}	
Input Current:						
Low (V_{IL} = 0 V, V_{DD} = 5.25 V)	I_{IL}	–5	—	—	mA	
High (V_{IH} = 5.25 V, V_{DD} = 5.25 V)	I_{IH}	—	—	5	mA	
Output Low Voltage:						
Low (I_{OL} = 2.0 mA)	V_{OL}	—	—	0.4	V	
Output High Voltage:						
High (I_{OH} = –2.0 mA)	V_{OH}	V_{DD} – 0.4 V	—	—	V	
Output 3-State Current:						
Low (V_{DD} = 5.25 V, V_{IL} = 0 V)	I_{OZL}	–10	—	—	mA	
High (V_{DD} = 5.25 V, V_{IH} = 5.25 V)	I_{OZH}	—	—	10	mA	
Input Capacitance, Digital Pins	CI	—	—	10	pF	
Small Signal Peak-to-Peak Voltage on MC1	V_{pp}	1.0	—	—	V	1
Small Signal Input Duty Cycle, 13 MHz	DC13	48	50	52	%	2
Small Signal Input Duty Cycle, 26 MHz	DC26	45	50	55	%	2
Small Signal MC1 Input Voltage Range	V_{in}	0.2 x V_{DD}	—	0.6 x V_{DD}	V	
Small Signal Input Buffer Start-up Time	t_{SSI}	—	—	10	µs	
Small Signal Output Buffer Peak-to-Peak Voltage on CLKO (C_L = 20pf, f = 26 MHz, V_{DD} = 2.7 V	V_{ppO}	—	1.0	—	V	3
Small Signal Output Buffer Common Mode Voltage (C_L = 20 pf, f = 26 MHz, V_{DD} = 2.7 V)	V_{CMO}	—	1.1	—	V	
Small Signal Output Buffer Load Capacitance (CLKO and CLKOREF)	C_{LO}	5	—	20	pF	
Small Signal Output Buffer Load Current (CLKO or CLKOREF)	I_O	—	—	5	µA	
Small Signal Output Buffer Start-up Time	t_{SSO}	—	—	10	µs	

Electrical Characteristics (continued)

Small Signal Clock Applications

1. The small signal input buffer must be used in a "single-ended" mode where an ac waveform (sine or square) is applied to MC1 and a dc voltage approximately equal to the average value of MC1 is applied to MC2, as shown in the figure below:

Figure 32. Small Signal Single-Ended Buffer

A diagram of an external network that produces signals for MC1 and MC2 from an oscillator unit is shown below.

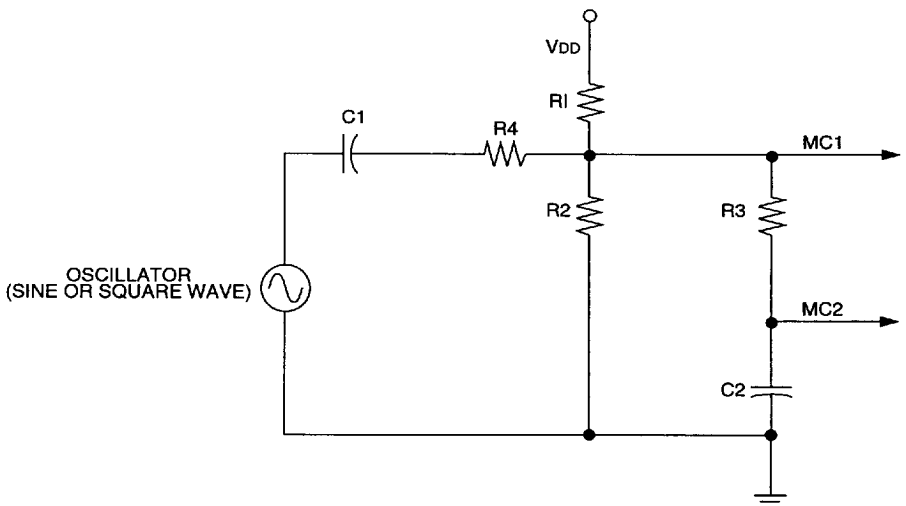


Figure 33. External Network for MC1 and MC2

The dc level will be set by R1 and R2, with the amplitude at MC1 being set by R3 and R4. C1 and C2 should be large enough so that their reactances at 13 MHz will be small compared to the resistors. Also, R1 and R2 should be much greater then R3 and R4. R3 should be sufficiently small so that the 5 ∝A leakage current will cause no more than 10 mV offset between MC1 and MC2. The equations for selecting component values would be as follows:

$$\text{MC1 (amplitude)} = \text{(oscillator amplitude)} \cdot \frac{R3}{R3 + R4}$$

$$\text{MC1, MC2 (dc level)} = V_{DD} \cdot \frac{R2}{R1 + R2} \pm 10\mu A\,(R2 \parallel R1)$$

$$\text{MC1, MC2 (offset)} = 5\ \mu A \cdot R3$$

Electrical Characteristics (continued)

Small Signal Clock Applications (continued)

For example, suppose that V_{DD} = 3.3, and the TCXO is a CMOS square wave with a 50/50 duty cycle. The following values meet the small signal input buffer requirements:

R1 = 16 kΩ, R2 = 11 kΩ, k3 = 500 Ω, R4 = 850 Ω, C1 = 100 pF, C2 = 1000 pF

The start-up time for the RC network is determined by the component values.

2. Duty cycle for a sine wave is defined as the percentage of time during each clock cycle that the voltage on MC1 exceeds the voltage on MC2. For 26 MHz operation, the input clock must be divided by 2 internally by setting the MCSEL bit of the Test Control Register. If a bias circuit that adjusts the voltage on MC2 to equal the average voltage on MC1 (see Figure 33) is used, then a 45/55 or a 55/45 duty cycle on the external oscillator is acceptable for 13 MHz operation.
3. The small signal output buffer produces two signals, CLKO and CLKOREF, that can be used to drive the CKI and CKI2 inputs, respectively, of a DSP1616/17/18/11 with a small signal input clock option. CLKO is an ac waveform, and CLKOREF is a low-pass filtered version of this, as shown in the figures below. Nothing else should be connected to CLKO or CLKOREF, except for an optional external capacitor from CLKOREF to ground for the purpose of reducing noise on CLKOREF. Note that additional capacitance on CLKOREF will increase the start-up time. If the output buffer is disabled, both CLKO and CLKOREF will go to V_{SS}.
4. When designing the printed-circuit board layout, the input and output small signal clocks (MC1,MC2 and CLKO,CLKOREF) should be treated as sensitive analog signals. They should be routed in such as way as to minimize trace length and coupling from other signals. CLKO and CLKOREF should be routed such that their load capacitances are approximately equal, or such that CLKOREF sees a higher capacitance than CLKO.

Figure 34. 26 MHz Operation

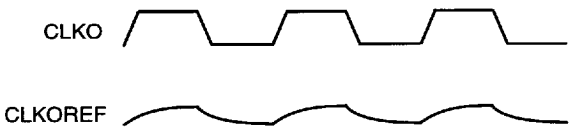


Figure 35. 13 MHz Operation

Electrical Characteristics (continued)

Differential Signals

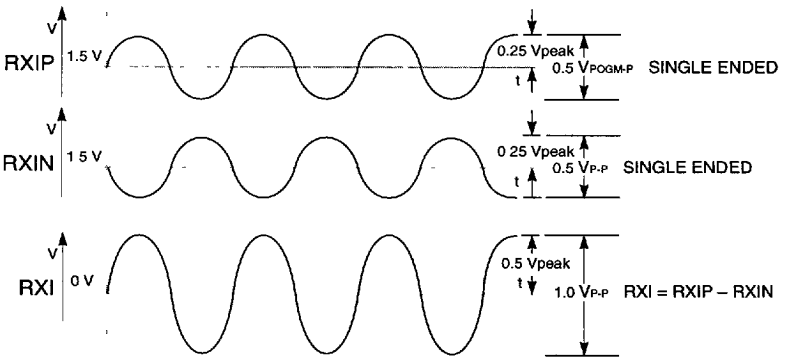
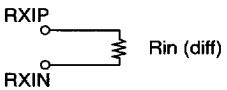


Figure 36. Differential Signal Definition

V_{RXI} (differential) = RXIP – RXIN

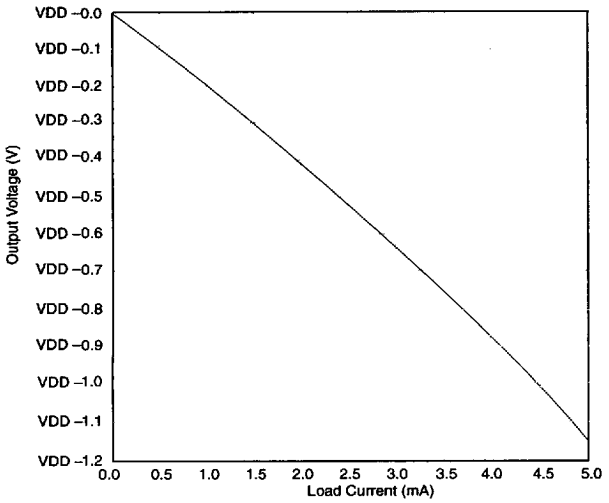
Differential Input Resistance:

$$\frac{V_{RXIP} - V_{RXIN}}{I_{PIN}} = R_{in}\,(diff)$$



Electrical Characteristics (continued)

Digital Output Buffer Drive



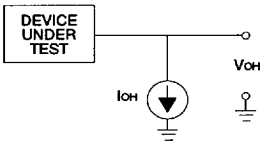
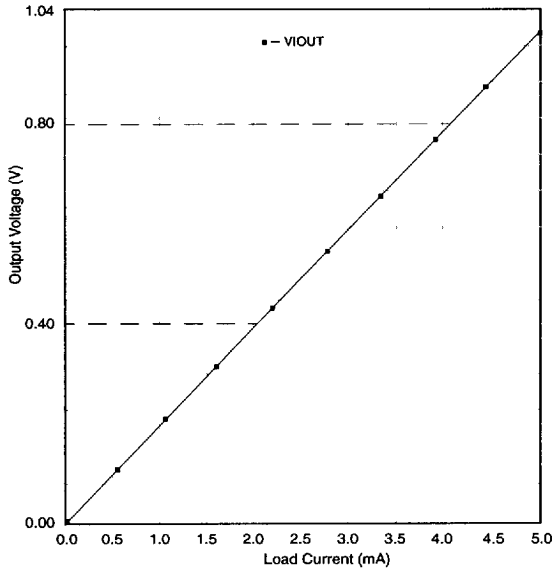


Figure 37. Plot of V_{OH} vs. I_{OH}, Typical Operating Conditions



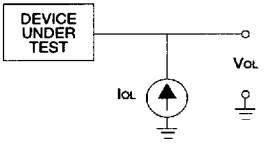


Figure 38. Plot of V_{OL} vs. I_{OL}, Typical Operating Conditions

Electrical Characteristics (continued)

Power Dissipation

Power dissipation is highly dependent on device activity and power supply. The following electrical characteristics are preliminary and are subject to change. All analog supplies (V_{DDD}, V_{DDB}, V_{DDF}, and V_{DDV}) are assumed to be 5.0 V.

Table 58. Power Dissipation

Operating Mode (Unused Inputs at VDD or VSS)	Typical Power Dissipation		
	(Digital Supply) 5.0 V	(Digital Supply) 3.0 V	(Digital Supply) 2.7 V
Typical TDMA Operation	118 mW	76 mW	75.0 mW
RX Mode (voice active)	227 mW	152 mW	147.0 mW
RX Mode (voice disabled)	190 mW	118 mW	112.0 mW
TX Mode (voice active)	160 mW	114 mW	110.0 mW
TX Mode (voice disabled)	115 mW	75 mW	72.0 mW
PLL (f = 26 MHz, QBC on)	60 mW	17 mW	14.0 mW
Standby (QBC on, PLL off)	34 mW	8 mW	5.8 mW

The power dissipation listed is for internal power dissipation only. Total power dissipation, including external parasitic load capacitance, can be calculated by adding $C \times (V_{DD})^2 \times f$ for each digital output, where C is the external load capacitance and f is the output frequency.

Power dissipation due to the digital input buffers is highly dependent on the input voltage level for digital pins. At full CMOS levels, essentially no dc current is drawn. However, for levels between the power supply rails, especially at or near the threshold of $V_{DD}/2$, high currents can flow. Therefore, **all unused input pins should be tied to their inactive state,** either V_{DD} or V_{SS}. The applications' maximum power, the package type, and the maximum ambient temperature determine the maximum activity factors for AT&T CSP1088. For more information, refer to the Absolute Maximum Ratings section. The following equations show how to calculate maximum power and junction temperature:

$$P = AF_{RX} \cdot P_{RX} + AF_{TX} \cdot P_{TX} + AF_{MONITOR} \cdot P_{MONITOR} + AF_{STANDBY} \cdot P_{STANDBY} + P_{EXTERNAL}$$

$$(T_J = P \cdot \Theta_{JA} + 85\ °C) \leq 125\ °C$$

where:
P = Maximum power in mW
AF_{RX} = Activity factor for RX mode
P_{RX} = Power dissipation in mW for RX mode operation
AF_{TX} = Activity factor for TX mode
P_{TX} = Power dissipation in mW for TX mode operation
$AF_{MONITOR}$ = Activity factor for monitor mode
$P_{MONITOR}$ = Power dissipation in mW for RX mode with voice disabled
$AF_{STANDBY}$ = Activity factor for standby mode
$P_{STANDBY}$ = Power dissipation in mW for sleep mode operation
$P_{EXTERNAL}$ = Power dissipation in mW for output switching power
TJ = Junction temperature
Q_{JA} = Thermal conductivity of 100 TQFP package = 110 °C/W

Electrical Characteristics and Requirements (continued)

Power Dissipation (continued)

For example, for a TQFP device in a 5 V application with 12.5% RX activity, 12.5% TX activity, 5% monitor activity (RX with voice disabled), and 70% standby activity, the equation would look like this:

$$P = 0.125 \cdot P_{RX} + 0.125 \cdot P_{TX} + 0.05 \cdot P_{MONITOR} + 0.7 \cdot P_{STANDBY}$$

$$(81.7 \text{ mW} \times 110 \text{ °C/W} + 85 \text{ °C} = 94.0 \text{ °C}) \leq 125 \text{ °C}$$

The above example demonstrates the maximum operating capability in the TQFP package. For low-voltage applications, the activity factor parameters become less critical.

Timing Characteristics

The following timing characteristics and requirements are preliminary information and are subject to change. Timing characteristics refer to the behavior of the device under specified conditions. Timing requirements refer to conditions imposed on the user for proper operation of the device. All timing data is valid for the following conditions:

T_A = –40 °C to +85 °C

2.7 V < V_{DD} < 5.25 V, V_{SS} = 0 V

Capacitance load on outputs (C_L) = 50 pF

Output characteristics can be derated as a function of load capacitance (C_L).

All outputs: $dt/dC_L \leq$ TBD ns/pF for $0 \leq C_L \leq 50$ pF at V_{IH} for rising edge
$dt/dC_L \leq$ TBD ns/pF for $0 \leq C_L \leq 50$ pF at V_{IL} for falling edge

For example, if the actual load capacitance is 30 pF instead of 50 pF, the derating for a rising edge is (30 – 50) pF x TBD ns/pF = TBD ns **less** than the specified rise time or delay which includes a rise time.

Test conditions for inputs:

Rise and fall times of 4 ns or less
Timing reference levels for delays = V_{IH}, V_{IL}
Test conditions for outputs (unless otherwise noted):

C_{LOAD} = 50 pF
Timing reference levels for delays = V_{IH}, V_{IL}
3-state delays measured to the high-impedance state of the output driver

AT&T CSP1088 is designed to interface directly to DSP1600 via the following signals: IO, RWN, INTR (usually connected to INT1 of DSP1600), AB[7:0], and DB[15:0]. When DSP1600 is operated at 26 MIPS (typical for GSM), then two wait-states are required when accessing AT&T CSP1088. Unless otherwise noted, CKO in the timing diagrams is the wait-stated DSP1600 CKO.

Timing Characteristics (continued)

CSP1088 Input Clock Generation and Reset

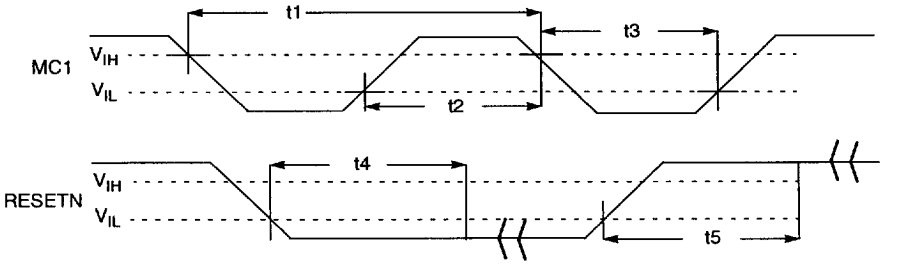


Figure 39. Master Clock Small Signal Differential

Table 59. Timing Requirements for Small Signal Input Clock (13 MHz)

Abbreviated Reference	Parameter	Min	Typ	Max	Unit
t1	Clock In Period (high to high)	76.9	—	—	ns
t2	Clock in Low Time	34.7	—	—	ns
t3	Clock in High Time	34.7	—	—	ns
t4	RESETN Enable Time (low to active)	—	—	500	ns
t5	RESETN Disable Time (high to inactive)	—	—	200	ns

Note: Device is fully static, t1 is tested at 100 µs, and register hold time is tested at 0.1 s.

Timing Characteristics (continued)

Digital Audio Interface

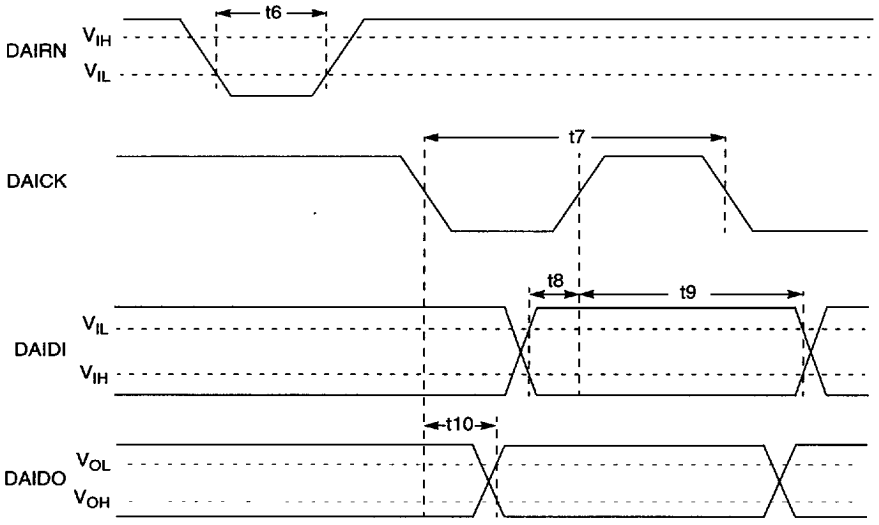


Figure 40. Digital Audio Interface Timing Diagrams

Table 60. Timing Requirements for Digital Audio Interface

Abbreviated Reference	Parameter	Min	Typ	Max	Unit
t6	Reset Active	4	—	—	ms
t7	Clock Out Period	—	9615	—	ns
t8	Data in SETUP TIME	100	—	—	ns
t9	Data in Hold Time	0	—	—	ns
t10	Data Out Delay	—	—	50	ns

Timing Characteristics (continued)

Data Read Timing

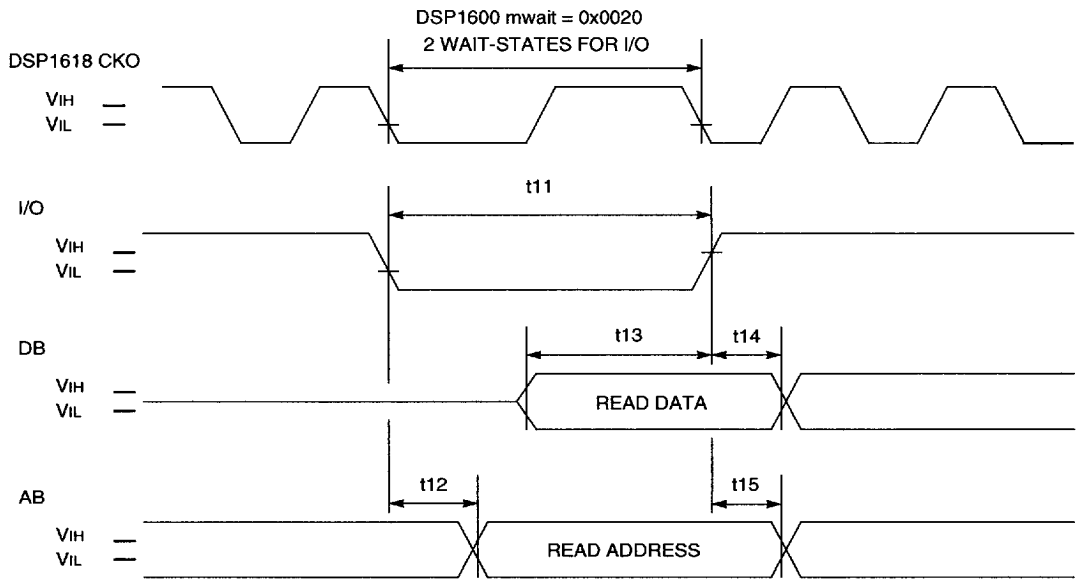


Figure 41. Data Read Timing Diagram (RWN Is Set to Logic High)

Table 61. Timing Characteristics for Read Access (RWN Is Set to Logic High.)

Abbreviated Reference	Parameter	Min	Typ	Max	Unit
t11	Enable Width (low to high)	110	—	—	ns
t12	Address Valid (enable low to valid)	—	—	4	ns
t13	Read Data Setup (data valid to IO high)	25	—	—	ns
t14	Read Data Hold (data hold from IO high)	0	—	—	ns
t15	Address Hold (address hold from IO high)	0	—	—	ns

Timing Characteristics (continued)

Data Write Timing

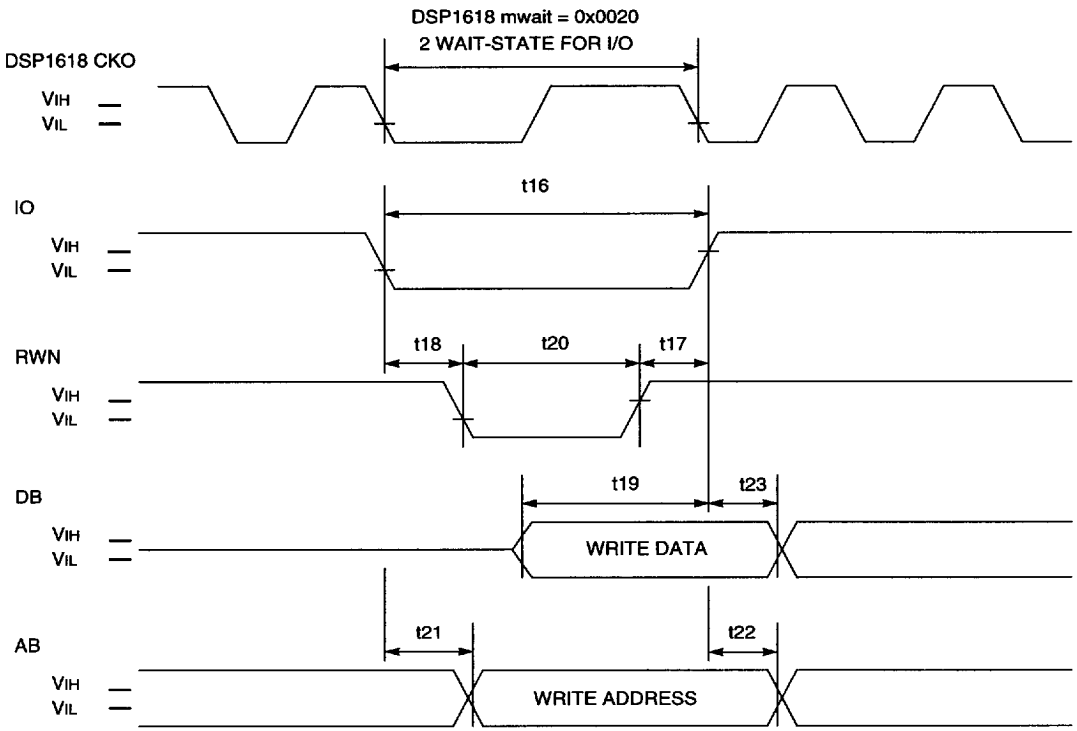


Figure 42. Data Write Timing Diagram

Table 62. Timing Characteristics Data Write

Abbreviated Reference	Parameter	Min	Typ	Max	Unit
t16	Enable Width (low to high)	110	—	—	ns
t17	RWN Advance (RWN high to enable high)	0	—	—	ns
t18	RWN Delay (enable low to RWN low)	0	—	—	ns
t19	Write Data Setup (data valid to RWN high)	50	—	—	ns
t20	RWN Width (low to high)	66	—	—	ns
t21	Write Address Setup (address valid to RWN low)	0	—	—	ns
t22	Write Address Hold (address hold from IO high)	0	—	—	ns
t23	Write Data Hold (data hold from IO high)	0	—	—	ns

Timing Characteristics (continued)

Serial Interface

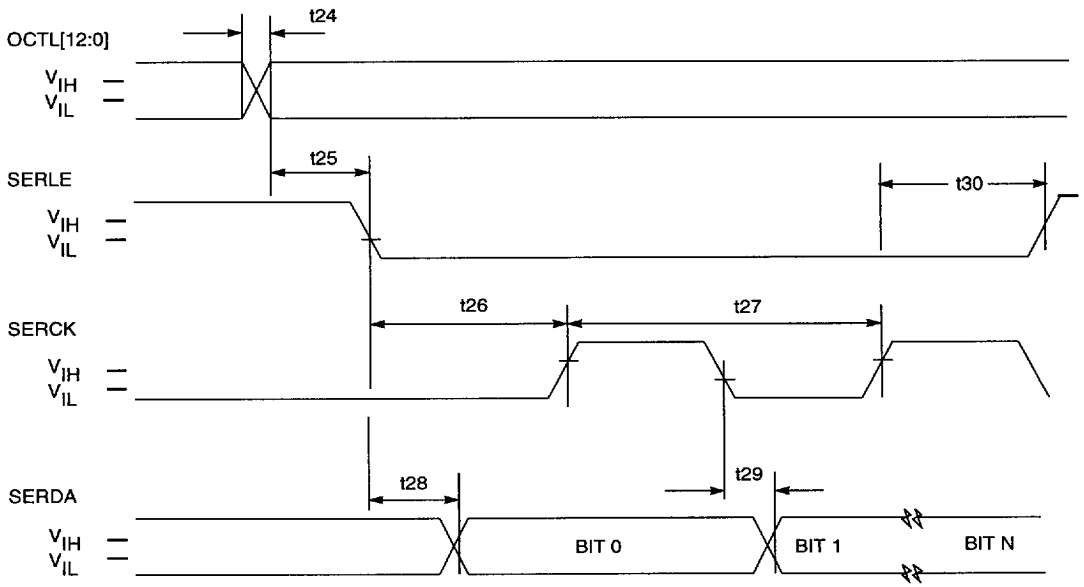


Figure 43. Serial Interface and OCTL[12:0] Timing Diagram

Table 63. Timing Characteristics for Serial Interface and OCTL[12:0]

Abbreviated Reference	Parameter	Min	Typ	Max	Unit
t24	Skew Between any Two OCTL Pins	0	—	15	ns
t25	Serial Interface Active Delay (relative to OCTL)	5.0	—	8.0	µs
t26	Serial Clock Active for 542 kHz/1.08 MHz Mode	400/900	—	—	ns
t27	Serial Clock Period for 542 kHz/1.08 MHz Mode	923/1846	—	—	ns
t28	Serial Data Delay (relative to SERLE low)	0	—	50	ns
t29	Serial Data Delay (relative to SERCK low)	0	—	50	ns
t30	Final Rising Edge of Serial Clock to SERLE High	400/900	—	—	ns

Timing Characteristics (continued)

JTAG I/O Specifications

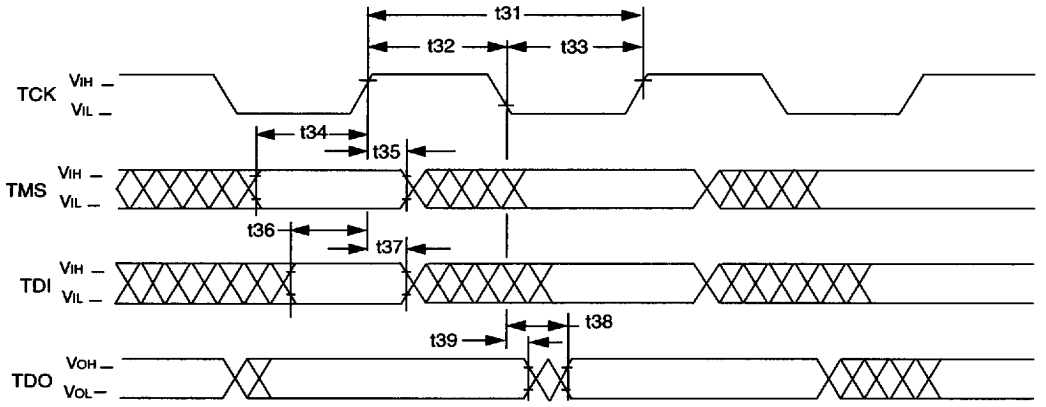


Table 64. Timing Requirements for JATG I/O

Abbreviated Reference	Parameter	Min	Max	Unit
t31	TCK Period (high to high)	150	—	ns
t32	TCK High Time (high to low)	35	—	ns
t33	TCK Low Time (low to high)	35	—	ns
t34	TMS Setup Time (valid to high)	10	—	ns
t35	TMS Hold Time (high to invalid)	5	—	ns
t36	TDI Setup Time (valid to high)	10	—	ns
t37	TDI Hold Time (high to invalid)	5	—	ns

Table 65. Timing Characteristics for JATG I/O

Abbreviated Reference	Parameter	Min	Max	Unit
t38	TDO Delay (low to valid)	—	25	ns
t39	TDO Hold (low to invalid)	0	—	ns

Outline Diagram

100-Pin Thin Quad Flat Pack TQFP

All dimensions are in millimeters.