16M x 64 PC100 SDRAM SO DIMM

Features

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual-In-line Memory Module
- 16Mx64 Synchronous DRAM SO DIMM
- Performance PC100

		-360	Units
$\overline{CAS}$ Latency		3	
f_{CK}	Clock Frequency	100	MHz
t_{CK}	Clock Cycle	10	ns
t_{AC}	Clock Access Time	6	ns

- Inputs and outputs are LVTTL (3.3V) compatible
- 10 Ohm Resistors on DQ's
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have 4 internal banks
- Fully Synchronous to positive Clock Edge
- Data Mask for Byte Read/Write control
- Programmable Operation:
  - CAS Latency: 2, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 12/9/2 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size: 2.66" x 1.25" x 0.149"
- Gold contacts
- SDRAMs in TSOP Type II Package

Description

IBM13T16644NPA is a 144-pin Synchronous DRAM Small Outline Dual In-line Memory Module (SO DIMM) which is organized as a 16Mx64 high-speed memory array. The SO DIMM uses eight 8Mx16 SDRAMs in 400mil TSOP II packages. The SO - DIMM achieves high speed data transfer rates of up to 100MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

The SO DIMM is intended to comply with all JEDEC and INTEL PC100 rev 1.0 standards set for 144 pin SDRAM SO DIMMs.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.

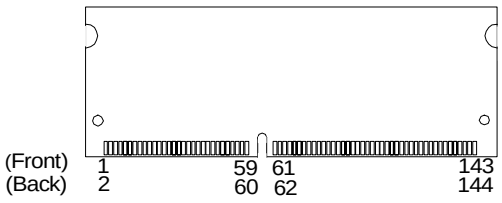
All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK1). Internal operating modes are defined by combinations of the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, $\overline{S1}$, DQMB, and CKE0, CKE1, signals. A command decoder initiates the necessary timings for each operation. A 12 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the SO DIMM by address inputs A0-A9 during the Mode Register Set cycle.

The SO DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.66" long space-saving footprint.

Card Outline



Pin Description

CK0, CK1	Clock Inputs	BS0 - BS1	SDRAM Bank Address
CKE0, CKE1	Clock Enable	DQ0 - DQ63	Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQMB0 - DQMB7	Data Mask
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (3.3V)
$\overline{WE}$	Write Enable	V_{SS}	Ground
$\overline{S0}$, $\overline{S1}$	Chip Selects	NC	No Connect
A0 - A11	Address Inputs	SCL	Serial Presence Detect Clock Input
A10 /AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output

Pinout

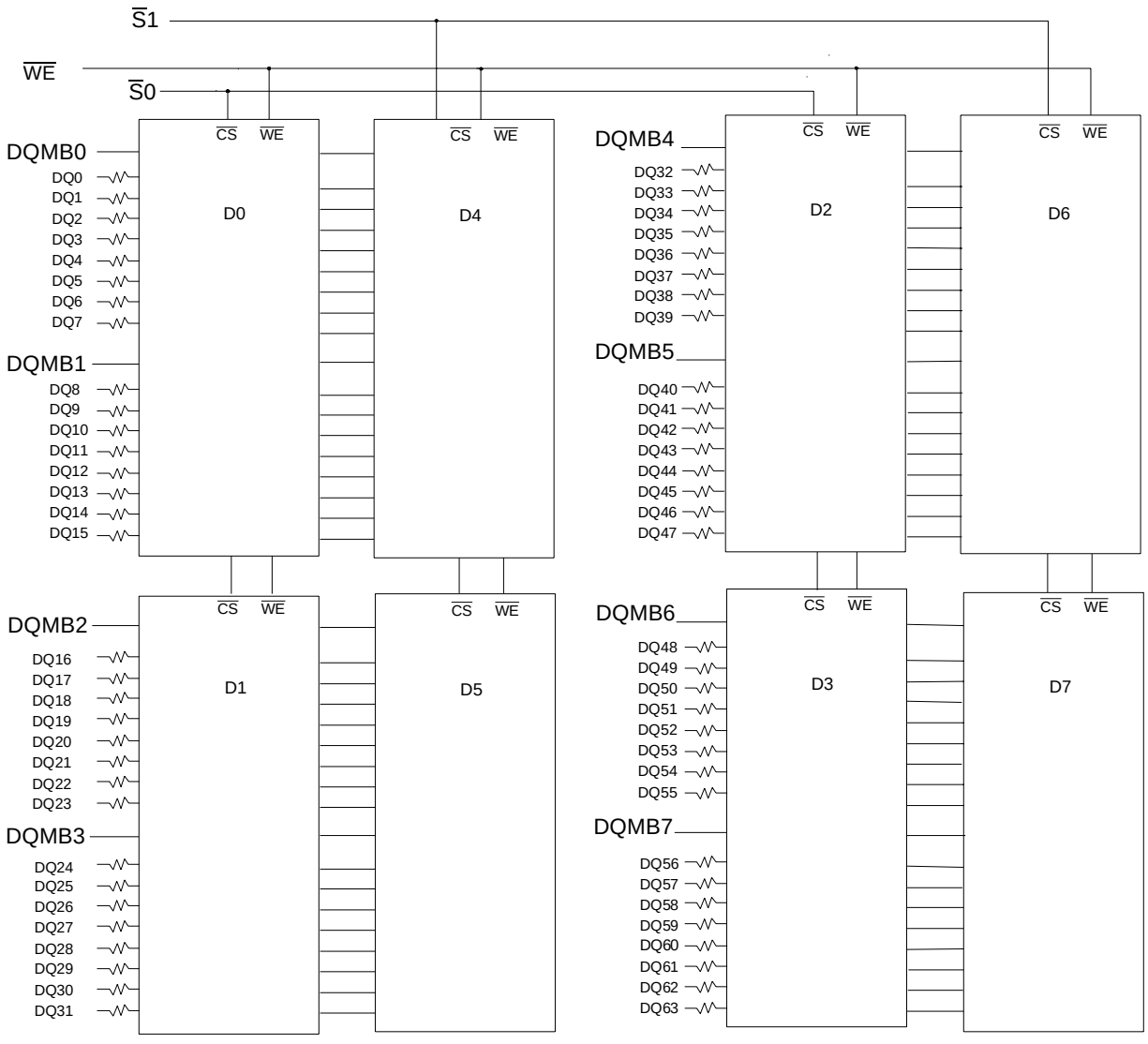
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	2	V_{SS}	37	DQ8	38	DQ40	71	$\overline{S1}$	72	NC	107	V_{SS}	108	V_{SS}
3	DQ0	4	DQ32	39	DQ9	40	DQ41	73	DU	74	CK1	109	A9	110	BS1
5	DQ1	6	DQ33	41	DQ10	42	DQ42	75	V_{SS}	76	V_{SS}	111	A10/AP	112	A11
7	DQ2	8	DQ34	43	DQ11	44	DQ43	77	NC	78	NC	113	V_{CC}	114	V_{CC}
9	DQ3	10	DQ35	45	V_{CC}	46	V_{CC}	79	NC	80	NC	115	DQMB2	116	DQMB6
11	V_{CC}	12	V_{CC}	47	DQ12	48	DQ44	81	V_{CC}	82	V_{CC}	117	DQMB3	118	DQMB7
13	DQ4	14	DQ36	49	DQ13	50	DQ45	83	DQ16	84	DQ48	119	V_{SS}	120	V_{SS}
15	DQ5	16	DQ37	51	DQ14	52	DQ46	85	DQ17	86	DQ49	121	DQ24	122	DQ56
17	DQ6	18	DQ38	53	DQ15	54	DQ47	87	DQ18	88	DQ50	123	DQ25	124	DQ57
19	DQ7	20	DQ39	55	V_{SS}	56	V_{SS}	89	DQ19	90	DQ51	125	DQ26	126	DQ58
21	V_{SS}	22	V_{SS}	57	NC	58	NC	91	V_{SS}	92	V_{SS}	127	DQ27	128	DQ59
23	DQMB0	24	DQMB4	59	NC	60	NC	93	DQ20	94	DQ52	129	V_{CC}	130	V_{CC}
25	DQMB1	26	DQMB5	VOLTAGE KEY				95	DQ21	96	DQ53	131	DQ28	132	DQ60
27	V_{CC}	28	V_{CC}	61	CK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
29	A0	30	A3	63	V_{CC}	64	V_{CC}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
31	A1	32	A4	65	$\overline{RAS}$	66	$\overline{CAS}$	101	V_{CC}	102	V_{CC}	137	DQ31	138	DQ63
33	A2	34	A5	67	$\overline{WE}$	68	CKE1	103	A6	104	A7	139	V_{SS}	140	V_{SS}
35	V_{SS}	36	V_{SS}	69	$\overline{S0}$	70	NC	105	A8	106	BS0	141	SDA	142	SCL
												143	V_{CC}	144	V_{CC}

Note: * Pin Assignments are NC for 4Mx64

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13T16644NPA-360T	16Mx64	10ns	Gold	2.66" x 1.25" x 0.149"	3.3V

16M x 64 PC100 SDRAM SO DIMM Block Diagram



Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0, CK1	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0, CKE1	Input	Level	Active High	Activates the CK0 and CK1 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BS0, BS1	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A11 A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0 defines the bank to be precharged (low=bank A, high=bank B). If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0 to control which bank(s) to precharge. If AP is high, both bank A and bank B will be precharged regard-less of the state of BA0. If AP is low, then BA0 is used to define which bank to precharge.
DQ0 - DQ63	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sam-pled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
SDA	Input Output	Level	—	Serial Data. Bidirectional signal used to transfer data into and out of the Serial Presence Detect EEPROM. Since the SDA signal is Open Drain/Open Collector at the EEPROM, a pull-up resistor is required on the system board.
SCL	Input	Pulse	—	Serial Clock. Used to clock all Serial Presence Detect data into and out of the EEPROM. Since the SCL signal is inactive in the “high” state, a pull-up resistor is recommended on the system board.
V_{CC}, V_{SS}	Supply			Power and ground for the module.

Serial Presence Detect (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	12	0C	
4	Number of Column Addresses on Assembly	9	09	
5	Number of DIMM Banks	2	02	
6 - 7	Data Width of Assembly	x64	4000	
8	Voltage Interface Level of this Assembly	LVTTL	01	
9	SDRAM Device Cycle Time at CL=3	10.0ns	A0	
10	SDRAM Device Access Time from Clock at CL=3	6.0ns	60	
11	DIMM Configuration Type	Non-Parity	00	
12	Refresh Rate/Type	SR/1x(15.625us)	80	
13	Primary SDRAM Device Width	x16	10	
14	Error Checking SDRAM Device Width	N/A	00	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	2, 3	06	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	
21	SDRAM Module Attributes	Unbuffered	00	
22	SDRAM Device Attributes: General	Wr-1/Rd Burst, Pre-charge All, Auto-Pre-charge, V_{CC} +/- 10%	0E	
23	Minimum Clock Cycle at CL=2	15.0ns	F0	
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2	9.0ns	90	
25	Minimum Clock Cycle Time at CL=1	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=1	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	20ns	14	
28	Minimum Row Active to Row Active delay (t_{RRD})	20ns	14	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	20ns	14	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	50ns	32	
31	Module Bank Density	64MB	10	
32	Address and Command Setup Time Before Clock	2.0ns	20	
33	Address and Command hold Time After Clock	1.0ns	10	
34	Data Input Setup Time Before Clock	2.0ns	20	
35	Data Input Hold Time After Clock	1.0ns	10	
36 - 61	Reserved	Undefined	00	
62	SPD Revision	1.2A	12	
63	Checksum for bytes 0 - 62	Checksum Data	cc	1

1. cc = Checksum Data byte, 00-FF (Hex)
2. “R” = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte “R”
4. yy = Binary coded decimal year code, 00-99 (Decimal) ‘00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) ‘01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

Serial Presence Detect (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Module Part Number	ASCII '13T16644NP"R"-360T'	31335431363634344E50 rr2D33363054202020	2, 3
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	4, 5
95 - 98	Module Serial Number	Serial Number	ssssssss	6
99 - 125	Reserved	Undefined	00	
126	Module Supports this Clock Frequency	100MHz	64	
127	Attributes for Clock Frequency defined in byte 126	CK0,CK1,CL3, concurrent AP	C5	
128 - 255	Open for Customer Use	Undefined	00	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) '00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) '01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{CC}	Power Supply Voltage		-0.3 to +4.6	V	1
V_{IN}	Input Voltage	SDRAM Devices	-0.3 to +V_{CC}+0.3		
		Serial PD Device	-0.3 to +6.5		
V_{OUT}	Output Voltage	SDRAM Devices	-0.3to +V_{CC}+0.3		
		Serial PD Device	-0.3 to +6.5		
T_{OPR}	Operating Temperature		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation		1.73	W	1, 2
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Power is calculated using I_{DD1} @ 3.6Volt.

Recommended DC Operating Conditions (T_A= 0 to 70°C)

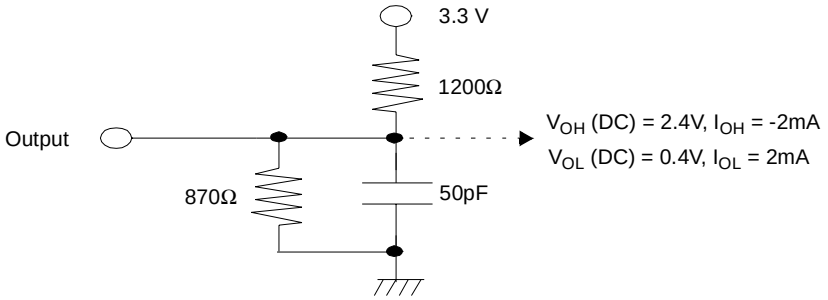
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f=1MHz, V_{CC}= 3.3V ± 0.3V)

Symbol	Parameter	Max. Capacitance	Units
C_{I1}	Input Capacitance (A0 - A9, A10/AP, A11, BS0, BS1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	58	pF
C_{I2}	Input Capacitance (CKE0, CKE1)	28	pF
C_{I3}	Input Capacitance ($\overline{S0}$, $\overline{S1}$)	28	pF
C_{I4}	Input Capacitance (CK0, CK1)	32	pF
C_{I5}	Input Capacitance (DQMB0 - DQMB7)	14	pF
C_{I6}	Input Capacitance (SCL)	13	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63)	17	pF
C_{IO2}	Input/Output Capacitance (SDA)	15	pF

DC Output Load Circuit



Output Characteristics (T_A= 0 to +70°C, V_{CC}= 3.3V ± 0.3V)

Symbol	Parameter		Min.	Max.	Units	Notes
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ V_{CC}), All Other Pins Not Under Test = 0V	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, A0-A9, A10/AP, A11, BS0, BS1	-8	+8	µA	
		CK0, CK1; CKE0, CKE1; S0, S1	-4	+4		
		DQMB0-7	-2	+2		
		SCL	-2	+2		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ V_{CC})	DQ0 - 63	-2	+2	µA	
		SDA	2	2		
V_{OH}	Output Level (LVTTL) Output “H” Level Voltage (I_{OUT} = -2.0mA)		2.4	—	V	1
V_{OL}	Output Level (LVTTL) Output “L” Level Voltage (I_{OUT} = +2.0mA)		—	0.4		

1. See DC output load circuit.

Operating, Standby and Refresh Currents (T_A= 0 to +70°C, V_{CC} = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	Speed/Organization	Units	Notes
			-360/16Mx64		
Operating Current $t_{RC} = t_{RC}$(min), t_{CK} = min Active-Precharge command cycling without Burst operation	I_{CC1}	1 bank operation	480	mA	1, 3, 4
Precharge Standby Current in Power Down Mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min)	8	mA	2
	I_{CC2Ps}	CKE ≤ V_{IL}(max), t_{CK} = Infinity, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min)	8	mA	2
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min)	280	mA	2, 5
	I_{CC2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity, $\overline{S0}$, $\overline{S1}$ =V_{IH} (min)	80	mA	2
No Operating Current (Active state: 4 bank)	I_{CC3N}	CKE ≥ V_{IH}(min), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min)	320	mA	2, 5
	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min, $\overline{S0}$, $\overline{S1}$ =V_{IH}(min) (Power Down Mode)	80	mA	2
Burst Operating Current	I_{CC4}	t_{CK} = min, Read/ Write command cycling	520	mA	1, 4, 5
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, CBR command cycling	900	mA	1, 6
Self Refresh Current	I_{CC6}	CKE0 ≤ 0.2V	6.4	mA	6
Serial PD Device Standby Current	I_{SB5}	V_{IN} = GND or V_{CC}	30	µA	7
Serial PD Device Active Power Supply Current	I_{CCA}	SCL Clock Frequency = 100KHz	1	mA	8

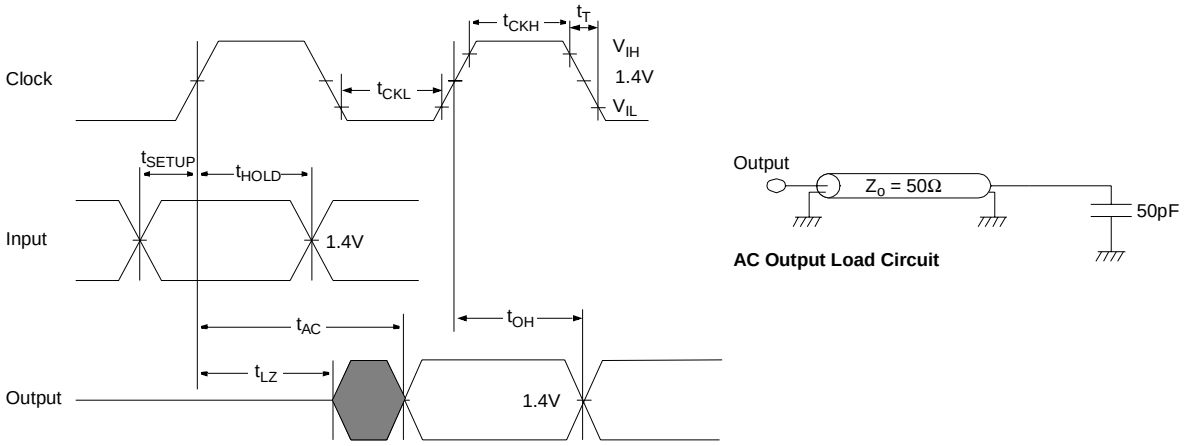
1. The specified values are for one SO DIMM bank in the specified mode and the other SO DIMM bank in Active Standby (I_{CC3N}).
2. The specified values are for both SO DIMM banks operating in the specified mode.
3. Input signals are changed up to three times during t_{RC}(min). This assumes the 14 Row Address mode with four-bank operation using rows A0-A11 and BA0-BA1.
4. The specified values are obtained with the outputs open.
5. Input signals are changed once during three clock cycles.
6. 64ms refresh time (15.6µs, 4K refresh).
7. V_{CC} = 3.3V.
8. Input pulse levels V_{CC} x 0.1 to V_{CC} x 0.9, Input rise and fall times 10ns, Input and output timing levels V_{CC} x 0.5, Output load 1 TTL gate and CL=100pf

AC Characteristics (T_A= 0 to +70°C, V_{CC}= 3.3V ± 0.3V)

An initial pause of 200µs, with DQMB0-7 and CKE0-CKE1 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.

1. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
2. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
3. Load Circuit: AC timing tests have V_{IL} = 0.8 V and V_{IH} = 2.0 V with the timing referenced to the 1.40V crossover point
4. Load Circuit: AC measurements assume t_T=1.2ns.

AC Characteristics Diagram



Clock and Clock Enable Parameters

Symbol	Parameter	-360 (CL, t_{RCD}, t_{RP} = 3 / 2 / 2)		Units	Notes
		Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	10	1000	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	15	1000	ns	1
t_{AC3}	Clock Access Time, $\overline{CAS}$ Latency = 3	—	6	ns	2
t_{AC2}	Clock Access Time, $\overline{CAS}$ Latency = 2	—	9	ns	2
t_{CKH}	Clock High Pulse Width	3	—	ns	3
t_{CKL}	Clock Low Pulse Width	3	—	ns	3
t_{CES}	Clock Enable Set-up Time	2	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	ns	
t_{SB}	Power down mode Entry Time	0	10	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	ns	

1. For -360 sort, 66Mhz clock: $\overline{CAS}$ Latency = 2.
2. Access time is measured at 1.4V. See AC Characteristics: notes: 1, 2, 3, 4 .
3. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Common Parameters

Symbol	Parameter	-360 (CL, t_{RCD}, t_{RP} = 3 / 2 / 2)		Units	Notes
		Min.	Max.		
t_{CS}	Command Setup Time	2	—	ns	
t_{CH}	Command Hold Time	1	—	ns	
t_{AS}	Address and Bank Select Set-up Time	2	—	ns	
t_{AH}	Address and Bank Select Hold Time	1	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	—	ns	1
t_{RC}	Bank Cycle Time	70	—	ns	1
t_{RAS}	Active Command Period	50	100000	ns	1
t_{RP}	Precharge Time	20	—	ns	1
t_{RRD}	Bank to Bank Delay Time	20	—	ns	1
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	—	CLK	

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Mode Register Set Cycle

Symbol	Parameter	-360 (CL, t_{RCD}, t_{RP} = 3 / 2 / 2)		Units	Notes
		Min.	Max.		
t_{RSC}	Mode Register Set Cycle Time	2	—	CLK	1

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

Read Cycle

Symbol	Parameter	-360 (CL, t_{RCD}, t_{RP} = 3 / 2 / 2)		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0	—	ns	
t_{HZ3}	Data Out to High Impedance Time	3	6	ns	1
t_{HZ2}	Data Out to High Impedance Time	3	8	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	CLK	1

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage level.

Refresh Cycle

Symbol	Parameter	-360 (CL, t_{RCD}, t_{RP} = 3 / 2 / 2)		Units	Notes
		Min.	Max.		
t_{REF}	Refresh Period	—	64	ms	1
t_{SREX}	Self Refresh Exit Time	10		ns	

1. 4096 auto refresh cycles.

Write Cycle

Symbol	Parameter	-360 (CL, t_{RCD}, t_{RP} = 3 / 2 / 2)		Units
		Min.	Max.	
t_{DS}	Data In Set-up Time	2	—	ns
t_{DH}	Data In Hold Time	1	—	ns
t_{DPL}	Data Input to Precharge	10	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	CLK

Clock Frequency and Latency

Symbol	Parameter			Units
f_{CK}	Clock Frequency	100	66	MHz
t_{CK}	Clock Cycle Time	10	15	ns
t_{AA}	$\overline{CAS}$ Latency	3	2	CLK
t_{RP}	Precharge Time	2	2	CLK
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	2	2	CLK
t_{RC}	Bank Cycle Time	7	6	CLK
t_{RAS}	Minimum Bank Active Time	5	4	CLK
t_{DPL}	Data In to Precharge	1	1	CLK
t_{DAL}	Data In to Active/Refresh	3	3	CLK
t_{RRD}	Bank to Bank Delay Time	2	2	CLK
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	1	CLK
t_{WL}	Write Latency	0	0	CLK
t_{DQW}	DQM Write Mask Latency	0	0	CLK
t_{DQZ}	DQM Data Disable Latency	2	2	CLK
t_{CSL}	Clock Suspend Latency	1	1	CLK

Presence Detect Read and Write Cycle

Symbol	Parameter	Min	Max	Unit	Notes
f_{SCL}	SCL Clock Frequency		100	kHz	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs	
t_{LOW}	Clock Low Period	4.7		µs	
t_{HIGH}	Clock High Period	4.0		µs	
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_r	SDA and SCL Rise Time		1	µs	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

1. The Write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal Erase/Program cycle. During the Write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

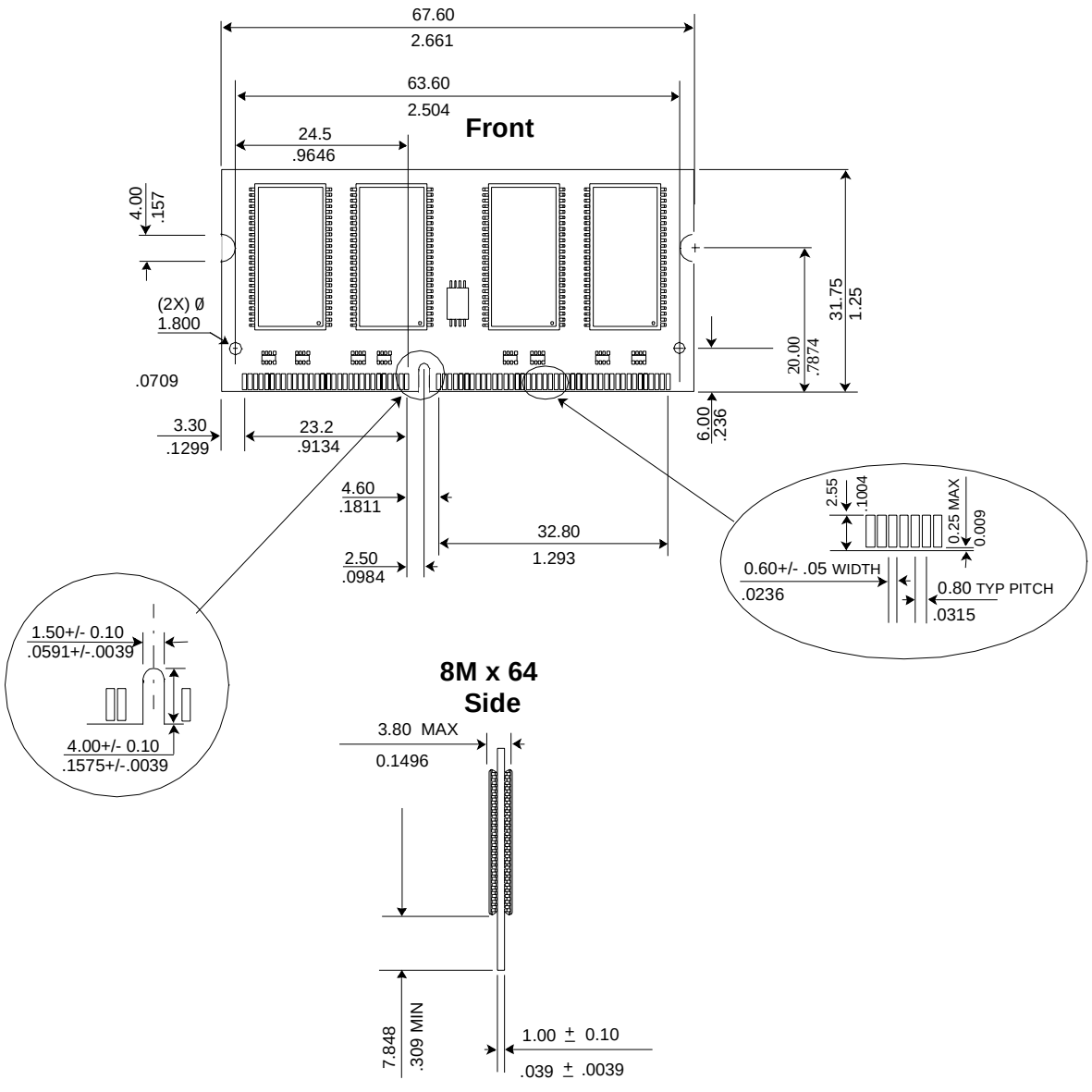
Functional Description and Timing Diagrams

Refer to the IBM 64Mb Synchronous DRAM data sheet, document 33L8019.F45415, for the functional description and timing diagrams for SDRAM operation

Refer to the IBM Application Notes: *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

All AC timing information refers to the timings at the SDRAM devices.

Layout Drawing



Note: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Revision Log

Rev	Contents of Modification
7/99	Initial Release
11/99	Removed Preliminary
2/01	Corrected error in title of block diagram.

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IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351

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