ABRIDGED VERSION

SSI 34P3210

Read Channel for High Density Floppy and Tape Storage

Advance Information

February 1996

DESCRIPTION

The SSI 34P3210 is a high performance BiCMOS single chip read channel IC for high density floppy or tape storage applications. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. VCO range of 0.6 MHz to 9.6 MHz is selectable through the serial port.

Programmable functions of the SSI 34P3210 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 34P3210 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption. The SSI 34P3210 supports a sleep mode for minimal power dissipation in non-operational periods.

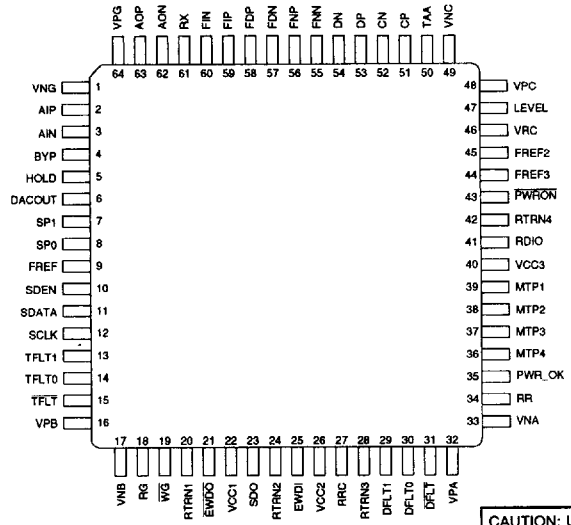
The SSI 34P3210 is available in a 64-lead TQFP package.

FEATURES

- **Complete zoned recording application support**
- **VCO range: 0.6 MHz to 9.6 MHz selectable through the serial port**
- **Supports 1,7 RLL, MFM, FM, and GCR Encoding Formats**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Programmable cutoff frequency of 0.4 to 4 MHz**
- **Time base generator with better than 1% frequency resolution**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data synchronizer with programmable window shift control**
- **Programmable write precompensation**
- **Write equalization**
- **Write current DAC**

(continued)

PIN DIAGRAM



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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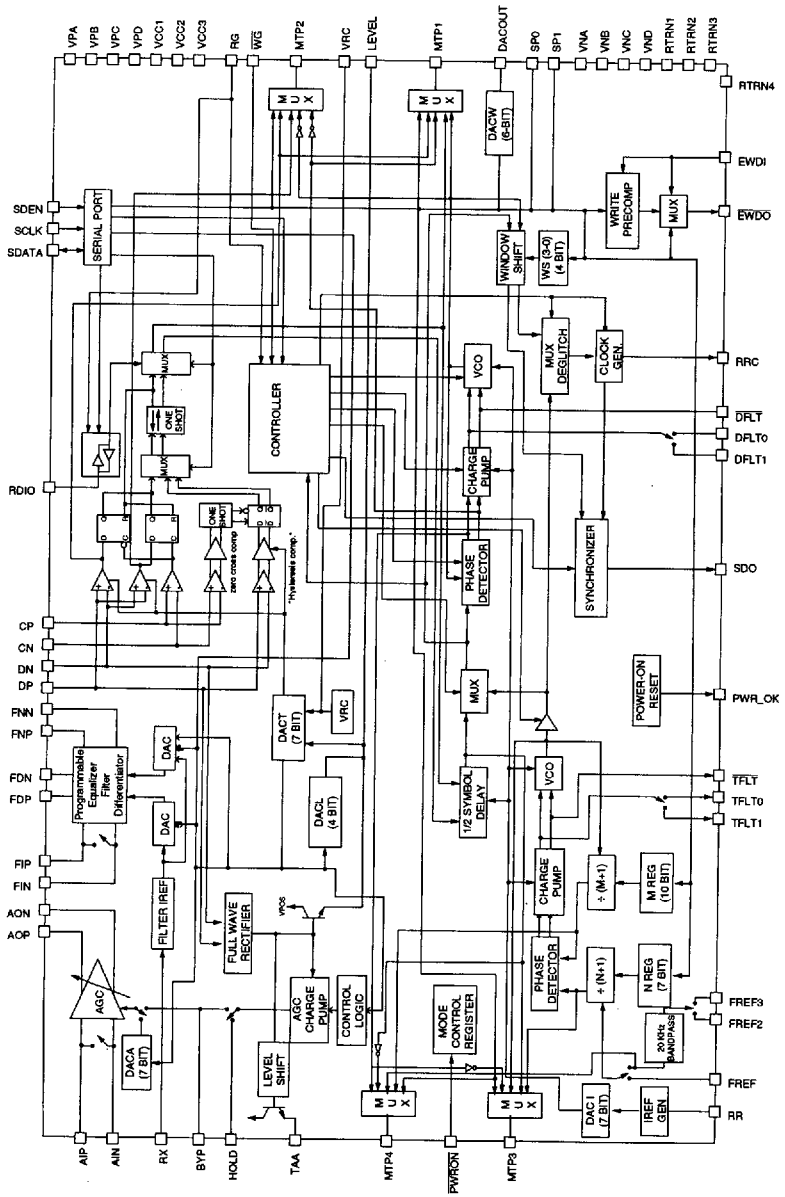
BLOCK DIAGRAM



FEATURES (continued)

- Bi-directional serial port for register access
- Register programmable power management (Sleep mode <5 mW)
- Power-on reset function
- Low Operating Power (400 mW typical @ 5V)

FUNCTIONAL DESCRIPTION

The SSI 34P3210 implements a high performance complete read channel, including pulse detector, programmable active filter, time base generator, data synchronizer, and VCO range of 0.6 MHz to 9.6 MHz. A circuit block diagram is shown in Figure 1.

PULSE DETECTOR

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC Circuit

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}). A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the correct AGC level, the nominal attack current of approximately 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the correct AGC level, a fast attack current of approximately eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of approximately 4 µA acts to increase the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA : 4 µA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased, if required. In fast decay mode, the decay current is increased by a factor of approximately 21.

When the chip is in power down mode, the AGC dual rate charge pump is disabled.

The AGC amplifier can be set into a fixed gain mode. The gain is programmable over a 2 to 51 V/V range in 0.4 V/V steps by a 7-bit DAC (DACA). If DACA = 0, the amplifier is in AGC mode.

BYP Control Voltage

The BYP capacitor voltage will be held constant (subject to leakage currents) during sleep mode, write mode, or when the HOLD signal is high. Upon the transition of $\overline{PWRON}$ from high to low, there is a 1 uS delay inserted before the AGC charge pump is allowed to drive the BYP capacitor.

AGC Mode Control

When write gate ($\overline{WG}$) is driven low, the Low-Z mode is activated. In this mode the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced also. When the $\overline{WG}$ pin transitions from low to high, the Low-Z mode is held for 1 µs. The input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the LOW-Z mode is the fast decay mode which allows rapid acquisition of the proper AGC level. The duration of the LOW-Z and fast decay mode is internally set at a nominal 1 µs. When the pulse detector is powered-down, V_{BYP} will be held constant subject to leakage currents only. Upon power-up, the LOW-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYP} will be held constant subject to leakage currents only.

FUNCTIONAL DESCRIPTION(continued)

Peak Level Output

An open emitter follower output proportional to DP-DN and referenced to ground is also provided. A capacitor/resistor combination connected to the TAA pin allows a peak detector with variable decay to be constructed.

RDIO Pin

A CMOS compatible, 30 ns wide, Raw Data I/O (RDIO) signal is provided. The signal at this pin is controlled through several bits in the serial port register set as shown in the table below.

During normal operation, RDIO is held low when RG is high. Bit 7 of register 20 allows this feature to be bypassed. When bit 7 is high RDIO will be the Read Data Output of the qualifier, independent of the RG input.

Qualifier Selection

The SSI 34P3210 provides both hysteresis and dual comparator pulse qualification circuits that may be selected for read mode operation. The pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for read mode. The option of using a fixed threshold is also provided. Register 34 bit 4 allows the user to set the data threshold as fixed or driven by the level pin. If set as fixed the threshold is set as if the DP/DN amplitude is 1 Vp-pd. Whether fixed or floating the threshold is set by the DACT value in the DTCR. The formula for the threshold level is

Threshold = DACT • 0.93/127 for 38 < DACT < 127

Dual Comparator Qualification

When in dual comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by LEVEL and referenced to VRC. Hysteresis thresholds from 10 to 80% may be set with a resolution of 1%. An external resistor/capacitor combination (RT/CT) set the hysteresis threshold time constant. DACL is set by a 4-bit register to determine the sink current magnitude in data mode. In data mode, the four LSBs of the Hysteresis Decay Control Register (HDCR) determine the value of the pull-down current. The LSB value of DACL is 3.125 µA, and DACL is offset by 1 LSB such that "0000" corresponds to 3.125 µA, and "1111" results in 50 µA. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot. Dual comparator timing is shown in Figure 2A.

Hysteresis Comparator Qualification

When the hysteresis qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Hysteresis comparator timing is shown in Figure 2B.

RG	$\overline{WG}$	Reg 12 Bit 5 RDI/O	Reg 20 Bit 6 WCLK IN	Reg 20 Bit 7 RDIO	SIGNAL
0	0	1	1	X	WCLK Input
1	1	1	0	X	Read Data Input
0	1	0	0	0	Read Data Output
1	1	0	0	0	No Output
1	1	0	0	1	$\overline{DRD}$ Output

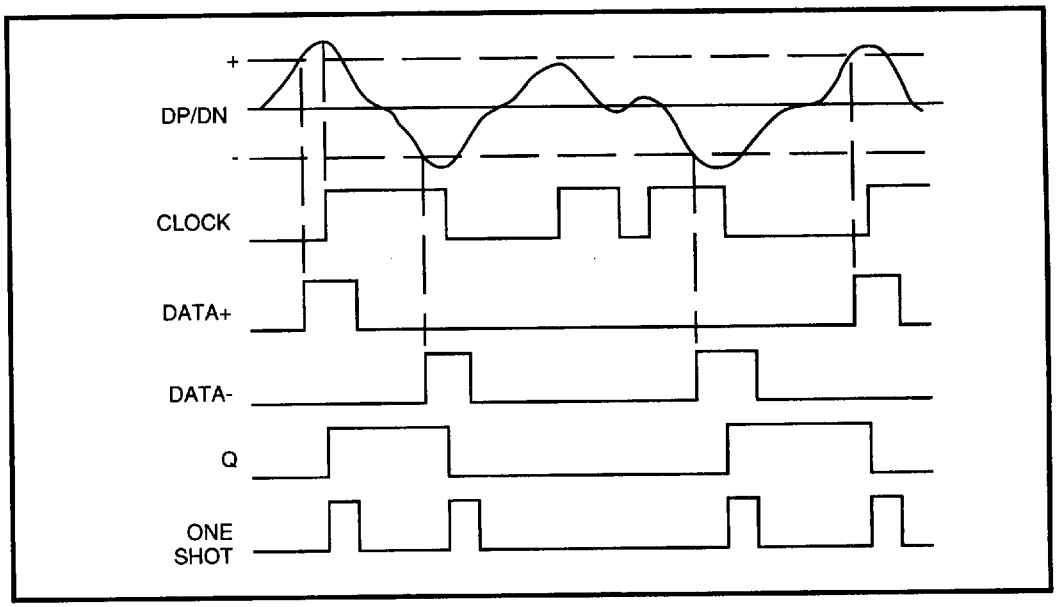


FIGURE 2A: Dual Comparator Timing Diagram

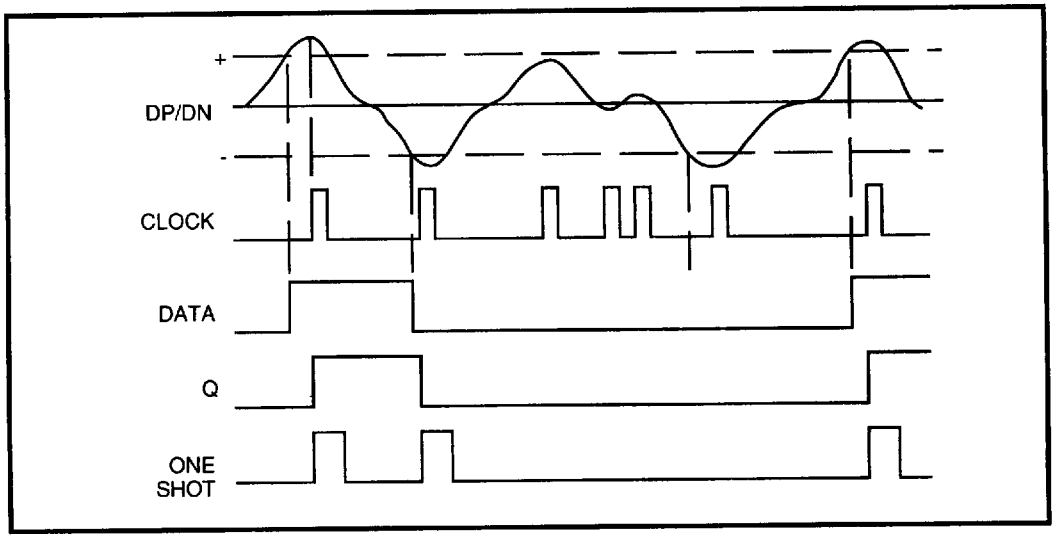


FIGURE 2B: Hysteresis Comparator Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

PROGRAMMABLE FILTER

The SSI 34P3210 programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks^2 + 17.98016)/D(s)] \bullet An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \bullet (s/0.86133) \bullet Ad$$

Where D (s)=

$(s^2+1.68495s+1.31703)(s^2+1.54203s+2.95139)(s^2+1.14558s+5.37034)(s+0.86133)$, An and Ad are adjusted for a gain of 2 at fs = (2/3)fc.

Filter Operation

AC coupled differential signals from the AGC are applied to the FIP/FIN inputs of the filter. To improve settling time of the coupling capacitors, the FIP/FIN inputs are held in a Low-Z state for an additional 1 µs when the $\overline{WG}$ pin is brought high. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 9.09 kΩ external resistor connected from pin RX to ground.

Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC as follows:

$$FC = 29.57 \bullet (DACF)^2 + 29775 \bullet (DACF) - 37700(Hz)$$

where DACF = DMCR value

for $13 \le DACF \le 127$

The Data Mode Cutoff Register (DMCR) is used to determine the filter's 3 dB cutoff frequency. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

TABLE 1: 3 dB Cutoff frequency versus boost magnitude.

BOOST (dB)	FC (3 dB)	BOOST (dB)	FC (3 dB)
0	1.00	6	2.32
1	1.21	7	2.42
2	1.50	8	2.51
3	1.80	9	2.59
4	2.04	10	2.66
5	2.20		

Boost/Equalization Control

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost (dB) = 0 for FBCR = 0

Boost (dB) = 0.0776 • (FBCR) + 0.0023 • (DACF) + 0.000265(FBCR)^2 + 0.000129 • (FBCR) • (DACF) - 0.169 • (FBCR) / (DACF) - 0.47

for $32 \le FBCR \le 127$ and

$13 \le DACF \le 127$

For example, with the DACS set for maximum output (FBCR = 7 fH or 127) there will be 13 dB of boost added at the 3 dB frequency.

TIME BASE GENERATOR

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

In read, write and idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$\text{Reference Frequency} = ((M+1)/(N+1))\text{FREF}$$

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register (DRCR). This DAC, DACI, also sets the 1/2 symbol delay, VCO center frequency, and phase detector gain for the data synchronizer circuitry. The VCO center frequency is also a function of bit 7 in the DRCR. The formula for the VCO center frequency is shown below. When changing frequencies, the M and N registers must be loaded first, followed by the DRCR register. A frequency change is initiated only when the DRCR register has been changed.

$$\text{FVCO} = \left(\frac{12.5}{RR + .4}\right) \bullet S \bullet (42 \bullet \text{DACI} + 16.5)\ \text{kHz}$$

$S = 3$ if R4 Bit 7 = 1

$S = 1$ if R4 Bit 7 = 0

To optimize the TBG PLL performance over the wide range of M counter values available, provision is made to select one of the two external loop filters via serial port control.

There are three multiplexed FREF inputs; one is high speed, the other two have low Q filtering with a 20 kHz center frequency. The 20 kHz filter is followed by a comparator with 100 mV hysteresis. This allows the PLL to lock to a 20 kHz signal while reducing the possibility of noise interference. The normalized transfer function for the 20 kHz bandpass filter is: $S/(S^2 + S + 1)$. Bit 5 ($\overline{\text{HARMONIC}}$) of the Control A register allows the user to put the phase detector of the TBG into a harmonic mode when the 20 kHz FREF input is used. When Harmonic = 0 the rising edge of the 20 kHz FREF input enable the phase detector, and the falling edge is phase compared to the rising edge of the TBG VCO. This mode should only be entered when the TBG is already frequency locked. If the high speed FREF input is used then $\overline{\text{HARMONIC}}$ must be set to 1.

The TBG reference input is selected from the three FREF inputs by the table below.

Fref Select Bit 1 (R21 bit 7)	Fref Select Bit 0 (R21 bit 6)	Fref Input to TBG
0	X	Fref (8-20 MHz)
1	0	Fref 3 (20 kHz)
1	1	Fref 2 (20 kHz)

DATA SYNCHRONIZER

In the read mode, the data synchronizer performs sync field search and data synchronization. In the write mode, the circuit provides write precompensation or equalization. Data rate is established by the time base generator and the internal reference DACI controlled by the DR register. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/2 symbol delay.

Phase Locked Loop

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

Phase Locked Loop (continued)

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL. Provision for two loop filters is made with the selection control provided via the serial port.

Mode Control

The read gate (RG) and write gate ($\overline{WG}$) inputs control the device operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

Read Mode

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal $\overline{RD}$ input and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/2 symbol wide (TVCO) pulse whose leading edge is defined by the falling edge of $\overline{RD}$. A decode window is developed from the VCOR clock. Read data synchronization waveforms are shown in Figure 3.

Bit 5 of register 34 controls the input to the data synchronizer. If bit 5 = 1 then $\overline{RD}$ is the input to the synchronizer instead of $\overline{DRD}$. This mode can have advantages when the data contains consecutive ones. If this is the case and two of these pulses are shifted towards one another, the $\overline{DRD}$ one shot may mask the second pulse. For normal operation bit-5 of register 34 should be set low.

Preamble Search

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read data, $\overline{RD}$. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO Lock and Bit Sync Enable

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 3, in the Control B register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period, the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 11 transitions.

Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR).

Window Shift Control

Window shift magnitude is set by the value in the Window Shift Control Register (WSCR). The WSCR bits are as follows:

BIT	NAME	FUNCTION
0	WSO	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable
6	—	
7	—	

Window shift early and window shift late waveforms are shown in Figure 3. The window shift magnitude is set as a percentage of the full decode window, in 2.4% steps. This results in a window shift capability of ±36%. The tolerance of the window shift magnitude is ±20%. Window shift should be set during idle mode or write mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	Shift Magnitude
1	1	1	1	No shift
1	1	1	0	2.4% (minimum shift)
1	1	0	1	4.8%
1	1	0	0	7.2%
1	0	1	1	9.6%
1	0	1	0	12%
1	0	0	1	14.4%
1	0	0	0	16.8%
0	1	1	1	19.2%
0	1	1	0	21.6%
0	1	0	1	24%
0	1	0	0	26.4%
0	0	1	1	28.8%
0	0	1	0	31.2%
0	0	0	1	33.6%
0	0	0	0	36% (maximum shift)

Non Read Mode

In the non-read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

Write Mode

Write mode is entered by asserting the write gate ($\overline{WG}$) while the RG is held low. During write mode the VCO and the RRC are referenced to the internal time base generator signal.

Write Precompensation / Equalization

Write precompensation is provided to compensate for media bit shift caused by intersymbol interference. A description of how to set the magnitude of early and late write precomp is shown in the Write Precomp Control section.

When write precompensation is not being used the SSI 34P3210 allows the user to insert equalization timing pulses into the write data stream. These pulses provide some high frequency boost at the write side of the read/write interface and reduce the read flux amplitude differences between high and low density data signals.

Two pulses of width equal to 0.1T (T = write clock period) are inserted; the first pulse is delayed a time TWED from the rising clock edge, the second pulse is spaced TWES from the rising edge of the first. The dual pulses are inserted for every 0 not preceding a 1 in the data pattern. TWED is variable from 0.22T to 0.44T, using the write precomp early bits in the Write Precomp Control Register (WPCR). TWES is variable from 0.2T to 0.3T using the write precomp late bits in the WPCR. Write data showing the insertion of equalization pulses into the write data stream is shown in Figure 4.

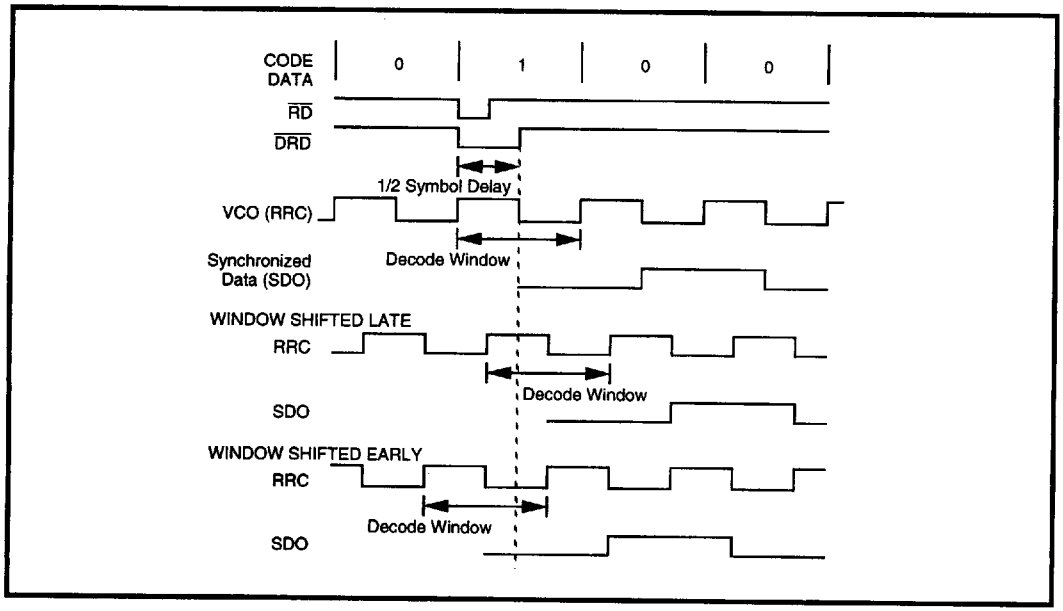


FIGURE 3: Read Data Synchronization Waveforms

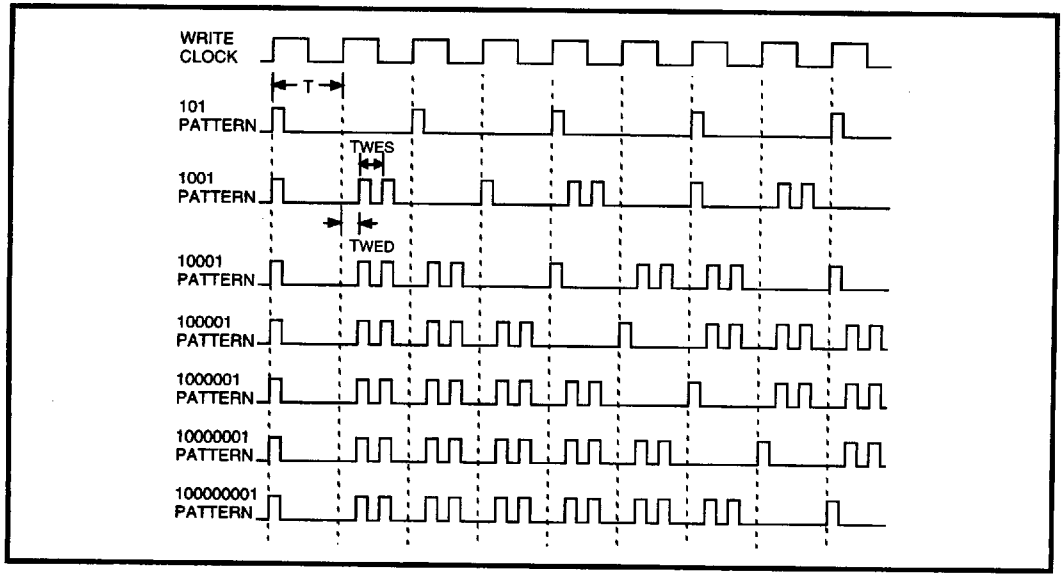


FIGURE 4: Write Data with Equalization Pulse Insertion

DATA SYNCHRONIZER (continued)

Write Precomp Control

Write precomp magnitude is set by the value in the Write Precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WE0}$	
1	$\overline{WE1}$	
2	$\overline{WE2}$	
3	WPE	Write Precomp Enable
4	$\overline{WL0}$	
5	$\overline{WL1}$	
6	$\overline{WL2}$	
7	WE	Write equalization select 1 = Write Equalization 0 = Write Precomp

WPE	WE	MODE
0	0	Bypass
1	0	Precomp
X	1	Equalization

The write precomp magnitude is calculated as:

$$TPE = n \bullet 0.045 \bullet TREF$$

where n = precomp magnitude scaling factor as shown below. TREF is the period of the reference frequency provided by the internal time base generator. Only the leading edge of the data is moved when a bit is precomped.

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	Precomp Magnitude Scaling Factor (n value)
1	1	1	No precomp
1	1	0	1X
1	0	1	2X
1	0	0	3X
0	1	1	4X
0	1	0	5X
0	0	1	6X
0	0	0	7X (maximum)

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	BIT N COMPENSATION
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude

Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

Write Equalization Enable

Write equalization is enabled when WE (R22 bit 7) is high.

Write Equalization Control

T_{WES} is variable from 0.2T to 0.3T in 7 equal steps using $\overline{WLX}$ (write precomp late) DAC control. T_{WED} is variable from 0.44T to 0.22T in 7 equal steps using $\overline{WEX}$ (write precomp early) DAC control.

$$T_{WES} = [.2 + n \bullet (.0143)]TREF \quad 0 \le n \le 7$$

$$T_{WED} = [.44 - n \bullet (.0314)]TREF \quad 0 \le n \le 7$$

n = equalization magnitude scaling factor as shown in the Write Precomp Control section.

Direct Write Function

The SSI 34P3210 includes a Direct Write (DW) function that allows the EWDI data to bypass the write precomp circuitry. When bits D3 and D7 in the write precomp register are set to 0, the data applied to EWDI will bypass the write precomp and directly control the EWDO output buffer. This allows the user to perform DC erase and media tests.

Write DAC

A 6-bit write (DACW) is provided for current reference for the R/W chip. This is enabled by setting bit 1 of register 2 (PDCR), and the write current is seen at DACOUT. The output current sink is programmable from 0 to 2.52 mA as follows:

$$IWRITE = 2.52\ mA \bullet DACW / 63$$

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DATA SYNCHRONIZER (continued)

Head Select

Two serial port bits, bits 6 and 7 of R2 (PDCR) are buffered and provided as CMOS outputs. These outputs can be used for head select or other customized control logic.

Operating Modes and Control

The SSI 34P3210 has several operating modes that support read, write, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate ($\overline{WG}$), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

External Mode Control

All operating modes of the device are controlled by driving the read gate (RG), write gate ($\overline{WG}$), and $\overline{PWRON}$ pins with CMOS compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 34P3210 is controlled by the read gate (RG) and write gate ($\overline{WG}$) pins. When RG is high and $\overline{WG}$ is high the device is in read mode. When $\overline{WG}$ is low and RG is low the device is in write mode. If the RG is low and $\overline{WG}$ is high the device will be in idle mode.

TABLE 2: Mode Control Table

CONTROL LINE				DAC CONTROL			
$\overline{PWRON}$	RG	$\overline{WG}$	DEVICE MODE	VTH	FC	BOOST	HYSTERESIS
1	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	**WRITE MODE:** The pulse detector is inactive. The synchronizer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base.	DR	DR	DR	DR
0	1	1	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. RDIO is inactive.	DR	DR	DR	DR
0	0	1	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.	DR	DR	DR	DR

DAC Control Key: DR = Data Register, off = disabled

REGISTER DESCRIPTION

CONTROL REGISTERS

Control registers CAR and CBR allow the user to configure the SSI 34P3210 test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the time base generator and test point output selection. CBR controls DAC test points and functions of the data synchronizer. The bits of the CA and CB registers are defined as follows:

Control Register CAR:

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLT sources current, $\overline{\text{TFLT}}$ sinks Current)
2	DT	Pump Down (TFLT sinks current, $\overline{\text{TFLT}}$ sources Current)
3	TBG KD	Change phase detector gain by a factor of 3
4	BYPT	Bypass Time Base Generator Circuit Function
5	HRMEN	Enable Harmonic mode
6	TBG F0	Select TBG PLL loop filter 0
7	TBG F1	Select TBG PLL loop filter 1

Control Register CBR:

0	EPDD	Enable Phase Detector (Data synchronizer)
1	UD	Pump Up (DFLT sources current, $\overline{\text{DFLT}}$ sinks current)
2	DD	Pump Down (DFLT sinks current, $\overline{\text{DFLT}}$ sources current)
3	GS	Enable Phase Detector Gain Switching
4	DST	DS Test Mode
5	RDIO	Select input (logic 1) or output (logic 0)
6	DSF0	Select DS PLL Loop Filter 0
7	DSF1	Select DS PLL Loop Filter 1

CONTROL REGISTERS (continued)

TABLE 3: Multiplexed Test Point Signal Selection

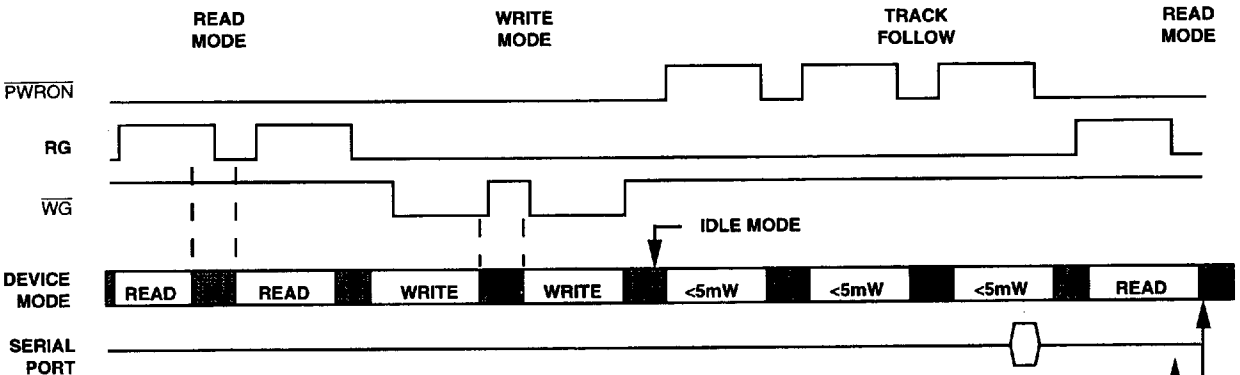
MTPE	TMS1	TMS0	MTP1	MTP2	MTP3	MTP4
1	X	X	OFF	OFF	OFF	OFF
0	0	0	VCOREF	$\overline{\text{VCOREF}}$	DRD	$\overline{\text{DRD}}$
0	0	1	SET	RESET	DSREF	AFREF
0	1	0	PDQ	$\overline{\text{PDQ}}$	$\overline{\text{PUQ}}$	PUQ
0	1	1	RD	SET	NCTR	MCTR

VCOREF = Data synchronizer VCO reference clock
DSREF = Output of the time base generator
MCTR = M counter output of the time base generator
DOUT = Output of the pulse qualifier data comparators
RD = Read MO data output from the pulse qualifier
PDQ/PUQ = Data synchronizer phase detector monitor points
NCTR = N counter output of the time base generator
RESET = Output of the negative threshold comparator
SET = Output of the positive threshold comparator
AFREF = Analog output of FREF2, FREF3

TABLE 4: DACOUT Signal Selection

Write DAC	TDAC1	TDAC0	DAC MONITORED
1	0	0	Filter DACs
1	0	1	Qualifier threshold DAC (VTH)
1	1	0	Window shift DAC
1	1	1	Write precomp DAC
0	X	X	Write current DAC

WDACE = D1 bit of Register 2



NOTES:

1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5 µs for the DAC.

FIGURE 5: Power Control Timing

CONTROL REGISTERS (continued)

Power Down Control

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into sleep mode (<5 mW) and all circuits are powered down except the serial port and the power-on reset circuitry. This allows the user to program the serial port registers while still conserving power. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 5. To improve recovery time from the sleep mode, the $\overline{\text{WG}}$ pin should be asserted following power down to initiate the AGC recovery sequence. Power control timing is shown in Figure 5.

Bits 7 and 6 of the PDCR register control the speed of the CMOS output buffers according to the following table:

Bits 1	0	
0	0	= slow
0	1	= medium
1	0	= fast
1	1	= very fast

Power-On Reset

The SSI 34P3210 provides a power-on reset function. When VCC is increasing from zero and is between 0.8V and 4.5V, the PWR_OK pin will be a logic low. When VCC is greater than the 4.57V nominal trigger threshold, the PWR_OK pin switches high. When VCC is falling, the PWR_OK pin will switch to a logic low when VCC is less than 4.55V nominal.

SERIAL INTERFACE

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 34P3210. The serial port data transfer format is shown in Figure 6. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 5 provides register mapping information. The second byte contains the programming data. In read mode (R/W = 1) the SSI 34P3210 will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 7.

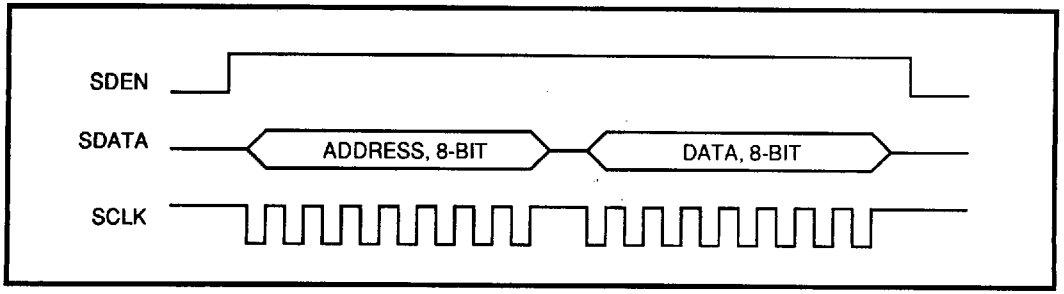


FIGURE 6: Serial Port Data Transfer Format

TABLE 5: Port Register Mapping

REG#	REGISTER NAME	ADDRESS A6						A0	R/W	DATA BIT MAP D7	D6	D5	D4	D3	D2	D1	D0
R2	POWER DOWN CONTROL REGISTER (PDCR)	0	0	0	0	0	1	0	0	I/O Speed Bit 1	I/O Speed Bit 0	MTPE 1=Disable 0=Enable	TBG 1=Disable 0=Enable	DATA SEP 1=Disable 0=Enable	FILTER 1=Disable 0=Enable	WRITE DAC 1=Disable 0=Enable	PD 1=Disable 0=Enable
R11	DATA MODE CUTOFF REGISTER (DMCR)	0	0	0	1	0	1	1	0	Set to 0	DACF BIT 6	DACF BIT 5	DACF BIT 4	DACF BIT 3	DACF BIT 2	DACF BIT 1	DACF BIT 0
R4	DATA RECOVERY CONTROL REGISTER (DRCR)	0	0	0	0	1	0	0	0	VCO FREQ 1=High 0=Low	DACI BIT 6	DACI BIT 5	DACI BIT 4	DACI BIT 3	DACI BIT 2	DACI BIT 1	DACI BIT 0
R5	N COUNTER CONTROL REGISTER (NCCR)	0	0	0	0	1	0	1	0	--	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
R10	DATA THRESHOLL CONTROL REGISTER(DTCR)	0	0	0	1	0	1	0	0	Data Qual 1=Dual 0=Hyst	DACT BIT 6	DACT BIT 5	DACT BIT 4	DACT BIT 3	DACT BIT 2	DACT BIT 1	DACT BIT 0
R3	FILTER BOOST CONTROL REGISTER (FBCR)	0	0	0	0	0	1	1	0	Set to 0	DACS BIT 5	DACS BIT 5	DACS BIT 5	DACS BIT 5	DACS BIT 2	DACS BIT 1	DACS BIT 0
R12	CONTROL B REGISTER (CBR)	0	0	0	1	1	0	0	0	Data Sync Loop Filter Select 1 1=Enable	Loop Filter Select 0 1=Enable	RDIO 1=Input 0=Output	DS TEST 1=Enable 0=Disable	GAIN SHIFT 1=ON 0=OFF	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1=Enable 0=Disable
R13	M COUNTER LSB CONTROL REGISTER (MCLCR)	0	0	0	1	1	0	1	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
R18	AGC GAIN CONTROL REGISTER (AGCR)	0	0	1	0	0	1	0	0	Set to 0	DACA BIT 6	DACA BIT 5	DACA BIT 4	DACA BIT 3	DACA BIT 2	DACA BIT 1	DACA BIT 0
R20	WINDOW SHIFT CONTROL REGISTER (WSCR)	0	0	1	0	1	0	0	0	Gated RDIO 0=Gated 1=On	WCLK from RDIO 1=Enable 0=Disable	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	WS3*	WS2*	WS1*	WS0*
R21	M COUNTER MSB CONTROL REGISTER (MCMCR)	0	0	1	0	1	1	1	0	FREF Select BIT 1	FREF Select BIT 0	TMS1	TMS0	TDAC1	TDAC0	M COUNT BIT 9	M COUNT BIT 8
R28	WRITE PRECOMP CONTROL REGISTER (WPCR)	0	0	1	1	1	0	0	0	Equalization 1=Enable 0=Disable	WL2*	WL1*	WL0*	WR PRCMP 1=ENABLE 0=DISABLE	WE2*	WE1*	WE0*
R29	CONTROL A REGISTER (CAR)	0	0	1	1	1	0	1	0	TBG Loop Filter Select 1 1=Enable	Loop Filter Select 0 1=Enable	HARMONIC 0-ENABLE	TBG Bypass 1=Enable 0=Disable	TBG KD 0 = 1 x KD 1 = 3 X KD	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=Enable 0=Disable
R36	WRITE CURRENT CONTROL REGISTER (WCCR)	0	1	0	0	1	0	0	0	Serial Port OUT1	Serial Port OUT0	DACW BIT 5	DACW BIT 4	DACW BIT 3	DACW BIT 2	DACW BIT 1	DACW BIT 0
R34	HYSTERESIS DECAY CONTROL REGISTER (HDCR)	0	1	0	0	0	1	0	0	--	--	DS REF 0=$\overline{DRD}$ 1=RD	Threshold 0=Fixed 1=Level	DACL BIT 3	DACL BIT 2	DACL BIT 1	DACL BIT 0

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data synchronizer PLL power supply pin
VPB	-	Time base generator PLL power supply pin
VPC	-	Pulse detector, serial port power supply pin
VPG	-	AGC, filter power supply pin
VCC1	-	Write data I/O power supply pin
VCC2	-	Read data I/O power supply pin
VCC3	-	RDIO I/O power supply pin
VNA	-	Data synchronizer PLL ground pin
VNB	-	Time base generator PLL ground pin
VNC	-	Pulse detector, serial port ground pin
VNG	-	AGC, filter ground pin
RTRN1	-	Write data I/O ground pin
RTRN2	-	Read data I/O ground pin
RTRN3	-	RDIO ground pin
RTRN4	-	Ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{\text{PWRON}}$	I	POWER ENABLE: CMOS compatible power control input. A low level CMOS input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry.
HOLD	I	HOLD CONTROL: CMOS compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP, FIN	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF, FREF2, FREF3	I	REFERENCE FREQUENCY INPUTS: Multiplexed reference inputs for the time base generator. These may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. Pin FREF has an internal pull down resistor.

INPUT PINS

NAME	TYPE	DESCRIPTION
EWDI	I	ENCODED WRITE INPUT: CMOS compatible write data input.
RG	I	READ GATE: CMOS compatible read gate input. A high level CMOS input selects the RD input and enables the read mode/address detect sequences. A low level selects the FREF input.
$\overline{WG}$	I	WRITE GATE: CMOS compatible write gate input. A low level CMOS input enables the write mode.

OUTPUT PINS

MTP1-4	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the MCTR MSB register. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: CMOS output pin. Read data output when RG is high.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
RDIO	O	READ DATA I/O: Bi-directional CMOS output / input pin. RDIO is an output when RG is low and the RDIO bit is enabled in the CBR. RDIO is an input when the RDIO bit is disabled in the CBR. The minimum RDIO input pulse width is 10 ns. The RG and pulse detector functions override the bit in the CBR. When RDIO is used as an input pin, the 1/2 symbol delay in the data synchronizer is made from the rising edge. When RDIO is an input and $\overline{WG}$ = 0 and WS bit 6 = 1, RDIO is used to clock the write precomp / equalization.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. When the Sync Bits are detected, RRC is synchronized to the Read Data. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
EWD0	O	WRITE DATA OUTPUT: Encoded write data CMOS output. When direct write is active EWDO is directly driven by EWDI.
SP1, SP0	O	CMOS buffered serial port bits from DACW register.
PWR_OK	O	POWER-ON RESET OK: Open collector output pin. This signal is a logic low when VCC is increasing from zero and is between 0.8V and 4.6V. When VCC is greater than 4.6V, PWR_OK is a logic high. When VCC is falling, PWR_OK will be a logic low once VCC has dropped to 4.5V or less.

PIN DESCRIPTION (continued)

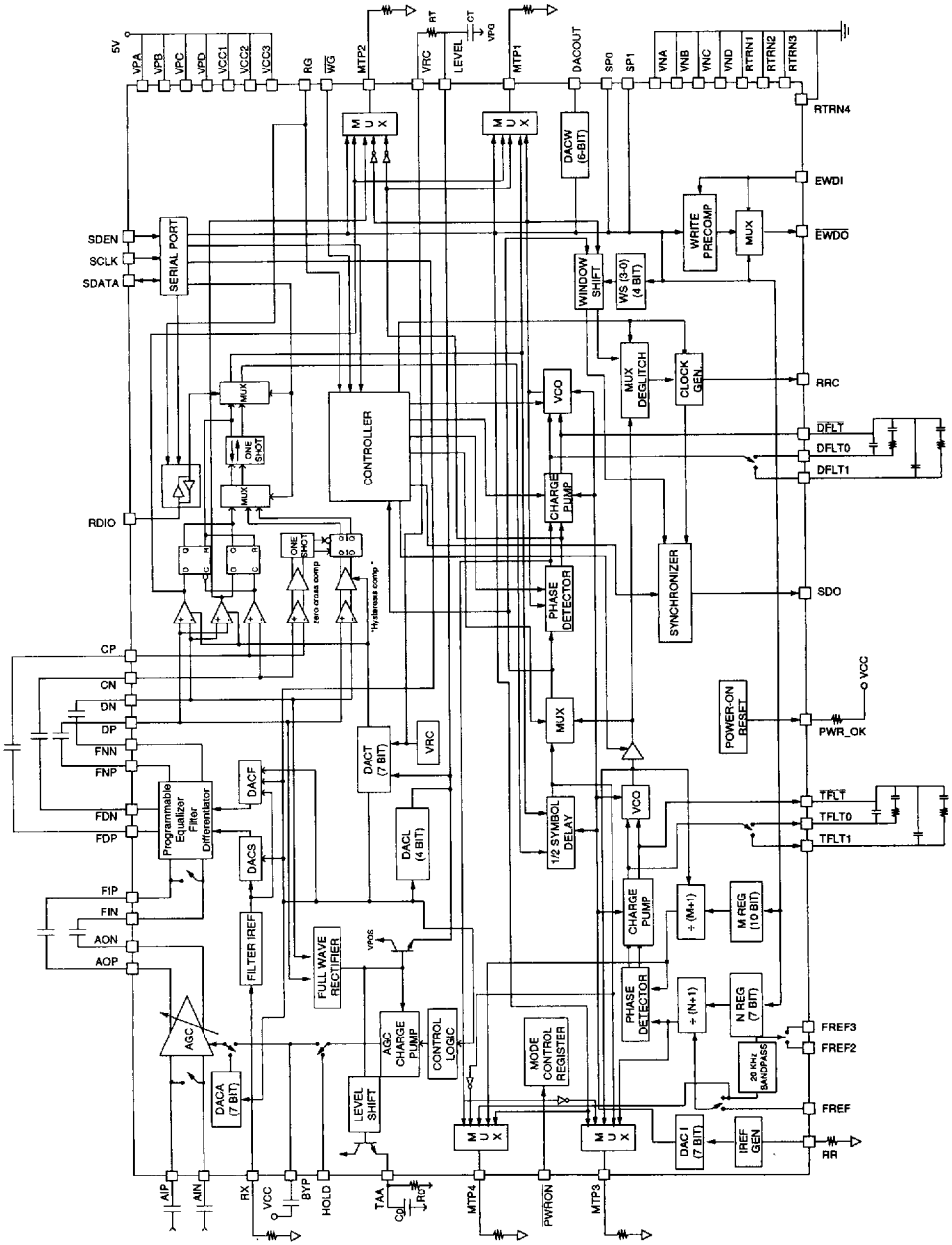
ANALOG PINS

NAME	TYPE	DESCRIPTION
BYP	-	The AGC read mode integration capacitor C_{BYP}, is connected between BYP and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT / WRITE DAC CURRENT SINK: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the Control B register (see Table 5). When the WRITE DAC is enabled in the power down register, this pin is used as the output sink.
TFLT0, TFLT1 $\overline{TFLT}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filters. Selection between TFLT0 and TFLT1 is done through the CA register (CAR).
DFLT0, DFLT1 $\overline{DFLT}$	-	PLL LOOP FILTER: These pins are the connection points for the data synchronizer loop filters. Selection between DFLT0 and DFLT1 is done through the CB register (CBR).
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VCC to set the hysteresis threshold time constant in conjunction with the level decay current DAC (R34).
TAA	-	An NPN emitter output that provides a full-wave rectified signal referenced to ground from the DP, DN inputs.
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data synchronizer and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 9.09 kΩ, 1% resistor is connected from this pin to VNG to establish a precise reference current for the filter.
VRC	-	Internal bandgap reference voltage, with respect to VCC

SERIAL PORT PINS

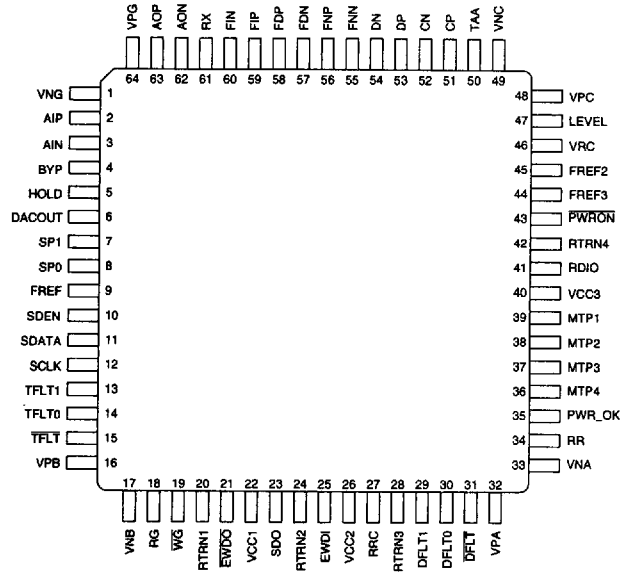
SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

APPLICATION DIAGRAM



SSI 34P3210
Read Channel for
High Density Floppy and Tape Storage

PACKAGE PIN DESIGNATIONS
(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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