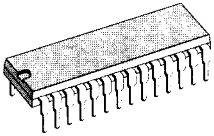
TDA7302

DIGITAL CONTROLLED STEREO AUDIO PROCESSOR

- INPUT AND OUTPUT PINS FOR EXTERNAL EQUALIZER
- THREE STEREO INPUT SOURCE SELECTION PLUS MONO INPUT
- TREBLE, BASS, VOLUME AND BALANCE CONTROL
- FOUR INDEPENDENT SPEAKER CONTROL (FRONT/REAR)
- SINGLE SUPPLY OPERATION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS
- VERY LOW NOISE AND VERY LOW DISTORTION
- POP FREE SWITCHING



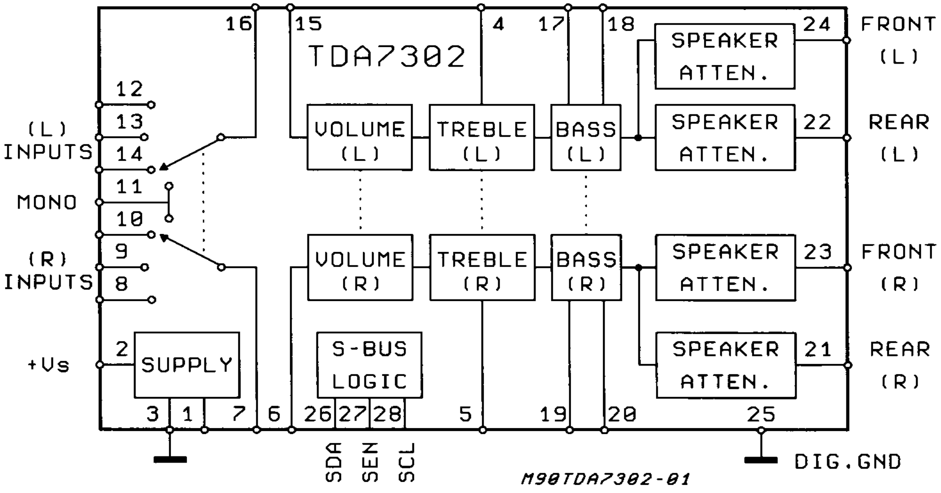
DIP28
ORDERING NUMBER: TDA7302

DESCRIPTION

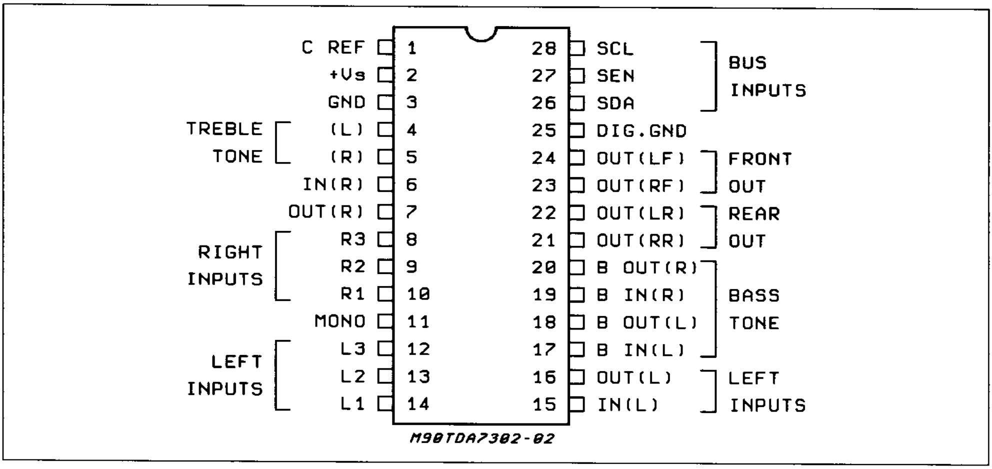
The TDA7302 is a volume, tone (bass and treble), balance (left/right) and fader (front/rear) processor for high quality audio applications in car radio and Hi-Fi system.

Control is accomplished by serial bus microprocessor interface.
The AC signal setting is obtained by resistor networks and analog switches combined with operational amplifiers.
The results are: low noise, low distortion and high dynamic range.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	14	V
P_{tot}	Total Power Dissipation T_{amb} = 25°C	2	W
T_{amb}	Operating Ambient Temperature Range	-40 to +85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	65	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, V_S = 10V, R_L = 10kΩ, R_g = 600Ω , f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		6	10	14	V
I_S	Supply Current		15	30	40	mA
SVR	Ripple Rejection	f = 300Hz to 10KHz	50	58		dB
INPUT SELECTORS						
R_i	Input Resistance		30	45		KΩ
$V_{IN\ max}$	Max. Input Signal	GV = 0dB d = 0.3%	1.5	2.2		Vrms
IN_S	Input Separation	f = 1KHz (2)	90	100		dB
		f = 10KHz (2)	70	80		dB
R_L	Output Load Resistance		5			KΩ
$V_{i\ (DC)}$	Input DC Voltage		3.5	4.3	5	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROLS						
R_{IN}	Input Resistance		5	10	20	KΩ
	Control Range			78		mA
G_{max}	Max Gain		8	10	12	dB
	Max Attenuation		64	68		dB
	Step Resolution			2	3	dB
	Attenuator Set Error	G_V = -50 to 10dB			2	dB
	Tracking Error				2	dB
SPEAKER ATTENUATORS						
	Control Range		35	38	41	dB
	Step Resolution			2	3	dB
	Attenuator Set Error				2	dB
	Tracking Error				2	dB
BASS AND TREBLE CONTROL (1)						
	Control Range			±15		dB
	Step Resolution			2.5	3.5	dB
AUDIO OUTPUT						
V_O	Max. Output Voltage	d = 0.3%	1.5	2.2		Vrms
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				1	nF
R_O	Output Resistance			70	150	Ω
$V_O(DC)$	DC Voltage Level		3	3.8	4.5	V
GENERAL						
e_{NO}	Output Noise	BW = 22Hz to 22KHz; G_v = 0dB		6	15	µV
		BW = 22Hz to 22KHz; Out atten. ≥ 20dB		3.5		µV
		G_v = 0dB Curve A		4		µV
S/N	Signal to Noise Ratio	All gain = 0dB V_O = 1Vrms BW = 22Hz to 22KHz		105		dB
d	Distortion	f = 1KHz V_O = 1V G_v = 0		0.01	0.1	%
	Frequency Response (-1dB)	G_v = 0 High Low	20		 20	KHz Hz
S_C	Channnel Separation left/right	f = 1KHz f = 10KHz	90 70	100 80		dB dB
BUS INPUTS						
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.4			V
V_O	Output Voltage SDA Acknowledge	I = 1.6mA			0.4	V
	Digital Input Current		-5		+5	µA

Notes:

(1) Bass and Treble response see attached diagram. The center frequency and quality of the resonance behaviour can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

(2) The selected input is grounded thru the 2.2µF capacitor.

Figure 1: Application Circuit

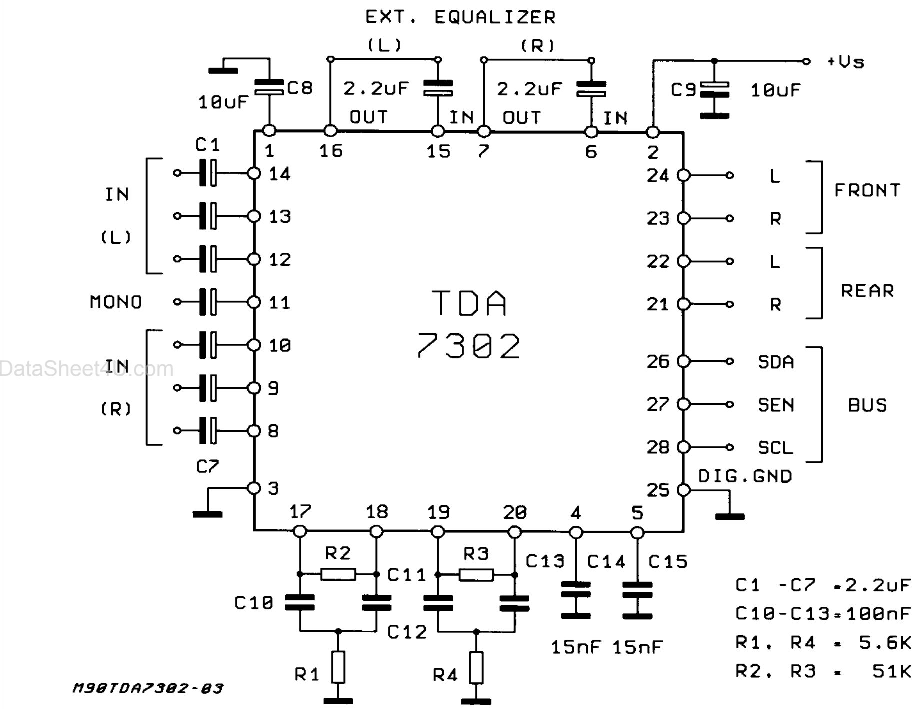


Figure 2: P.C. Board and Components Layout of the Fig.1 (1:1 scale)

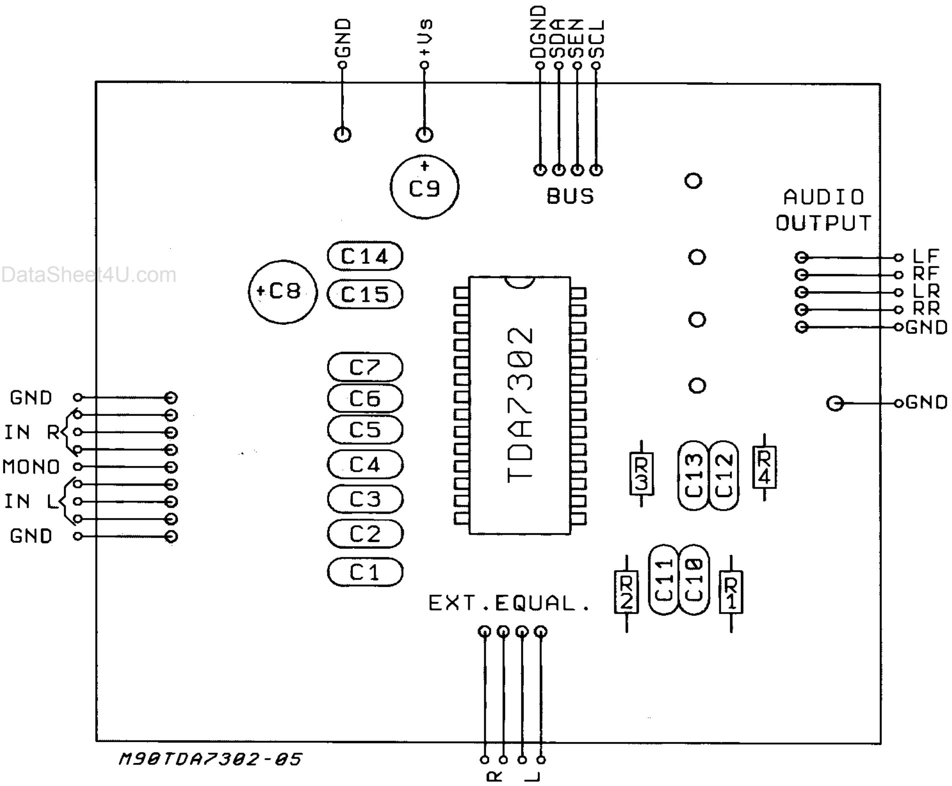


Figure 3: Total Output Noise vs. Volume Setting

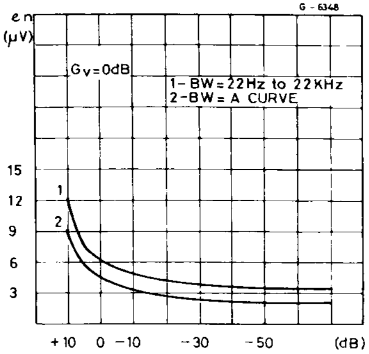


Figure 4: Signal to Noise Ratio vs. Volume Setting

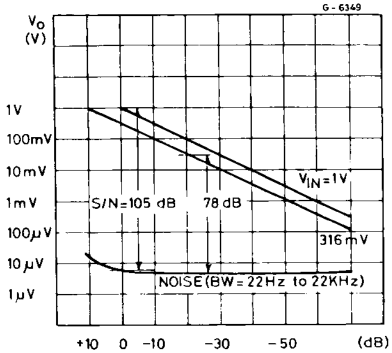


Figure 5: Distortion + Noise vs. Frequency

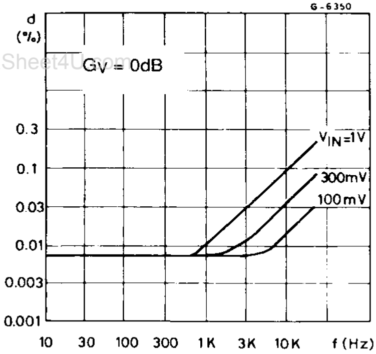


Figure 6: Distortion vs. Output Voltage

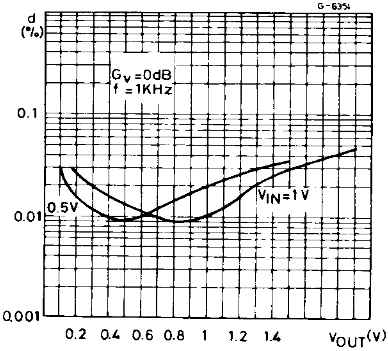


Figure 7: Distortion vs. Load Resistance

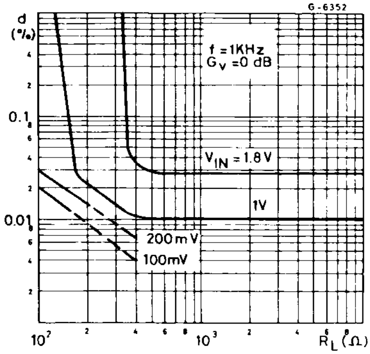


Figure 8: Channel Separation (L1 - R1) vs. Frequency

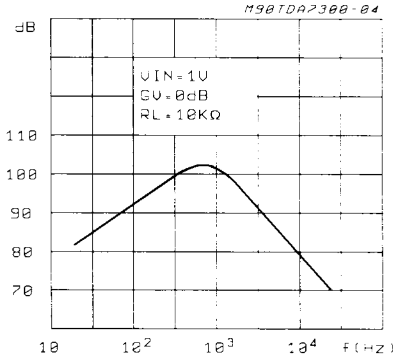


Figure 9: Input Separation (L1 - L2) vs. Frequency

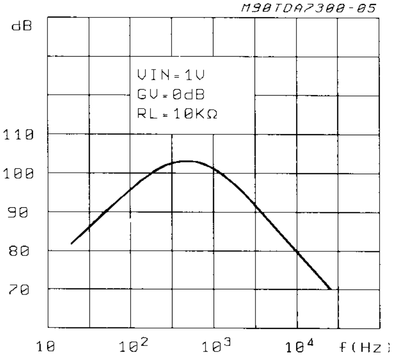


Figure 10: Supply Voltage Rejection vs. Frequency

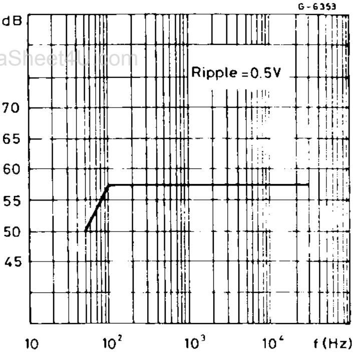
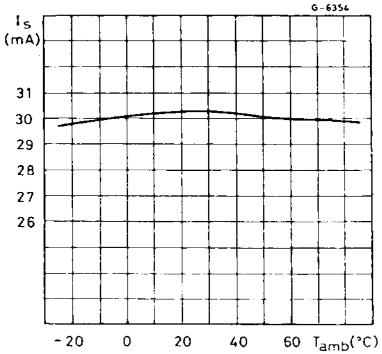


Figure 11: Quiescent Current vs. Temperature

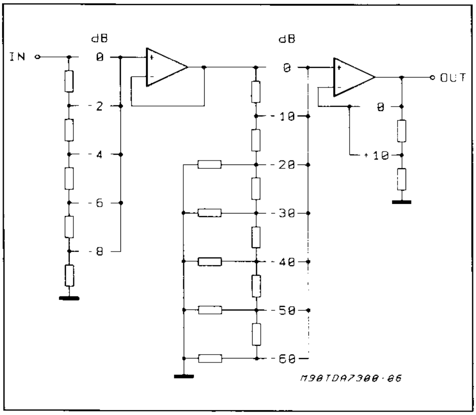


APPLICATION INFORMATION

Volume Control Concept

Traditional electronic volume control circuits use a multiplier technique with all the disadvantages of high noise and distortion.
The used concept, as shown in Fig. 12 with digital switched resistor dividers, provides extremely low noise and distortion. The multiplexing of the resistive dividers is realized with a multiple-input operational amplifier.

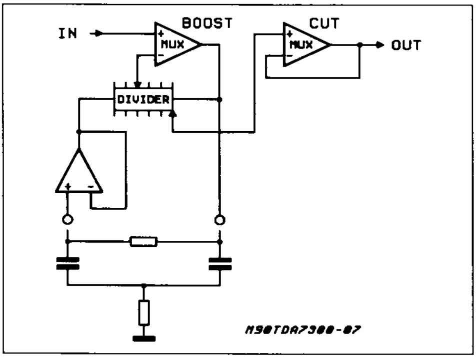
Figure 12: Volume Control



Bass and Treble Control

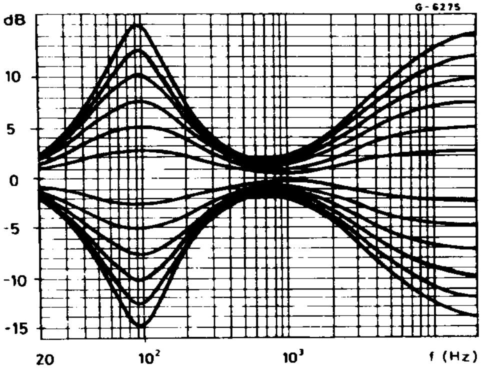
The principle operation of the bass control is shown in Fig. 12. The external filter together with the internal buffer allows a flexible filter design according to the different requirements in car radios. The function of the treble is similar to the bass.
A typical curve is shown in Fig.14.

Figure 13: Bass Control



APPLICATION INFORMATION (continued)

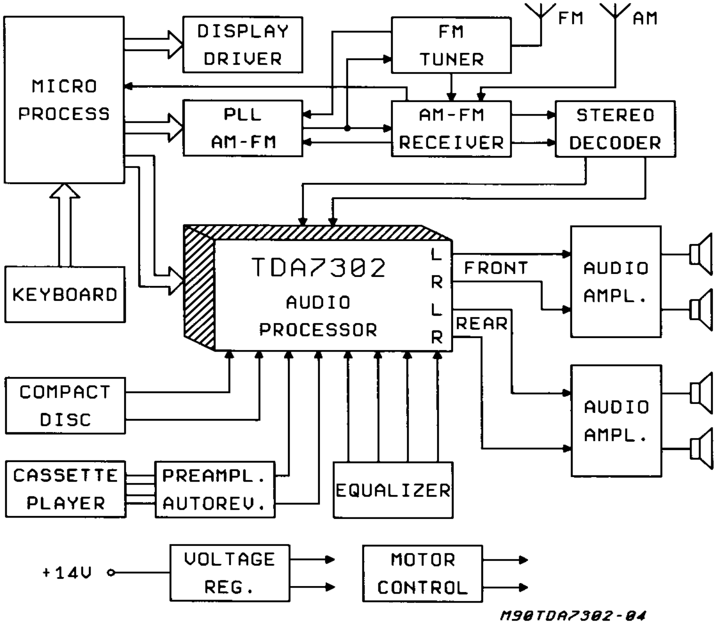
Figure 14: Typical Tone Response



Outputs

A special class-A output amplifier with a modulated sink current provides low distortion and ground compatibility with low current consumption.

Figure 15: Complete Car-Radio System using Digital Controlled Audio Processor



APPLICATION INFORMATION (continued)

SERIAL BUS INTERFACE

S-BUS Interface and I^{2}CBUS Compatibility

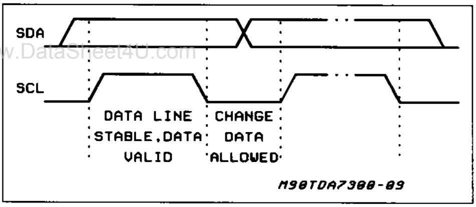
Data transmission from microprocessor to the TDA7302 and viceversa takes place thru the 3-wire S-BUS interface, consisting of the three lines SDA, SCL, SEN. If SDA and SEN inputs are short-circuited together, then the TDA7302 appears as a standard I^{2}CBUS slave.

According to I^{2}CBUS specification the S-BUS lines are connected to a positive supply voltage via pull-up resistors

Data Validity

As shown in fig. 16, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Figure 16: Data Validity on the I^{2}CBUS



Start and Stop Conditions

I^{2}CBUS:
as shown in fig.17 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

S-bus:
the start/stop conditions (points 1 and 6) are detected exclusively by a transition of the SEN line (1 → 0 / 0 →1) while the SCL line is at the HIGH level.

The SDA line is only allowed to change during the time the SCL line is low (points 2, 3, 4, 5). After the start information (point 1) the SEN line returns to the HIGH level and remains unchanged for all the time the transmission is performed.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (μP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 18). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Figure 17: Timing Diagram of S-BUS and I^{2}CBUS

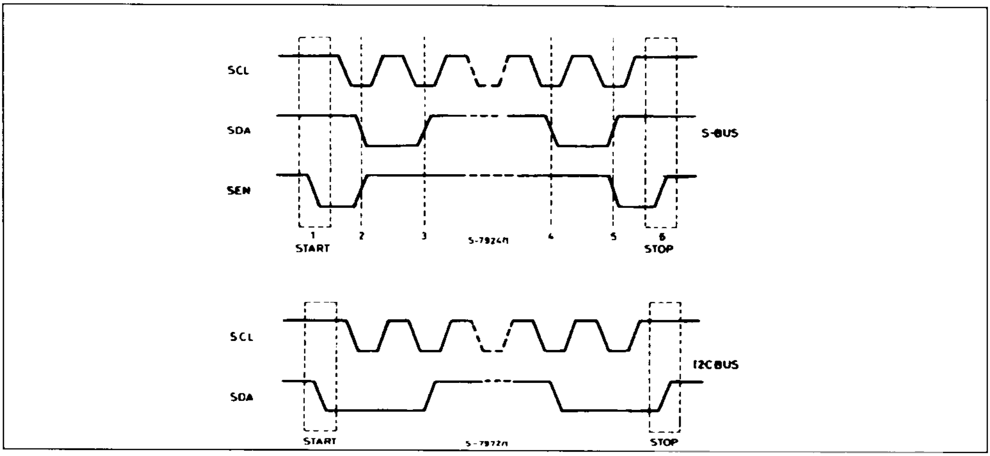
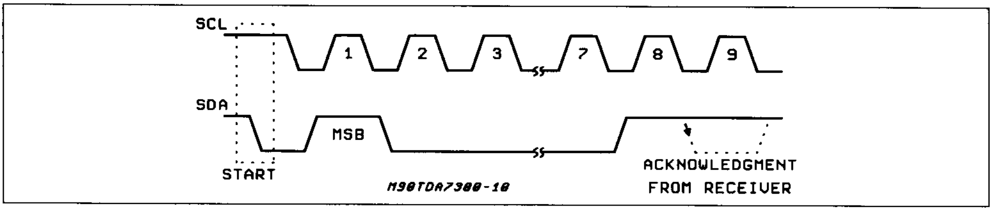


Figure 18: Acknowledge on the I^{2}CBUS



Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simplier transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7302 address (the 8th bit of the byte must be 0). The TDA7302 must always acknowledge at the end of each transmitted byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)

TDA7302 ADDRESS

MSB first byte LSB MSB LSB MSB LSB

S	1	0	0	0	1	0	0	0	ACK				DATA				ACK				DATA				ACK	P

Data Transferred (N-bytes + Acknowledge)

ACK = Acknowledge
S = Start
P = Stop

MAX CLOCK SPEED 100kbits/s

SOFTWARE SPECIFICATION

Chip address (TDA7302 address)

1	0	0	0	1	0	0	0
MSB							LSB

DATA BYTES

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	X	X	S2	S1	S0	Audio switch
0	1	1	0	C3	C2	C1	C0	Bass control
0	1	1	1	C3	C2	C1	C0	Treble control

X = don't care
Ax = 2dB steps
Bx = 10dB steps
Cx = 2.5dB steps

Status after power-on reset

STATUS AFTER POWER-ON-RESET

Volume	– 68 dB
Speaker	– 38 dB
Audio Switch	Mono
Bass	+ 2.5 dB
Treble	+ 2.5 dB

SOFTWARE SPECIFICATION (continued)
DATA BYTES (detailed description)

VOLUME

MSB							**LSB**	
0	0	B2	B1	B0	A2	A1	A0	Volume 2dB Steps
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
0	0	B2	B1	B0				Volume 10dB STEPS
		0	0	0				+10
		0	0	1				0
		0	1	0				-10
		0	1	1				-20
		1	0	0				-30
		1	0	1				-40
		1	1	0				-50
		1	1	1				-60

For example if you want setting the volume at -32dB the 8 bit string is: 0 0 1 0 0 0 0 1

SPEAKER ATTENUATORS

MSB							**LSB**	
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-2
					0	1	0	-4
					0	1	1	-6
					1	0	0	-8
					1	0	1	Not allowed
					1	1	0	Not allowed
					1	1	1	Not allowed
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30

For example attenuation of 24dB on speaker RF is given by: 1 0 1 1 0 0 1 0

SOFTWARE SPECIFICATION (continued)

AUDIO SWITCH - Select the input Channel to Activate

MSB							**LSB**	
0	1	0	X	X	S2	S1	S0	Audio Switch
			X	X	0	0	0	Stereo 1
			X	X	0	0	1	Stereo 2
			X	X	0	1	0	Stereo 3
			X	X	0	1	1	Mute Input
			X	X	1	0	0	Mono
			X	X	1	0	1	Not Allowed
			X	X	1	1	0	Not Allowed
			X	X	1	1	1	Not Allowed

X = don't care

For example to set the stereo 2 channel the 8 bit string must be: 0 1 0 0 0 0 0 1

BASS AND TREBLE - Control Range of ± 15 dB (boost and cut) Steps of 2.5 dB

0 **0**	**1** **1**	**1** **1**	**0** **1**	**C3** **C3**	**C2** **C2**	**C1** **C1**	**C0** **C0**	**Bass** **Treble**
				0	0	0	0	– 15
				0	0	0	1	– 15
				0	0	1	0	– 12.5
				0	0	1	1	– 10
				0	1	0	0	– 7.5
				0	1	0	1	– 5
				0	1	1	0	– 2.5
				0	1	1	1	– 0
				1	1	1	1	+ 0
				1	1	1	0	+ 2.5
				1	1	0	1	+ 5
				1	1	0	0	+ 7.5
				1	0	1	1	+ 10
				1	0	1	0	+ 12.5
				1	0	0	1	+ 15
				1	0	0	0	+ 15

C3 = Sign

For example Bass at -12.5dB is obtained by the following 8 bit string: 0 1 1 0 0 0 1 0

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