27HC1616

256K (16K x 16) High-Speed CMOS EPROM

FEATURES

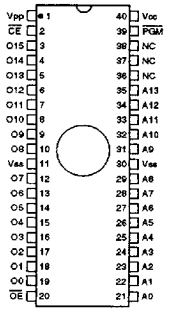
- 16 bit configuration
- High speed performance
  - 55 ns access time available
- CMOS Technology for low power consumption
  - 90 mA Active current
  - 50 mA Standby current
- Worldwide architecture offers space saving over Bytewide memories
- Organized 16K x 16: JEDEC standard pinouts
  - 40-Pin ceramic dual in line package
  - 44-Pin ceramic leadless chip carrier
- Temperature range available:
  - Commercial: 0°C to +70°C
  - Industrial: -40°C to +85°C

DESCRIPTION

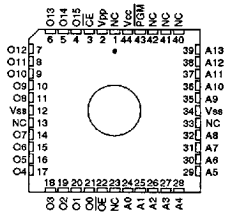
The Microchip Technology Inc. 27HC1616 is a CMOS 16K x 16 (256K) Programmable Read Only Memory. The device operates at Bipolar PROM speeds but uses far less current than any Bipolar PROM. The 27HC1616 is an excellent choice for any application requiring blazing speeds and low power consumption. The word wide (16 bit) architecture can replace two 8 bit EPROMS in any 16 bit application saving valuable printed circuit space and components costs. Typical applications for the 27HC1616 include automotive systems control, high speed modems, digital signal processing, or any application that uses the 80386, 68030, 29000, etc. high performance microprocessors.

PACKAGE TYPE

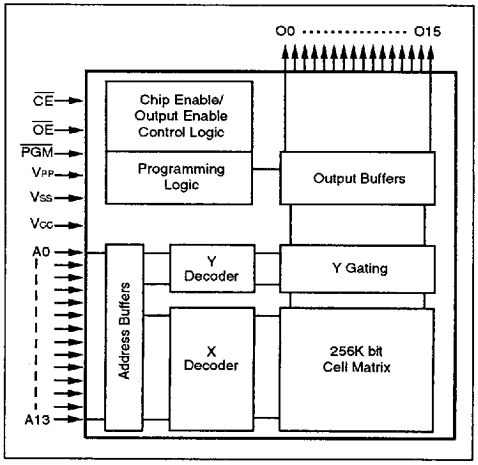
DIP



LCC



BLOCK DIAGRAM



7

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC} and input voltages w.r.t. V_{SS} ..... -0.6V to +7.25V

V_{PP} voltage w.r.t. V_{SS} during programming ..... -0.6V to +14.0V

Voltage on A9 w.r.t. V_{SS} ..... -0.6V to +13.5V

Output voltage w.r.t. V_{SS} ..... -0.6V to V_{CC} +1.0V

Temperature under bias ..... -65°C to +125°C

Storage temperature ..... -65°C to +150°C

ESD protection on all pins ..... 2 KV

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PIN FUNCTION TABLE

Name	Function
A0-A13	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
PGM	Program Enable
V_{PP}	Programming Voltage
O0 - O15	Data Output
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection; No Internal Connection

TABLE 1-2: READ OPERATION DC CHARACTERISTICS

V_{CC} = +5V ±10%
Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part	Status	Symbol	Min.	Max.	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	V_{IH} V_{IL}	2.0 -0.1	V_{CC}+1 0.8	V V	
Input Leakage	all	—	I_{LI}	-10	10	µA	V_{IN} = -0.1 to V_{CC} + 1.0V
Output Voltages	all	Logic "1" Logic "0"	V_{OH} V_{OL}	2.4	 0.45	V V	I_{OH} = - 2 mA I_{OL} = 8 mA
Output Leakage	all	—	I_{LO}	-10	10	µA	V_{OUT} = -0.1V to V_{CC} + 0.1V
Input Capacitance	all	—	C_{IN}	—	6	pF	V_{IN} = 0V; Tamb = 25°C; f = 1 MHz
Output Capacitance	all	—	C_{OUT}	—	12	pF	V_{OUT} = 0V; Tamb = 25°C; f = 1 MHz
Power Supply Current, Active	all	TTL input	I_{CC}	—	90	mA	V_{CC} = 5.5V; V_{PP} = V_{CC} f = 2 MHz; $\overline{OE}$ = $\overline{CE}$ = V_{IL}; I_{OUT} = 0 mA; V_{IL} = -0.1 to 0.8V; V_{IH} = 2.0 to V_{CC}; Note 1
Power Supply Current, Standby	all	—	I_{CC}	—	50	mA	
I_{PP} Read Current V_{PP} Read Voltage	all all	Read Mode Read Mode	I_{PP} V_{PP}	 V_{CC}-0.7	100 V_{CC}	µA V	V_{PP} = 5.5V Note 2

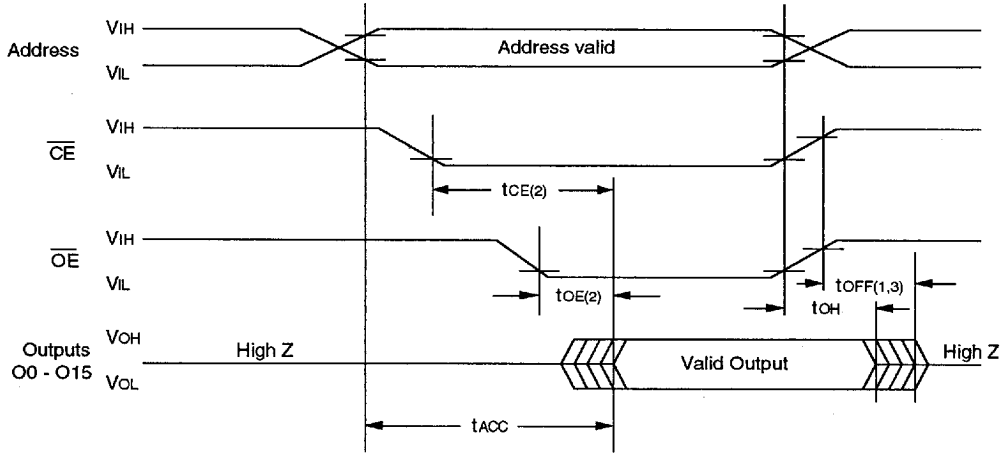
Note 1: Active current increases 2 mA per MHz up to operating frequency.
Note 2: V_{CC} must be supplied simultaneously or before V_{PP} and be removed simultaneously or after V_{PP}.

TABLE 1-3: READ OPERATION AC CHARACTERISTICS

AC Testing Waveform: V_{IH} = 3.0V and V_{IL} = 0.0V; V_{OH} = V_{OL} = 1.5V
Output Load: 1 TTL Load + 30 pF
Input Rise and Fall Times: 5 ns
Ambient Temperature: Commercial: Tamb = 0°C to +70°C
Industrial: Tamb = -40°C to +85°C

Parameter	Part	Sym	27HC1616-55		27HC1616-70		Units	Conditions
			Min	Max	Min	Max		
Address to Output Delay	all	t_{ACC}	—	55	—	70	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	all	t_{CE2}	—	35	—	45	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	all	t_{OE}	—	30	—	35	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{OE}$ to O/P High Impedance	all	t_{OFF}	0	20	0	25	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	all	t_{OH}	0	—	0	—	ns	

FIGURE 1-1: READ WAVEFORMS



Notes: (1) t_{OFF} is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}
(3) This parameter is sampled and is not 100% tested.

TABLE 1-4: PROGRAMMING DC CHARACTERISTICS

Ambient Temperature: Tamb = 25°C ± 5°C For VPP and VCC Voltages refer to Programming Algorithm						
Parameter	**Status**	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	VCC+1 0.8	V V	
Input Leakage	—	ILI	-10	10	µA	VIN = -0.1V to VCC + 1.0V
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4 —	 0.45	V V	IOH = -2 mA IOL = 8 mA
VCC Current, program & verify	—	ICC	—	90	mA	Note 1
VPP Current, program	—	IPP	—	50	mA	Note 1
A9 Product Identification	—	VH	11.5	12.5	V	

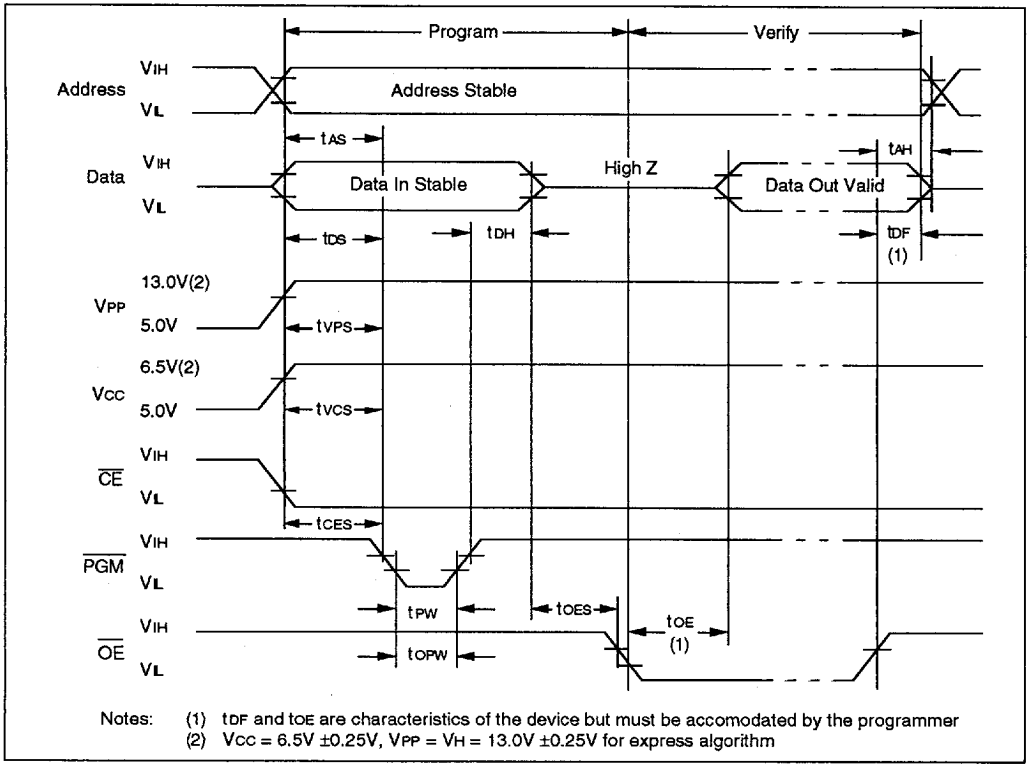
Note 1: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

TABLE 1-5: PROGRAMMING AC CHARACTERISTICS

for Program, Program Verify and Program Inhibit Modes	AC Testing Waveform: VIH=2.4V, VIL=0.45V; VOH=2.0V and VOL=0.8V Ambient Temperature: Tamb=25°C±5°C For VPP and VCC Voltages, refer to Programming Algorithm				
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Remarks**
Address Set-Up Time	tAS	2	—	µs	
Data Set-Up Time	tDS	2	—	µs	
Data Hold Time	tDH	2	—	µs	
Address Hold Time	tAH	0	—	µs	
Float Delay (2)	tDF	0	130	ns	
VCC Set-Up Time	tVCS	2	—	µs	
Program Pulse Width (1)	tPW	95	105	µs	100 µs typical
$\overline{CE}$ Set-Up Time	tCES	2	—	µs	
$\overline{OE}$ Set-Up Time	tOES	2	—	µs	
VPP Set-Up Time	tVPS	2	—	µs	
Data Valid from $\overline{OE}$	tOE	—	100	ns	

Note 1: For express algorithm, initial programming width tolerance is 100 µs ±5%.
Note 2: This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

FIGURE 1-2: PROGRAMMING WAVEFORMS



Notes: (1) tDF and tOE are characteristics of the device but must be accomodated by the programmer
(2) VCC = 6.5V ±0.25V, VPP = VH = 13.0V ±0.25V for express algorithm

TABLE 1-6: MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	VPP	A9	O0 - O7
Read	VIL	VIL	VIH	VCC	X	DOUT
Program	VIL	VIH	VIL	VH	X	DIN
Program Verify	VIH	VIL	VIH	VH	X	DOUT
Program Inhibit	VIH	X	X	VH	X	High Z
Standby	VIH	X	X	VCC	X	High Z
Output Disable	X	VIH	VIH	VCC	X	High Z
Identity	VIL	VIL	VIH	VCC	VH	Identity Code

X = Don't Care
VH = 12.0 ± 0.5V

2.0 FUNCTIONAL DESCRIPTION

The 27HC1616 has the following functional modes:

- Operation: The 27HC1616 can be activated for data read, be put in standby mode to lower its power consumption, or have the outputs disabled.
- Programming: To receive its permanent data, the 27HC1616 must be programmed. Both a program and program/verify procedure is available. The Express programming algorithm is recommended.

The programming equipment can automatically recognize the device type and manufacturer using the identity mode.

For the general characteristics in these operation and programming modes, refer to the table.

3.0 OPERATION

3.1 Read Mode

For timing and AC characteristics refer to the tables Read Waveforms and Read Operation AC Characteristics.

The 27HC1616's memory data is accessed when

- the chip is enabled by setting the $\overline{CE}$ pin low
- the data is gated to the output pins by setting the $\overline{OE}$ pin low

3.2 Standby Mode

The standby mode is entered when the $\overline{CE}$ pin is high, and the program mode is not defined. When these conditions are met, the supply current will drop from 90 mA to 50 mA.

3.3 Output Disable

This feature eliminates bus contention in multiple bus microprocessor systems. The outputs go to a high impedance when the $\overline{OE}$ pin is high, and the program mode is not defined.

3.4 Programming/Verification

The 27HC1616 has to be programmed, and afterward the programmed information verified. Before these operations, the Identity Code can be read to properly set up automated equipment. Multiple devices in parallel can be programmed using the programming and inhibit modes.

3.5 Programming Algorithm

The "Express" algorithm has been developed to improve programming through-put times in a production environment. Up to 10 pulses of 100 µs each are applied until the byte is verified. No overprogramming is required. A flowchart of this algorithm is shown in Figure 3-1.

Programming takes place when:

a) V_{CC} is brought to the proper level
b) V_{PP} is brought to the proper V_H level
c) the $\overline{OE}$ pin is high
d) the $\overline{CE}$ pin is low
e) the $\overline{PGM}$ pin is pulsed low

Since the erased state is "1" in the array, programming of "0" is required. The address of the memory location to be programmed is set via pins A0 - A13, and the data is presented to pins O0 - O15. When data and address are stable, a low going pulse on the $\overline{CE}$ line programs that memory location.

3.6 Verify

After the array has been programmed, it must be verified to make sure that all the bits have been correctly programmed. This mode is entered when all of the following conditions are met:

a) V_{CC} is at the proper level
b) V_{PP} is at the proper V_H level
c) the $\overline{OE}$ line is low
d) the $\overline{CE}$ pin is low, and
e) the $\overline{PGM}$ line is high.

3.7 Inhibit Mode

When Programming multiple devices in parallel with different data only $\overline{PGM}$ needs to be under separate control to each device. By pulsing the $\overline{PGM}$ line low on a particular device, that device will be programmed, and all other devices with corresponding $\overline{PGM}$ or $\overline{CE}$ held high will not be programmed with the data although address and data are available on their input pins.

3.8 Identity Mode

In this mode specific data is read from the device that identifies the manufacturer as Microchip Technology, and the device type. This mode is entered when pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ pins must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 - O7.

Pin →	Input	Output							
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	1	0	1	1	1	97

* Code subject to change

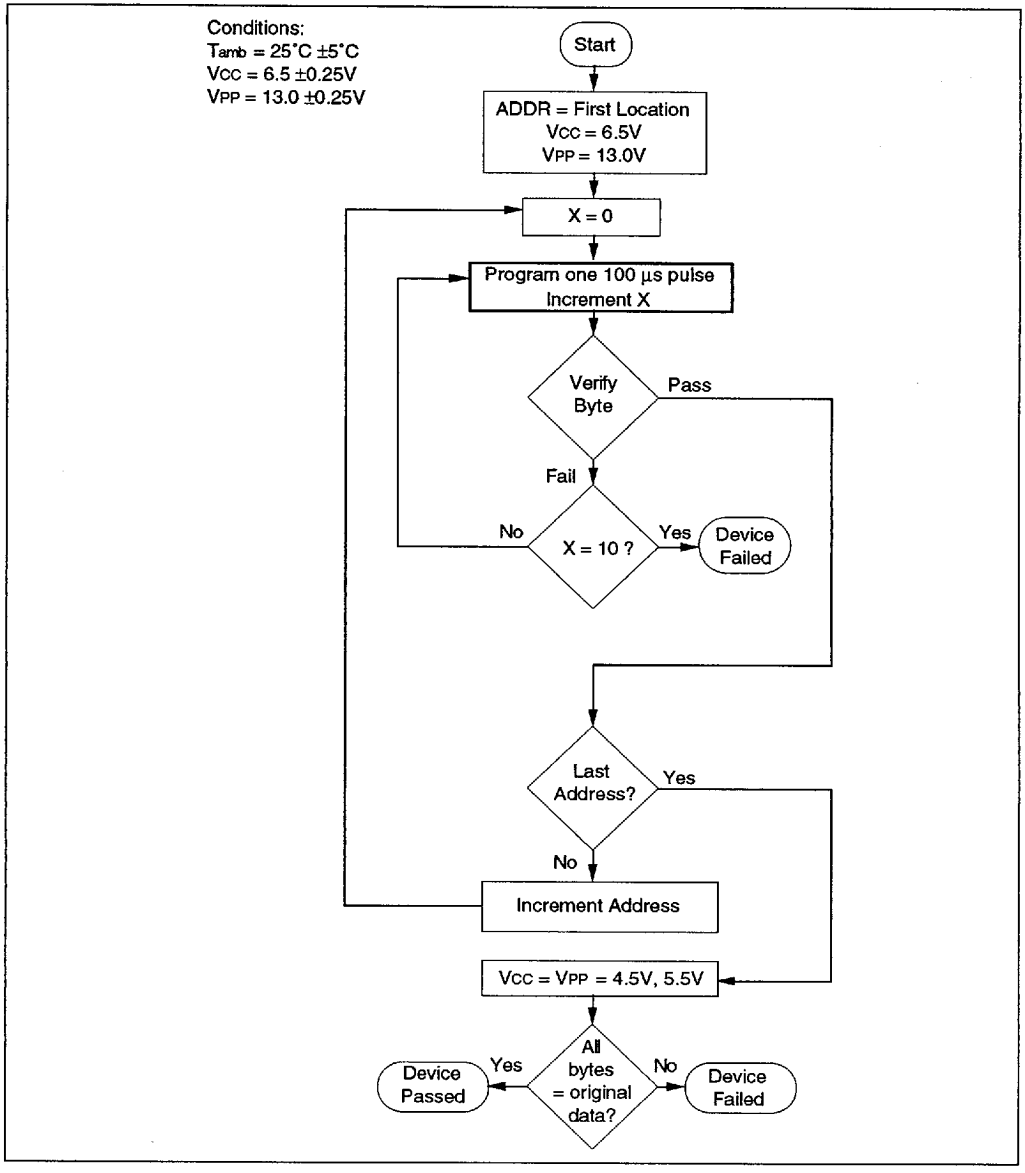
Note 1: O15 - O8 are 00 for the manufacturer and device type code.

3.9 Erasure

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all "1"s state as a result of being exposed to ultra-violet light at wavelengths ≤ 4000 Angstroms (Å). The recommended procedure is to expose the erasure window of device to a commercial UV source emitting at 2537Å with an intensity of 12,000µW/cm^2 at 1". The erasure time at that distance is about 15 to 20 minutes.

Note: Fluorescent lights and sunlight emit rays at the specified wavelengths. The erasure time is about 3 years or 1 week resp. in these cases. To prevent loss of data, an opaque label should be placed over the erasure window.

FIGURE 3-1: PROGRAMMING EXPRESS ALGORITHM



27HC1616 Product Identification System

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

27HC1616 - 55 I /P

Package:		J	CERDIP
		K	Ceramic Leadless Chip Carrier
Temperature Range:		-	0°C to +70°C
		I	–40°C to +85°C
Access Time:		55	55 ns
		70	70 ns
Device:	27HC1616		