

CXP80116

Description

80 pin QFP (Plastic)



Features

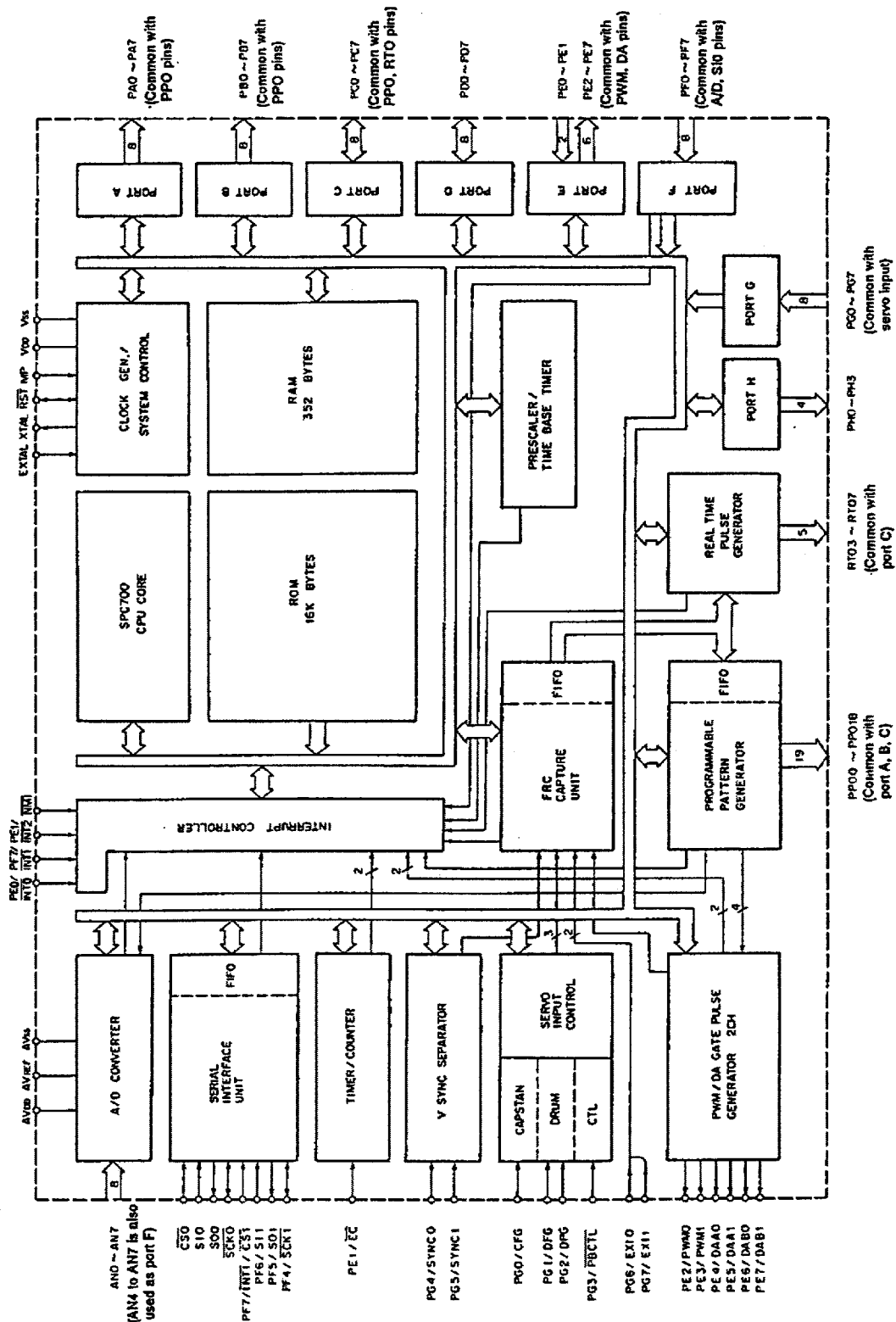
- A wide instruction set (213 instructions) which cover various types of data.
 - 16-bit arithmetic instruction/multiplication and division instructions/boolean bit operation instruction
- Minimum instruction cycle During operation 500ns/8MHz
- Incorporated ROM capacity 16Kbytes
- Incorporated RAM capacity 352bytes
- Enables to extend a memory (ROM, RAM) up to 64Kbytes
- Peripheral function
 - A/D converter 8-bit, 8-channel, successive approximation system
(Conversion time : 20 μ s)
 - Serial I/O Incorporated 8-bit and 8-stage FIFO for data
(1 to 8 bytes auto transfer)
 - Timer 8-bit timer, 8-bit timer/counter, 19-bit time base timer
 - High precision timing pattern generator PPG (19 pins) /RTG (5 pins)
 - PWM/DA gate output 12 bit, 2-channel
 - Servo input control Capstan FG, Drum FG/PG, CTL input
 - VSYNC separator
 - FRC capture unit Incorporated 22-bit and 6-stage FIFO
- Interruption 15 factors, 15 vectors, multi-interruption possible
- Standby mode SLEEP/STOP
- 3-type operation modes Single chip mode/Memory extension mode/Microprocessor mode
- Package 80-pin plastic QFP

Structure

Silicon gate CMOS IC

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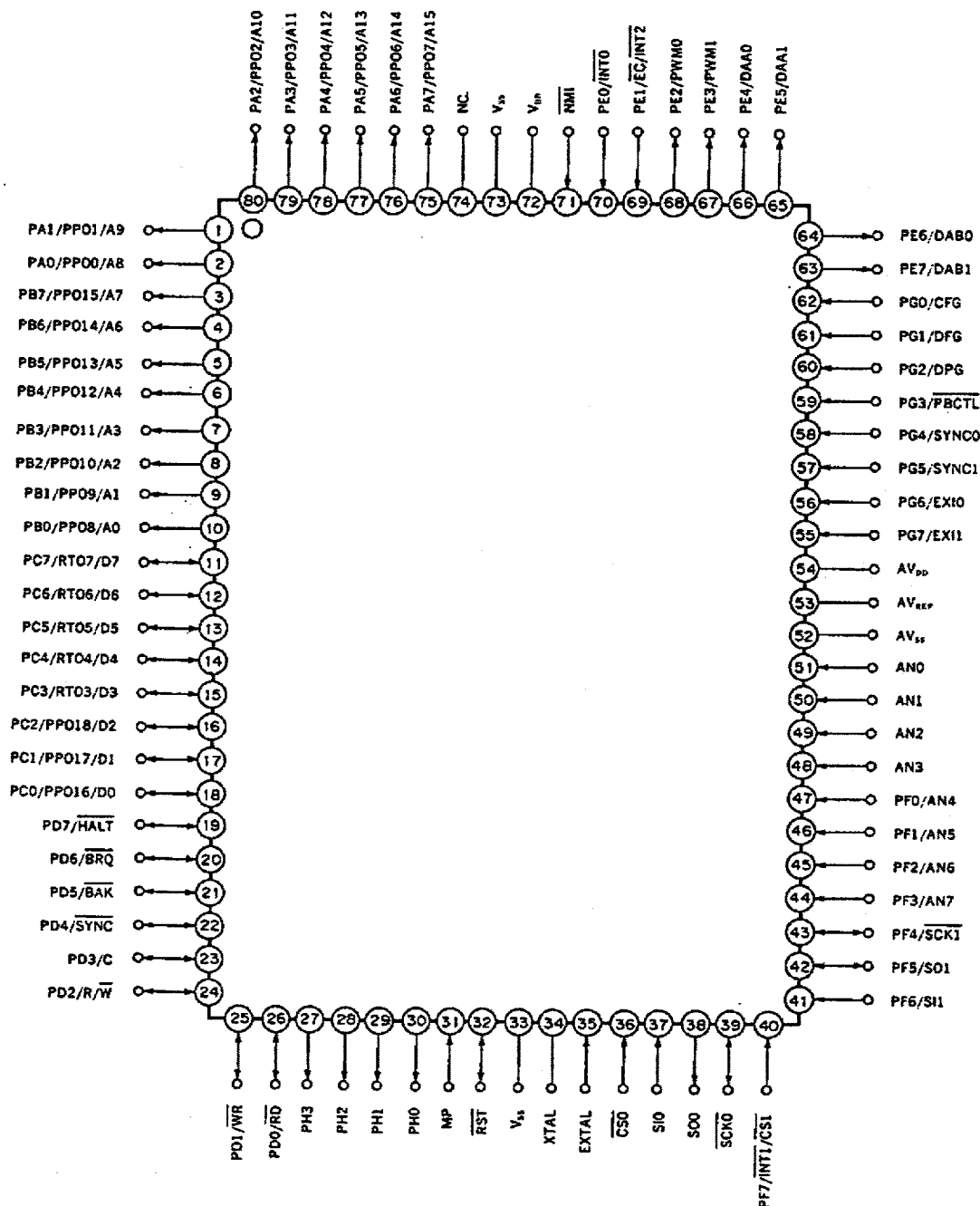
Block Diagram



Pin Configuration Diagram (Top View)

Note) 1) NC (pin 74) is always connected to V_{DD}.

2) V_{SS} (pins 33 and 73) are both connected to GND.



Pin Description

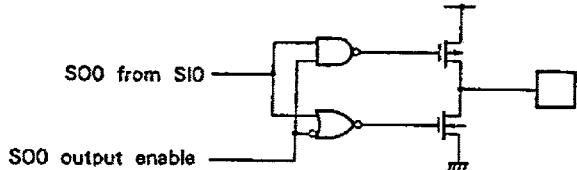
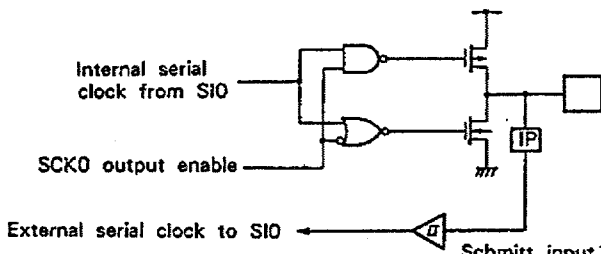
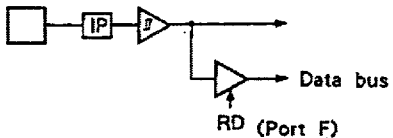
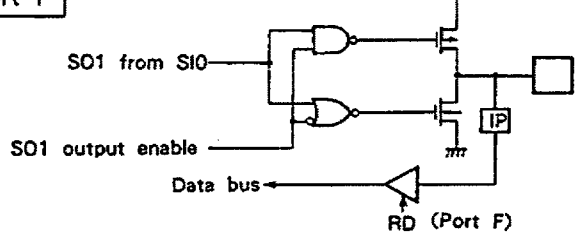
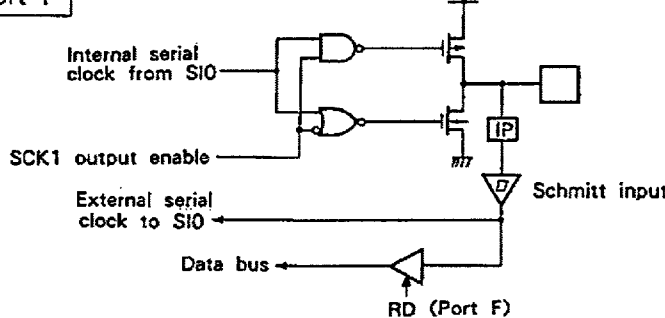
Symbol	I/O	Description		
PA0/PPO0 /A8 to PA7/PPO7 /A15	Output/ Real time Output/ Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. Functions as high precision real time pulse output port. (19 pins)	Functions as address bus for external memory in the memory extension mode or microprocessor mode. (16 pins)
PB0/PPO8 /A0 to PB7/ PPO15/A7	Output/ Real time Output/ Output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)		
PC0/ PPO16/D0 to PC2/ PPO18/D2	I/O/ Real time Output/ I/O	(Port C) 8-bit input/output port, enables to specify input/output by 4-bit unit.	Real time pulse generator (RTG) output. Functions as high precision real time pulse output port. (5 pins)	Functions as data bus for external memory in the memory extension mode or microprocessor mode. (8 pins)
PC3/RT03 /D3 to PC7/RT07 /D7	I/O/ Real time Output/ I/O	Data is gated with PPO or RTO contents by OR-gate and they are output. (8 pins)		
PD0/ $\overline{RD}$	I/O/Output	(Port D) 8-bit input/output port. Lower 4 bits can be specified as input/output by bit unit and upper 4 bits can be specified as input/output by 4-bit unit. Enables to drive 12mA sync current. (8 pins)	Strobe signal for external memory reading operation. Enabled when "L".	
PD1/ $\overline{WR}$	I/O/Output		Strobe signal for external memory writing operation. Enabled when "L".	
PD2/ $\overline{R/W}$	I/O/Output		"H" when CPU's machine cycle is in read cycle, "L" when in write cycle.	
PD3/ $\overline{C}$	I/O/Output		Timing signal output pin.	
PD4/ $\overline{SYNC}$	I/O/Output		"L" when CPU is in opcode fetch cycle.	
PD5/ $\overline{BAK}$	I/O/Output		"L" when CPU receives bus request ($\overline{BRQ}$), at the same time address output, data input/output, $\overline{RD}$, $\overline{WR}$ and $\overline{R/W}$ pins become high impedance state.	
PD6/ $\overline{BRQ}$	I/O/Output		Input pin to bus-request for CPU.	
PD7/ $\overline{HALT}$	I/O/Output		Input pin to stop CPU operation.	
PE0/ $\overline{INT0}$	Input	(Port E) 8-bit port. Lower 2 bits are input pins, upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.	
PE1/ $\overline{EC}/$ $\overline{INT2}$	Input		External event input pin for timer/counter.	Input pin to request external interruption. Active when falling edge.
PE2/PWM0	Output		PWM output pins. (2 pins)	
PE3/PWM1	Output			
PE4/DAA0	Output		DA gate pulse output pins. (4 pins)	
PE5/DAA1	Output			
PE6/DAB0	Output			
PE7/DAB1	Output			

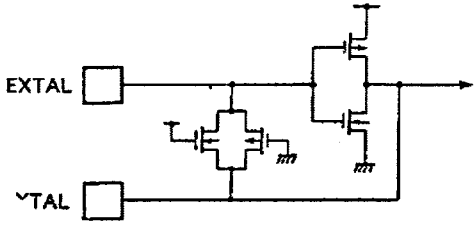
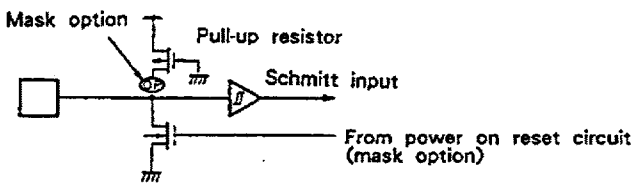
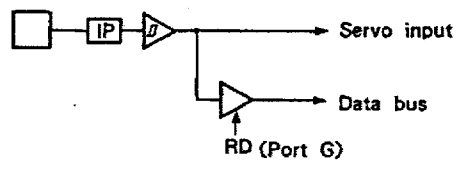
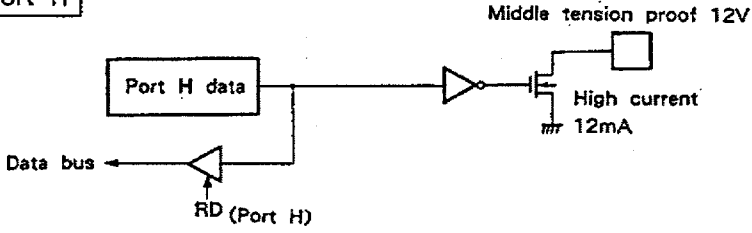
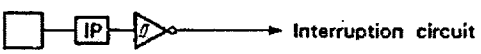
Symbol	I/O	Description
AN0 to AN3	Input	Analog input pins to A/D converter. (8 pins)
PF0/AN4 to PF3/AN7	Input	(Port F) 8-bit input port. Lower 4 bits also serve as standby release input pin. (8 pins)
PF4/SCK1	Input/I/O	
PF5/SO1	Input/Output	
PF6/SI1	Input	
PF7/INT1/CS1	Input	
SCK0	I/O	Serial clock input/output pin.
SO0	Output	Serial data output pin.
SI0	Input	Serial data input pin.
CS0	Input	Chip select input pin to serial interface.
PG0/CFG	Input	(Port G) 8-bit input port. (8 pins)
PG1/DFG	Input	
PG2/DPG	Input	
PG3/PBCTL	Input	
PG4/SYNC0	Input	
PG5/SYNC1	Input	
PG6/EXI0	Input	
PG7/EXI1	Input	
PH0 to PH3	Output	(Port H) 4-bit output port; Middle tension proof (12V) and high current (12mA), N-ch open drain output. (4 pins)
NMI	Input	Non-maskable interrupt request pin. Active during falling edge.
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and set XTAL pin to open.
XTAL	Output	
RST	I/O	System reset pin of active "L" level. RST pin is input/output pin, which output "L" level by incorporated power on reset function when power on. (Mask option)
MP	Input	Microprocessor mode input pin. When it is set to "H" level, it becomes microprocessor mode. When it is "L" level, single chip mode or memory extension mode is selected.
AVDD		Positive power supply pin of A/D converter.
AVREF	Input	Reference voltage input pin of A/D converter.
AVSS		GND pin of A/D converter.
VDD		Positive power supply pin.
VSS		GND pin. Connect both Vss pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PP00/A8 to PA7/PP07/A15 PB0/PP08/A0 to PB7/PP015/A7 16 pins	Port A Port B Address bus PPO data MPX Port A or Port B Data bus RD Output becomes active from high impedance by data writing to port register.	Hi-Z
PC0/PP016/D0 to PC2/PP018/D2 PC3/RT03/D3 to PC7/RT07/D7 8 pins	Port C Data bus PPO, RT0 data MPX Port C data Port C direction (Every 4 bits) Input protection circuit Buffer Data bus RD (Port C) Data bus RD	Hi-Z
PD0/RD PD1/WR PD2/R/W PD3/C PD4/SYNC PD5/BAK 6 pins	Port D Control output MPX Port D data Port D direction (Lower 4 bits are by bit unit, upper 4 bits are by 4-bit unit) High current 12mA IP Data bus RD (Port D)	Hi-Z
PD6/BRQ PD7/HALT 2 pins	Port D data Port D direction High current 12mA IP Data bus RD (Port D) Control input	Hi-Z

Pin	Circuit format	When reset
PE2/PWM0 PE3/PWM1 PE4/DAA0 PE5/DAA1 4 pins	Port E	Hi-Z
PE6/DAB0 PE7/DAB1 2 pins	Port E	H level
PE0/INT0 PE1/EC/INT2 2 pins	Port E	Hi-Z
AN0 to AN3 4 pins	Input multiplexer	Hi-Z
PF0/AN4 to PF3/AN7 4 pins	Port F	Hi-Z

Pin	Circuit format	When reset
$\overline{\text{CS0}}$ SIO 2 pins	Schmitt input 	Hi-Z
S00 1 pin		Hi-Z
$\overline{\text{SCK0}}$ 1 pin		Hi-Z
$\text{PF7}/\overline{\text{CS1}}/\overline{\text{INT1}}$ $\text{PF6}/\text{SI1}$ 2 pins	Port F Schmitt input 	Hi-Z
$\text{PF5}/\text{SO1}$ 1 pin	Port F 	Hi-Z
$\text{PF4}/\overline{\text{SCK1}}$ 1 pin	Port F 	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 - Shows the circuit composition during oscillation. - Feedback resistor is removed during stop.	Oscillation
$\overline{\text{RST}}$ 1 pin		L level
PG0/CFG PG1/DFG PG2/DPG PG3/PBCTL PG4/SYNC0 PG5/SYNC1 PG6/EXI0 PG7/EXI1 8 pins	Port G  (Note) For PG4/SYNC0, PG5/SYNC1, TTL schmitt input can be selected with the mask option.	Hi-Z
PH0 to PH3 4 pins	Port H 	Open
NMI 1 pin	Schmitt input 	Hi-Z
MP 1 pin		Hi-Z

Absolute Maximum Ratings

V_{SS} = 0V

Item	Symbol	Rating	Unit	Remarks
Power supply voltage	V _{DD}	-0.3 to +7.0	V	
	AV _{DD}	AV _{SS} to +7.0 ^{*1}	V	
	AV _{SS}	-0.3 to +0.3	V	
Input voltage	V _{IN}	-0.3 to +7.0 ^{*2}	V	
Output voltage	V _{OUT}	-0.3 to +7.0 ^{*2}	V	
Middle tension proof output voltage	V _{OUTP}	-0.3 to +15.0	V	PH pin
High level output current	I _{OH}	-5	mA	
High level total output current	Σ I _{OH}	-50	mA	Total of output pins
Low level output current	I _{OL}	15	mA	Other than high current output pins : per pin
	I _{OLC}	20	mA	High current port pin ^{*3} : per pin
Low level total output current	Σ I _{OL}	130	mA	Total of output pins
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operation conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

*1) AV_{DD} and V_{DD} should be set to a same voltage.

*2) V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V.

*3) The high current operation transistors are the N-CH transistors of the PD and PH ports.

Recommended Operating Condition

V_{SS} = 0V

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V _{DD}	4.5	5.5	V	Guaranteed range during operation
		2.5	5.5	V	Guaranteed data hold operation range during STOP
Analog power supply	AV _{DD}	4.5	5.5	V	^{*1}
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	^{*2}
	V _{IHS}	0.8V _{DD}	V _{DD}	V	C-MOS schmitt input ^{*3}
	V _{IHTS}	2.2	V _{DD}	V	TTL schmitt input ^{*4}
	V _{IHEX}	V _{DD} -0.4	V _{DD} +0.3	V	EXTAL pin ^{*5}
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	^{*2}
	V _{ILS}	0	0.2V _{DD}	V	C-MOS schmitt input ^{*3}
	V _{ILTS}	0	0.8	V	TTL schmitt input ^{*4}
	V _{ILEX}	-0.3	0.4	V	EXTAL pin ^{*5}
Operating temperature	T _{opr}	-20	+75	°C	

- *1) AV_{DD} and V_{DD} should be set to a same voltage.
 *2) Normal input port (each pin of PC, PD, PF0 to PF3 and PF5), MP pin
 *3) Each pin of $\overline{NMI}$, $\overline{CS0}$, $\overline{SI0}$, $\overline{SCK0}$, $\overline{RST}$, $\overline{PE0}/\overline{INT0}$, $\overline{PE1}/\overline{EC}/\overline{INT2}$, $\overline{PF4}/\overline{SCK1}$, $\overline{PF6}/\overline{SI1}$, $\overline{PF7}/\overline{INT1}/\overline{CS1}$ and PG (For PG4 and PG5, when CMOS schmitt input is selected with mask option)
 *4) Each pin of PG4 and PG5 (When TTL schmitt input is selected with mask option)
 *5) It specifies only when the external clock is input.

Electrical Characteristics

DC characteristics

 $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, $V_{SS} = 0\text{V}$

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PF4, PF5, $\overline{SO0}$, $\overline{SCK0}$, PH (V_{OL} only), $\overline{RST}^{*1}$ (V_{OL} only)	$V_{DD} = 4.5\text{V}$, $I_{OH} = -0.5\text{mA}$	4.0			V
			$V_{DD} = 4.5\text{V}$, $I_{OH} = -1.2\text{mA}$	3.5			V
Low level output voltage	V_{OL}	PA to PD, PE2 to PE7, PF4, PF5, $\overline{SO0}$, $\overline{SCK0}$, PH (V_{OL} only), $\overline{RST}^{*1}$ (V_{OL} only)	$V_{DD} = 4.5\text{V}$, $I_{OL} = 1.8\text{mA}$			0.4	V
			$V_{DD} = 4.5\text{V}$, $I_{OL} = 3.6\text{mA}$			0.6	V
		PD, PH	$V_{DD} = 4.5\text{V}$, $I_{OL} = 12.0\text{mA}$			1.5	V
Input current	I_{IHE}	EXTAL	$V_{DD} = 5.5\text{V}$, $V_{IH} = 5.5\text{V}$	0.5		40	μA
	I_{ILE}		$V_{DD} = 5.5\text{V}$, $V_{IL} = 0.4\text{V}$	-0.5		-40	μA
	I_{ILR}	$\overline{RST}^{*2}$	$V_{DD} = 5.5\text{V}$, $V_{IL} = 0.4\text{V}$	-1.5		-400	μA
I/O leakage current	I_{IZ}	PA to PG, AN0 to AN3, $\overline{CS0}$, $\overline{SI0}$, $\overline{SO0}$, $\overline{SCK0}$, $\overline{NMI}$, $\overline{RST}^{*2}$, MP	$V_{DD} = 5.5\text{V}$ $V_I = 0, 5.5\text{V}$			± 3	μA
Open drain output leakage current (N-CH Tr OFF in state)	I_{LOH}	PH	$V_{DD} = 5.5\text{V}$ $V_{OH} = 12\text{V}$			50	μA
Supply current	I_{DD}	V_{DD}	Operating mode (1/2 dividing clock) Crystal oscillation ($C1 = C2 = 15\text{pF}$) of 8MHz Entire output pins open		20	40	mA
	I_{DDSL}		SLEEP mode		5	15	mA
	I_{DDST}		STOP mode			3	μA
Input capacity	C_{IN}	Other than V_{DD} , V_{SS} , AV_{DD} , AV_{SS} pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1) $\overline{RST}$ pin specifies only when the power on reset circuit has been selected with mask option.

*2) $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

AC Characteristics

(1) Clock timing

 $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, $V_{DD} = 4.5\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_c	XTAL EXTAL	Fig. 1, Fig. 2	1	8	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 (External clock drive)	50		ns
System clock input rising and falling times	t_{CR} t_{CF}				200	ns
Event count clock input pulse width	t_{EL} t_{EH}	$\overline{\text{EC}}$	Fig. 3	t_{sys}^{*1} + 50		ns
Event count clock input rising and falling times	t_{ER} t_{EF}	$\overline{\text{EC}}$	Fig. 3		20	ms

*1) t_{sys} indicates three values according to the contents of the clock control register (address ; 00FFH) upper 2 bits (CPU clock selection).

$t_{\text{sys}} [\text{ns}] = 2000/f_c$ (Upper 2-bit = "00"), $4000/f_c$ (Upper 2-bit = "01"), $16000/f_c$ (Upper 2-bit = "11")

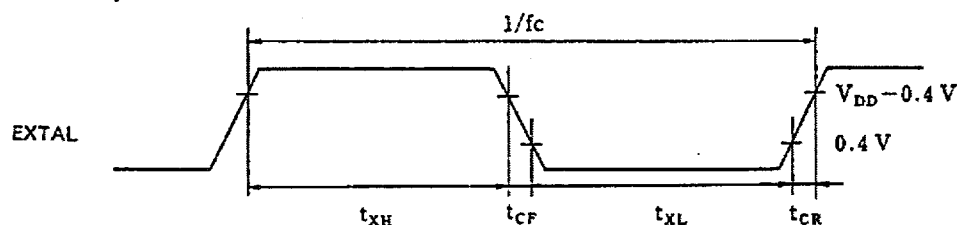


Fig. 1 Clock timing

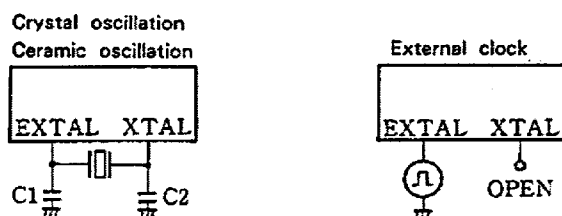


Fig. 2 Clock applying condition

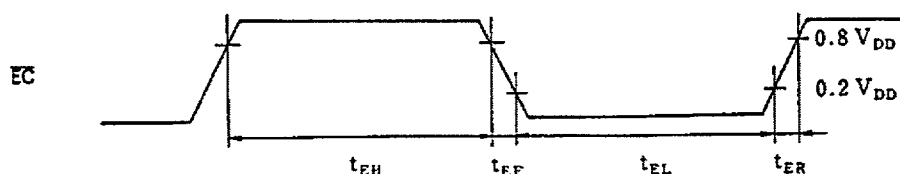


Fig. 3 Event count clock timing

(2) Serial transfer

Ta = -20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t _{D_{CSK}}	$\overline{SCK0}$ $\overline{SCK1}$	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ floating delay time	t _{D_{CSKF}}	$\overline{SCK0}$ $\overline{SCK1}$	($\overline{SCK}$ = output mode)		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ delay time	t _{D_{CSO}}	SO0 SO1	Chip select transfer mode		t _{sys} + 200	ns
$\overline{CS} \downarrow \rightarrow SO$ floating delay time	t _{D_{CSOF}}	SO0 SO1			t _{sys} + 200	ns
$\overline{CS}$ high level width	t _{WH_{CS}}	$\overline{CS0}$ $\overline{CS1}$		t _{sys} + 200		ns
$\overline{SCK}$ cycle time	t _{KCY}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	2t _{sys} + 200		ns
			Output mode	16000/f _c		ns
$\overline{SCK}$ high and low level widths	t _{KH} t _{KL}	$\overline{SCK0}$ $\overline{SCK1}$	Input mode	t _{sys} + 100		ns
			Output mode	8000/f _c - 50		ns
SI input setup time (against $\overline{SCK} \uparrow$)	t _{SIK}	SI0 SI1	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK} \uparrow$)	t _{KSI}	SI0 SI1	$\overline{SCK}$ input mode	t _{sys} + 200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow SO$ delay time	t _{KSO}	SO0 SO1	$\overline{SCK}$ input mode		t _{sys} + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (address ; 00FF_H) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/f_c (Upper 2-bit = "00"), 4000/f_c (Upper 2-bit = "01"), 16000/f_c (Upper 2-bit = "11")

2) The marks $\overline{CS}$, $\overline{SCK}$, SI and SO respectively mean pins of $\overline{CS} \rightarrow \overline{CS0}$, $\overline{CS1}$, $\overline{SCK} \rightarrow \overline{SCK0}$, $\overline{SCK1}$, SI $\rightarrow$ SI0, SI1, and SO $\rightarrow$ SO0, SO1.

3) The Load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.

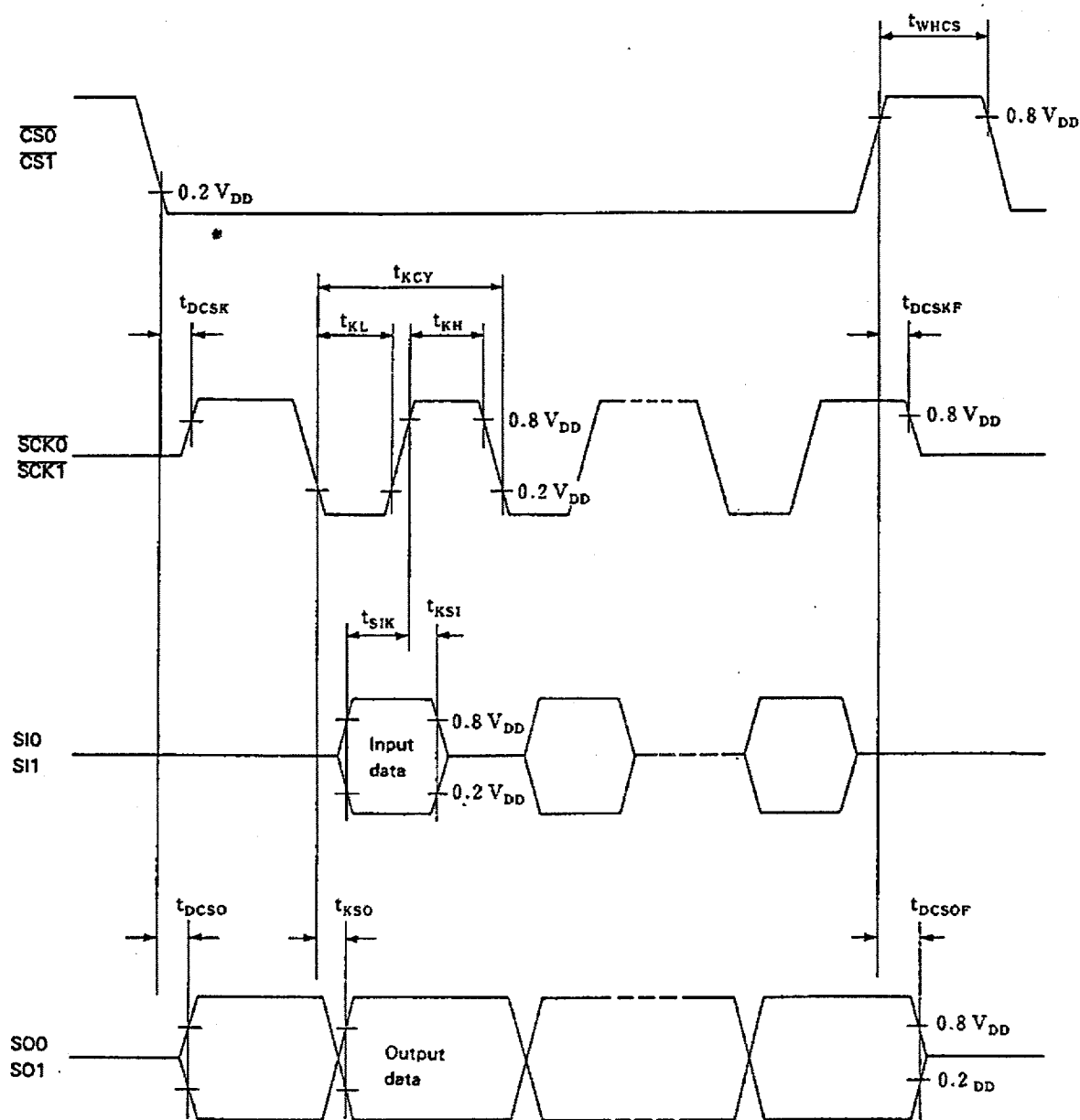
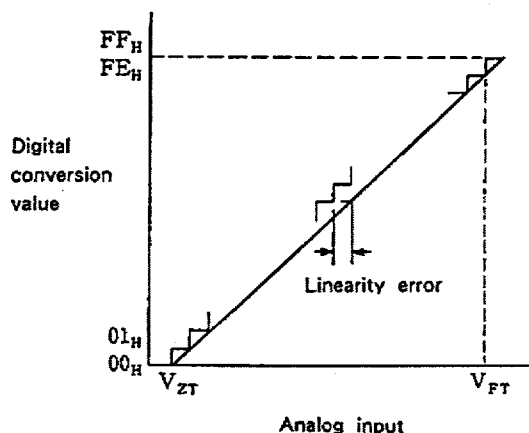


Fig. 4 Serial transfer timing

(3) A/D converter characteristics

 $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $V_{DD} = AV_{DD} = 4.5\text{V}$ to 5.5V , $AV_{REF} = 4.0\text{V}$ to AV_{DD} , $V_{SS} = AV_{SS} = 0\text{V}$

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			$T_a = 25^{\circ}\text{C}$			± 1	LSB
Zero transition voltage	V_{ZT} *1		$V_{DD} = AV_{DD} = 5.0\text{V}$	-10	30	70	mV
Full scale transition voltage	V_{FT} *2		$V_{SS} = AV_{SS} = 0\text{V}$	4930	4970	5010	mV
Conversion time	t_{CONV}			$160/f_c$			μs
Sampling time	t_{SAMP}			$12/f_c$			μs
Reference input voltage	V_{REF}	AV_{REF}		$AV_{DD} - 0.5$		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AVREF current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode			10	μA



* 1) V_{ZT} : Indicates the value that digital conversion value changes from 00H to 01H and vice versa.

* 2) V_{FT} : Indicates the value that digital conversion value changes from FEH to FFH and vice versa.

Fig. 5. Definitions of A/D converter terms

(4) Interruption, reset input

 $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $V_{DD} = 4.5\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} , t_{IL}	INT0, INT1, INT2, NMI		1		μs
Reset input low level width	t_{RSL}	RST		$8/f_c$		μs

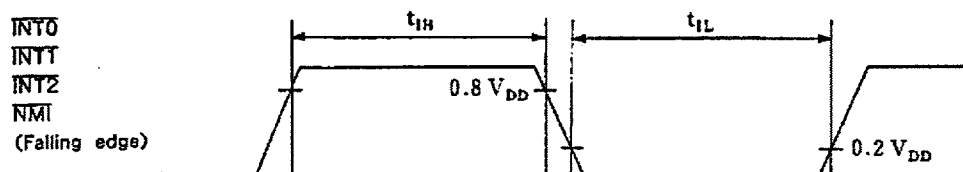


Fig. 6 Interruption input timing

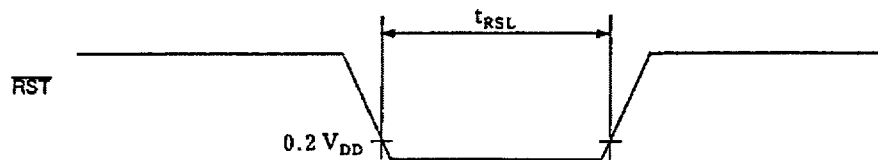


Fig. 7 Reset input timing

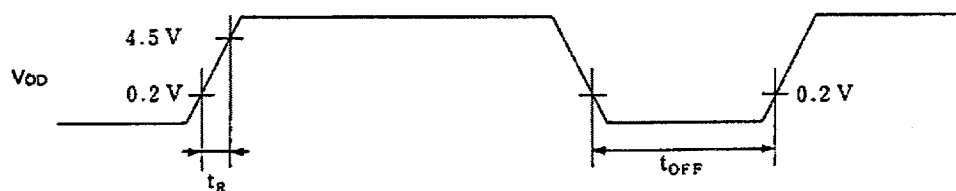
(5) Power on reset

Power on reset *

 $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $V_{DD} = 4.5\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.



The power supply should rise smoothly.

Fig. 8 Power on reset

(6) Others

Ta = -20°C to +75°C, V_{DD} = 4.5V to 5.5V, V_{SS} = 0V

Item	Symbol	Pin	Condition	Min.	Max.	Unit
GFG input high and low level widths	tCFH, tCFL	CFG		tsys + 200		ns
DFG input high and low level widths	tDFH, tDFL	DFG		1000/fc + 200		ns
DPG minimum pulse width	tDPW	DPG		50		ns
DPG minimum removal time	trem	DPG		50		ns
PBCTL input high and low level widths	tCTH, tCTL	PBCTL	tsys = 2000/fc	tsys + 200		ns
EXI input high and low level widths	tEIH, tEIL	EXI0 EXI1	tsys = 2000/fc	tsys + 200		ns

Note) tsys indicates three values according to the contents of the clock control register (address ; 00FFH) upper 2 bits (CPU clock selection).

tsys [ns] = 2000/fc (Upper 2-bit = "00"), 4000/fc (Upper 2-bit = "01"), 16000/fc (Upper 2-bit = "11")

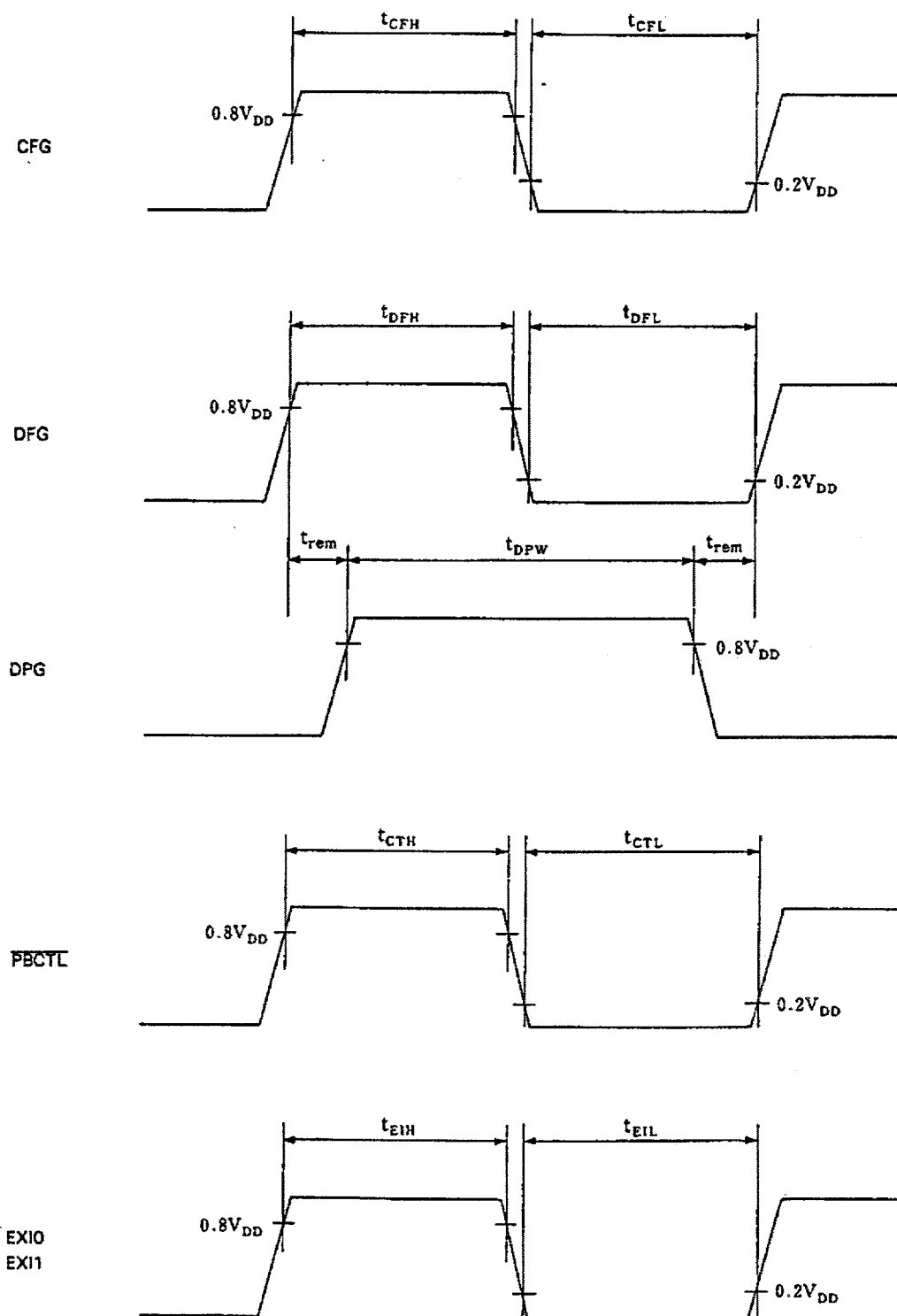


Fig. 9 Others timing

(7) Memory extension mode and microprocessor mode input/output timing

 $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $V_{DD} = 4.5\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$, $f_c = 8\text{MHz}$ ($t_{CYC} = 250\text{ns}$)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Control clock output (C) high and low level widths	tcWL, tcWH	C	Fig. 10	90		ns
High address (A15 to A8) output delay time	tCAHD	A15 to A8			80	ns
Low address (A7 to A0) output delay time	tCALD	A7 to A0			80	ns
Data (D7 to D0) output delay time	tcWD	D7 to D0			200	ns
Data (D7 to D0) output hold time	tWDHD				15	ns
Data (D7 to D0) input setup time	trDS			80		ns
Data (D7 to D0) input hold time	trDHD			15		ns
Read pulse ($\overline{RD}$) output delay time	trOD	$\overline{RD}$			90	ns
Write pulse ($\overline{WD}$) output delay time	tWRD	$\overline{WR}$			130	ns
Read/write pulse ($R/\overline{W}$) output delay time	trWD	$R/\overline{W}$			50	ns
Sync pulse ($\overline{SYNC}$) output delay time	tsyD	$\overline{SYNC}$		50	ns	

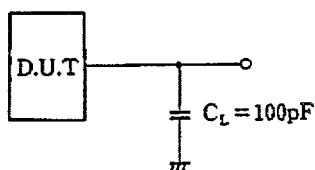


Fig. 10 Load condition

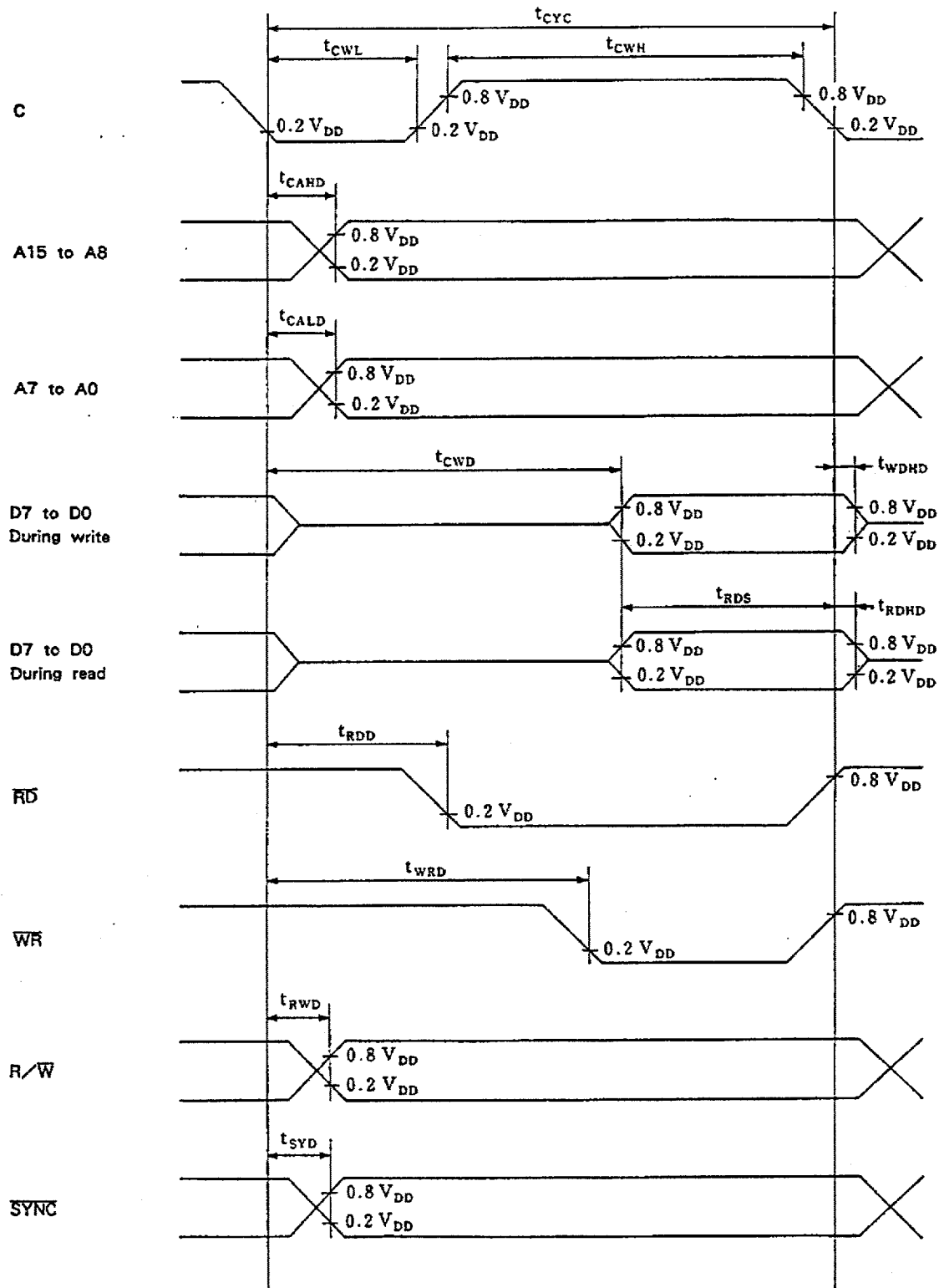


Fig. 11 Memory extension mode, microprocessor mode I/O timing

(8) Bus hold timing

 $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, $V_{DD} = 4.5\text{V}$ to 5.5V , $V_{SS} = 0\text{V}$, $f_c = 8\text{MHz}$

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Bus request ($\overline{\text{BRQ}}$) setup time	t_{BRDS}	$\overline{\text{BRQ}}$	Fig. 12	100		ns
Bus acknowledge ($\overline{\text{BAK}}$) delay time	t_{SYBA}	$\overline{\text{BAK}}$			50	ns
Bus acknowledge ($\overline{\text{BAK}}$) releasing delay time	t_{BRBA}				220	ns
Bus line, control signal releasing delay time	t_{BRAD}	A15 to A0 D7 to D0 $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\text{R}/\overline{\text{W}}$			210	ns

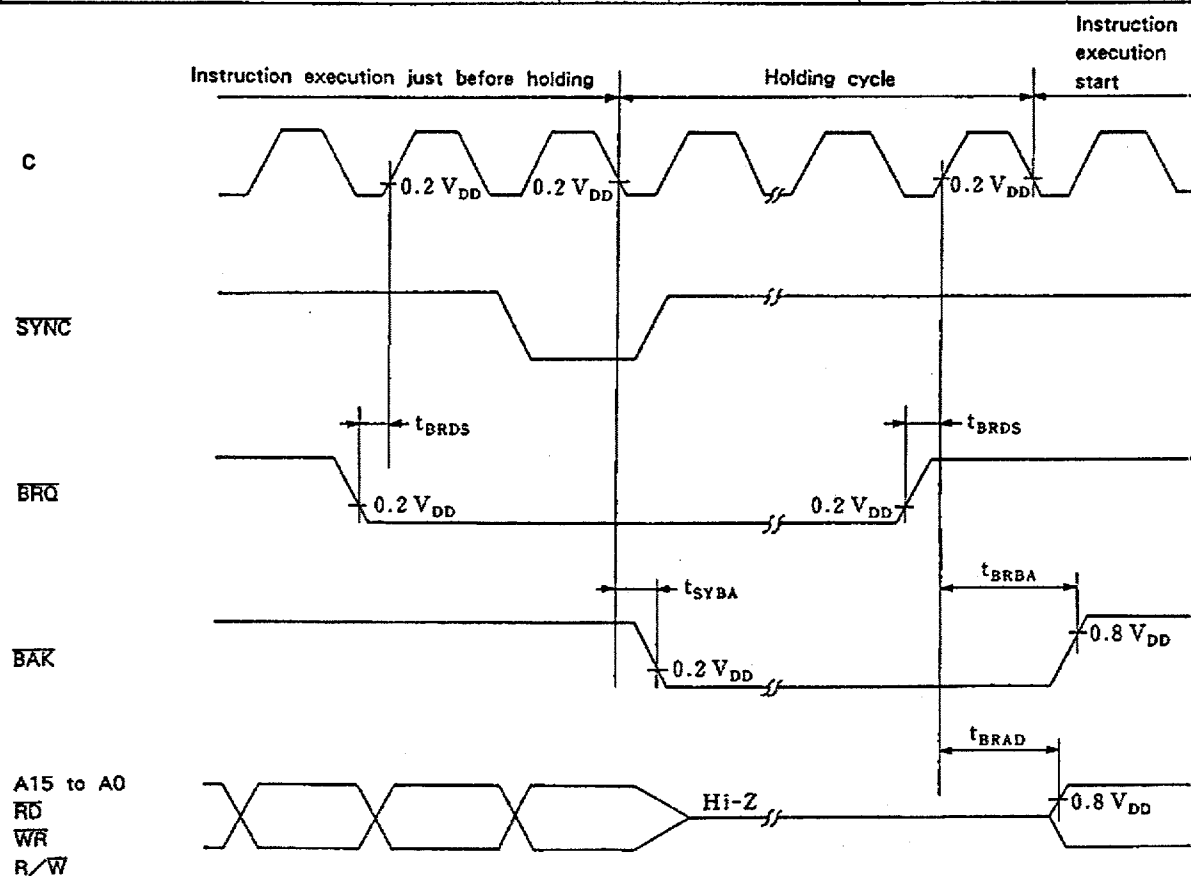


Fig. 12 Bus hold timing

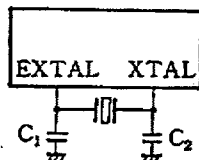
Fig. 13 shows recommended circuits and oscillators.

Use the trimmer capacitor to C1, in the case of accurate adjustment of the oscillation frequency.

1.

Ceramic resonator

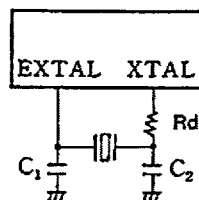
Manufacturer	Model	Frequency range(MHz)	C1 (pF)	C2(pF)
MURATA MFG CO., LTD.	CSA6.00MG010	6.00	100	100
	CSA8.00MT	8.00	30	30



Crystal oscillator

Manufacturer	Model	Frequency range(MHz)	C1 (pF)	C2(pF)
FUJI SANGYO CO., LTD.	HC-49/U-03	6.00	12	12
		8.00	12	12
KINSEKI LTD.	HC-49/U-S	6.00	15	15
		8.00	15	15

2.



Manufacturer	Model	Frequency range(MHz)	C1 (pF)	C2(pF)	Rd(k Ω)
CITIZEN WATCH CO., LTD.	CSA-309	6.144	5	5	1
		8.00	5	5	1

About the details of oscillators, please inquire the makers or the agencies.

Fig. 13 Recommended oscillation circuit

Mask option table

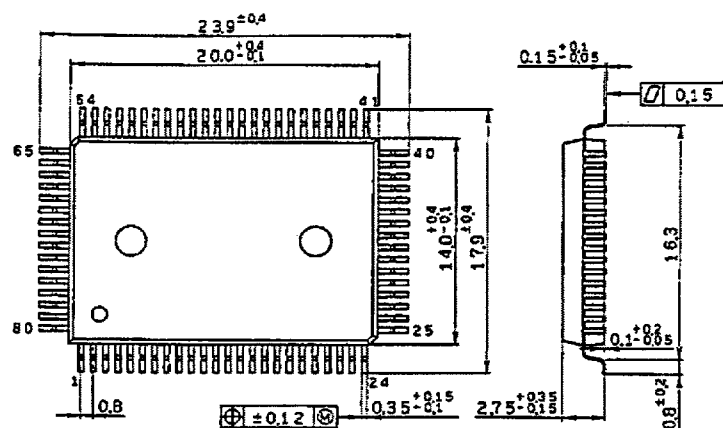
Item		
Reset pin pull-up resistor	Non-existent	Exsistent
Power on reset circuit	Non-existent	Exsistent
Input circuit format (Fig.1)	C-MOS schmitt	TTL schmitt

Note) In PG4/SYNCO pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

Package Outline

Unit : mm

80pin QFP (Plastic) 1.5g



SONY NAME	GFP-80P-L01
EIAJ NAME	*GFP080-P-1420-A
JEDEC CODE	_____