ispXPLD™ 5000MX Fa

3.3V, 2.5V and 1.8V In-System Progr
eXpanded Programmable Logic Device XPLD

August 2004

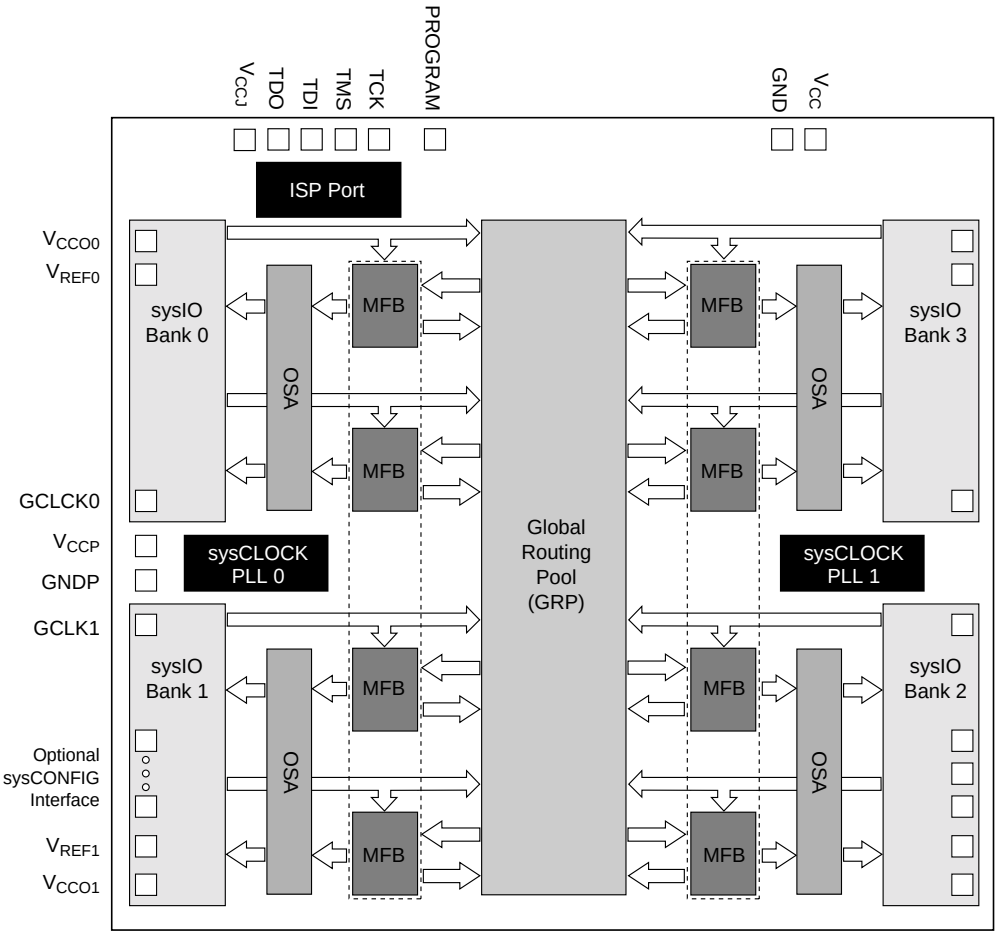
Features

- **Flexible Multi-Function Block (MFB) Architecture**
  - SuperWIDE™ logic (up to 136 inputs)
  - Arithmetic capability
  - Single- or Dual-port SRAM
  - FIFO
  - Ternary CAM
- **sysCLOCK™ PLL Timing Control**
  - Multiply and divide between 1 and 32
  - Clock shifting capability
  - External feedback capability
- **sysIO™ Interfaces**
  - LVCMOS 1.8, 2.5, 3.3V
    - Programmable impedance
    - Hot-socketing
    - Flexible bus-maintenance (Pull-up, pull-down, bus-keeper, or none)
    - Open drain operation
  - SSTL 2, 3 (I & II)
  - HSTL (I, III, IV)
  - PCI 3.3
  - GTL+
  - LVDS
  - LVPECL
  - LVTTL
- **Expanded In-System Programmability**
  - Instant-on capability
  - Single chip convenience
  - In-System Programmable via IEEE 1
    Interface
  - Infinitely reconfigurable via IEEE 153
    sysCONFIG™ microprocessor interf
  - Design security
- **High Speed Operation**
  - 4.0ns pin-to-pin delays, 300MHz f_{MA}
  - Deterministic timing
- **Low Power Consumption**
  - Typical static power: 20 to 50mA (1.8
    30 to 60mA (2.5/3.3V)
  - 1.8V core for low dynamic power
- **Easy System Integration**
  - 3.3V (5000MV), 2.5V (5000MB) and
    (5000MC) power supply operation
  - 5V tolerant I/O for LVCMOS 3.3 and
    interfaces
  - IEEE 1149.1 interface for boundary s
  - sysIO quick configuration
  - Density migration
  - Multiple density and package options
  - PQFP and fine pitch BGA packaging
  - Lead-free package options

Table 1. ispXPLD 5000MX Family Selection Guide

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPL
Macrocells	256	512	768	
Multi-Function Blocks	8	16	24	
Maximum RAM Bits	128K	256K	384K	
Maximum CAM Bits	48K	96K	144K	
sysCLOCK PLLs	2	2	2	
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	
t_S (Register Set-up Time)	2.2ns	2.8ns	2.8ns	
t_{CO} (Register Clock to Out Time)	2.8ns	3.0ns	3.2ns	
f_{MAX} (Maximum Operating Frequency)	300MHz	275MHz	250MHz	25
System Gates	75K	150K	225K	
I/Os	141	149/193/253	193/317	31
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 672

Figure 1. ispXPLD 5000MX Block Diagram



Introduction

The ispXPLD 5000MX family represents a new class of device, referred to as the eXpanded Programm Devices (XPLDs). These devices extend the capability of Lattice's popular SuperWIDE ispMACH 5000 by providing flexible memory capability. The family supports single- or dual-port SRAM, FIFO, and te operation. Extra logic has also been included to allow efficient implementation of arithmetic functions. sysCLOCK PLLs and sysIO interfaces provide support for the system-level needs of designers.

The devices provide designers with a convenient one-chip solution that provides logic availability at boo security, and extreme reconfigurability. The use of advanced process technology provides industry-lea mance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.2ns set-up tim ating frequency up to 300MHz. This performance is coupled with low static and dynamic power consu ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices along with the flexibility of the sysIO inte users meet the challenge of today's mixed voltage designs. Inputs can be safely driven up to 5.5V w bank is configured for 3.3V operation, making this family 5V tolerant. Boundary scan testability further gration into today's complex systems. A variety of density and package options increase the likelihood for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global R Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of t

5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. An Out Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-p access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysC are provided to allow the synthesis of new clocks and control of clock skews.

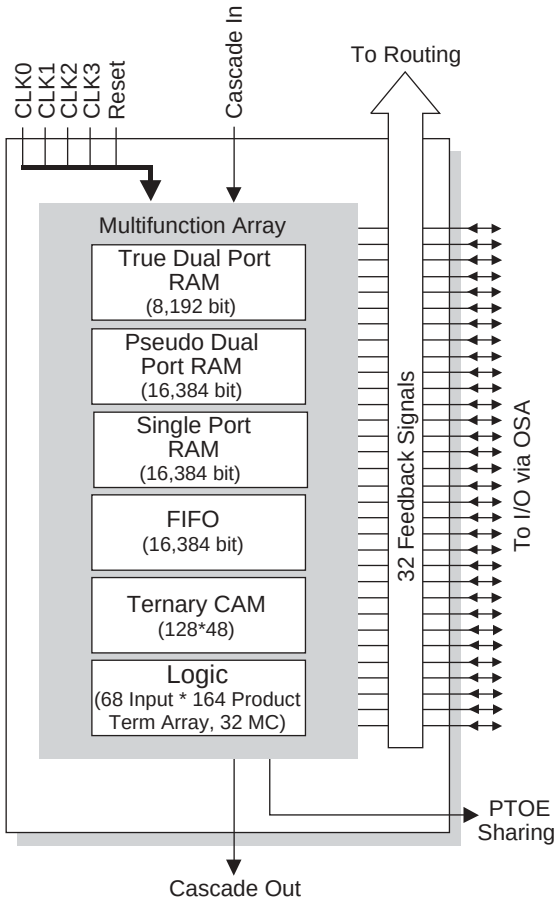
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. T a flexible approach to implementing logic and memory that allows the designer to achieve the mix of fu are required for a particular design, maximizing resource utilization. The six modes supported by the M

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

The MFB consists of a multi-function array and associated routing. Depending on the chosen function function array uses up to 68 inputs from the GRP and the four global clock and reset signals. The a data along with certain control functions to the macrocells. Output signals can be routed internally fo where in the device and to the sysIO banks for output. Figure 2 shows the block diagram of the MFB. configurations are described in more detail in the following sections.

Figure 2. MFB Block Diagram



Cascading For Wide Operation

In several modes it is possible to cascade adjacent MFBs to support wider operation. Table 2 details cascading options. There are chains of MFBs in each device which determine those MFBs that are adja purposes of cascading. Table 3 indicates these chains. The ispXPLD 5000MX design tools automatica blocks if required by a particular design.

Table 2. Cascading Modes For Wide Support

Mode	Cascading Function
Logic	**Input Width.** Allows two MFBs to act as a 136-input block.
	Arithmetic. Allow the carry chain to pass between two MFBs.
FIFO	**Memory Width Expansion.** Allows MFBs to be cascaded for greater width support.
CAM	**Memory Width Expansion.** Allows up to four MFBs to be cascaded for greater width suppo

Table 3. MFB Cascade Chain

Device	MFBs in Cascade Chain
ispXPLD 5256MX	A → B → C → D
	H -> G -> F -> E
ispXPLD 5512MX	A → B → C → D → E → F → G → H
	P → O → N → M → L → K → J → I
ispXPLD 5768MX	D → C → B → A → X → W → V → U → T → S → R → Q
	E → F → G → H → I → J → K → L → M → N → O → P
ispXPLD 51024MX	H → G → F → E → D → C → B → A → AF → AE → AD → AC → AB → AA → Z
	I → J → K → L → M → N → O → P → Q → R → S → T → U → V → W → X

SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array wi product terms and four control product terms. The MFB has 68 inputs from the Global Routing Poo available in both true and complement form for every product term. It is also possible to cascade adjac create a block with 136 inputs. The four control product terms are used for shared reset, clock, clock output enable functions. Figure 3 shows the overall structure of the MFB in logic mode while Figure 4 more detailed view from the perspective of a macrocell slice.

Figure 3. MFB in SuperWIDE Logic Mode

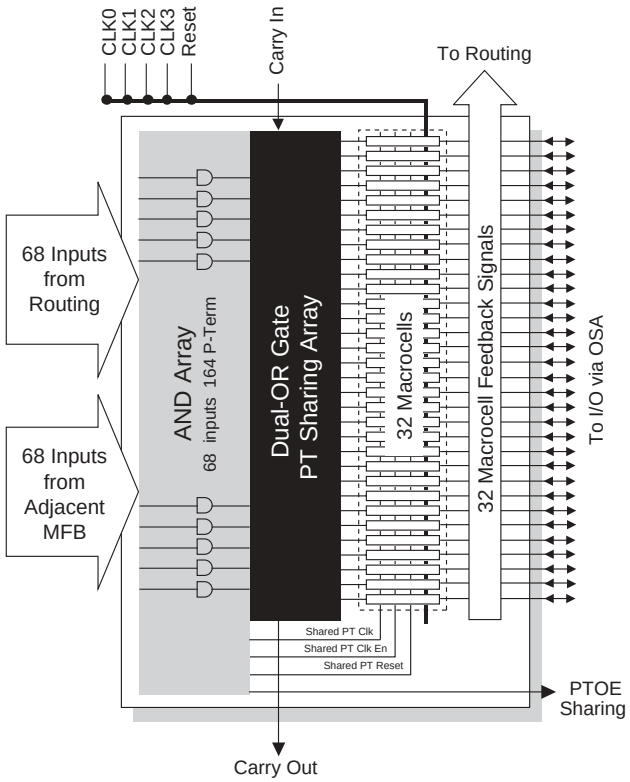
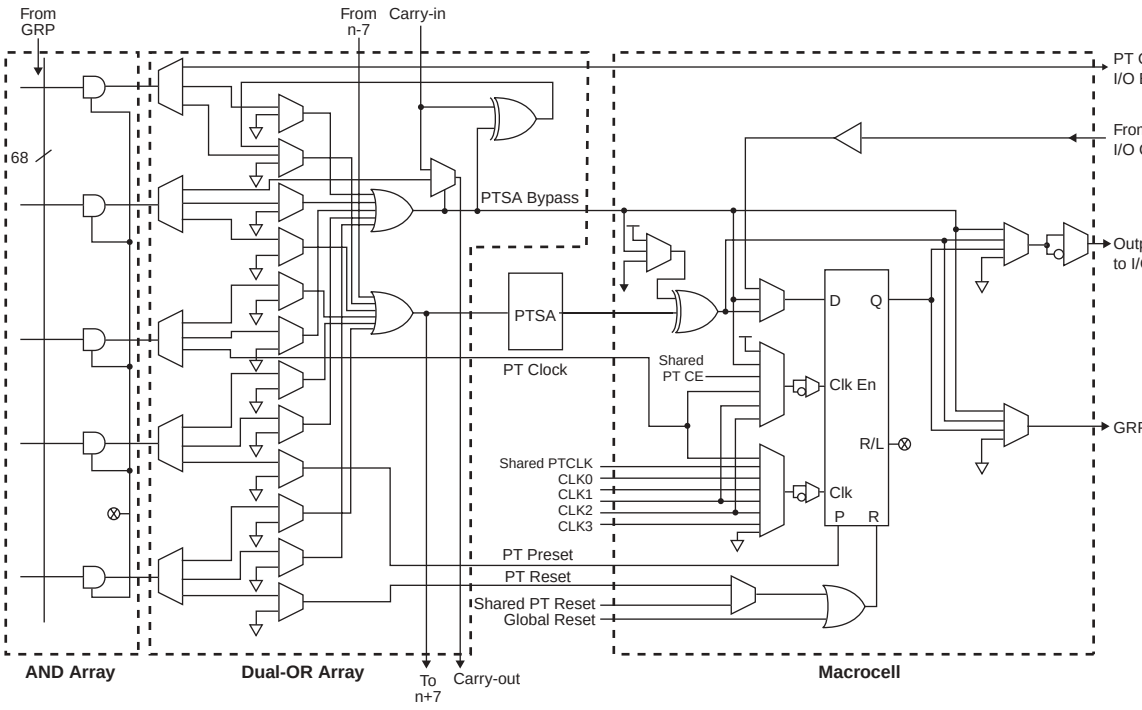


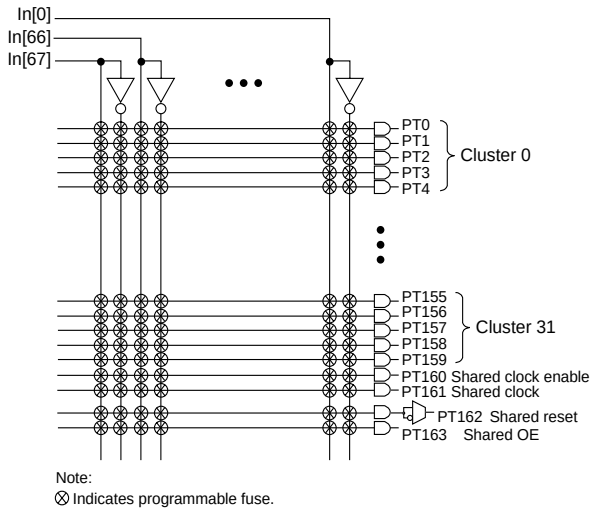
Figure 4. Macrocell Slice in Logic Mode AND-Array



AND-Array

The programmable AND-Array consists of 68 inputs and 164 output product terms. The 68 inputs from t used to form 136 lines in the AND-Array (true and complement of the inputs). Each line in the array nected to any of the 164 output product terms via a wired AND. Each of the 160 logic product terms fe OR Array with the remaining four control product terms feeding the Shared PT Clock, Shared PT Cl Shared PT Reset and Shared PT OE. Starting with PT0 sets of five product terms form product te There is one product term cluster for every macrocell in the MFB. In addition to the four control produc first, third, fourth and fifth product terms of each cluster can be used as a PTOE, PT Clock, PT Pre Reset, respectively. Figure 5 is a graphical representation of the AND-Array.

Figure 5. AND Array

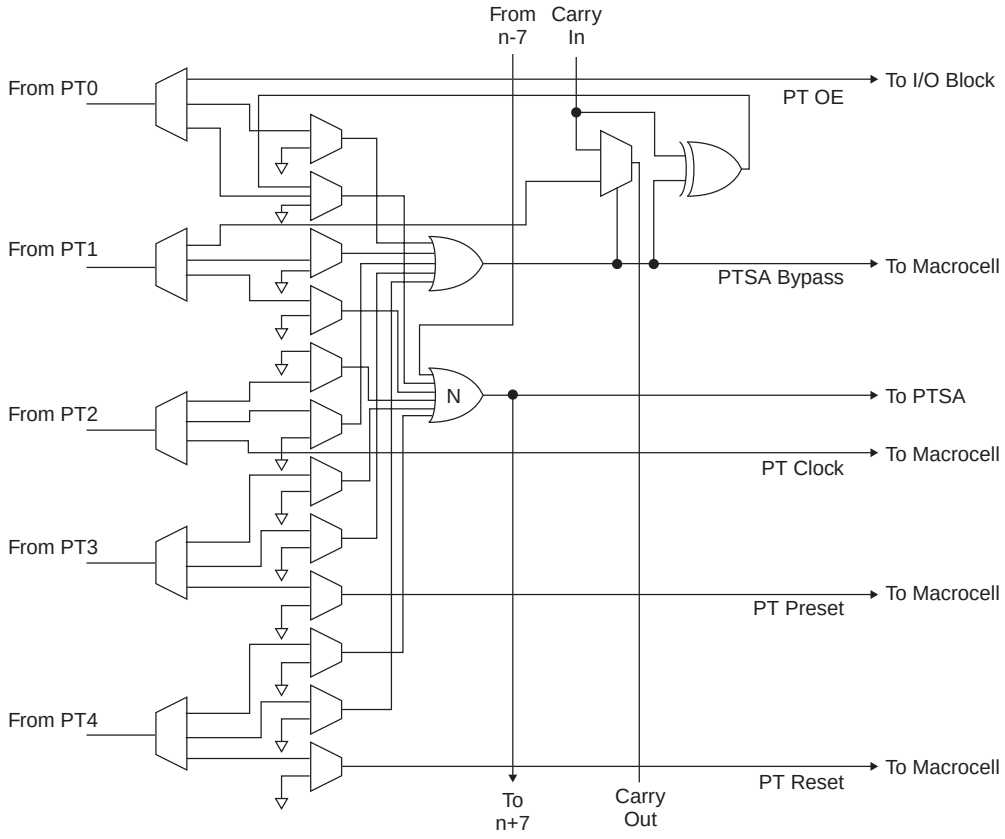


Dual-OR Array (Including Arithmetic Support)

The Dual-OR Array consists of 64 OR gates. There are two OR gates per macrocell in the MFB. Thes are referred to as the Expandable PTSA OR gate and the PTSA-Bypass OR gate. The PTSA-Bypa receives its five inputs from the combination of product terms associated with the product term cluster. Bypass OR gate feeds the macrocell directly for fast narrow logic. The Expandable PTSA OR gate r inputs from the combination of product terms associated with the product term cluster. It also receives a input from the Expanded PTSA OR gate of the N-7 macrocell, where N is the number of the macrocel with the current OR gate. The Expandable PTSA OR gate feeds the PTSA for sharing with other produc the N+7 Expandable PTSA OR gate. This allows cascading of multiple OR gates for wide functions small timing adder for each level of expansion. Figure 6 is a graphical representation of the Dual-OR A

The Dual-OR PT sharing array also contains logic to aid in the efficient implementation of arithmetic fu logic takes Carry In and allows the generation of Carry Out along with a SUM signal. Subtractors ca mented using the two's complement method. Carry is propagated from macrocells 0 to macrocell 3 zero can have its carry input connected to the carry output of macrocell 31 in an adjacent MFB or it c zero or one. If a macrocell is not used in an arithmetic function carry can bypass it. The carry chain same as that for PT cascading.

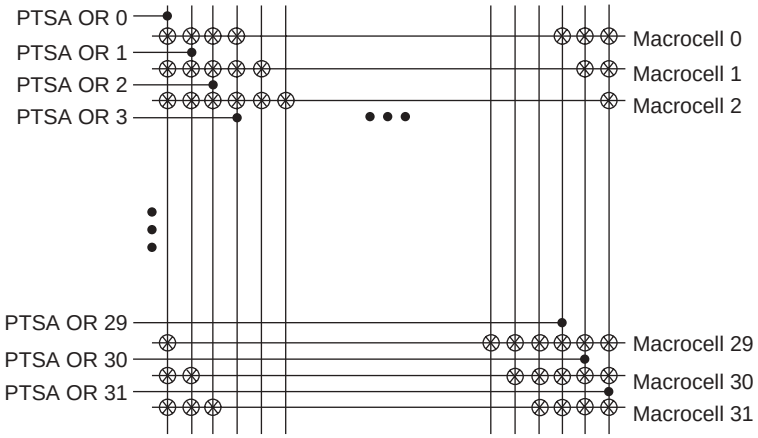
Figure 6. Dual-OR PT Sharing Array



Product Term Sharing Array

The Product Term Sharing Array (PTSA) consists of 32 inputs from the Dual-OR Array (Expandable PT 32 outputs directly to the macrocells. Each output is the OR term of any combination of the seven PTSA OR terms connected to that output. Every Nth macrocell is connected to N-3, N-2, N-1, N, N+ N+3 PTSA OR terms via a programmable connection. This wraps around the logic, for example, Macr its logic from 29, 30, 31, 0, 1, 2, 3. The Expandable PTSA OR used in conjunction with the PTSA allow tions to be implemented easily and efficiently. Without using the Expandable PTSA OR capability, t number of product terms that can be included in a single function with one pass of delay is 35. Up to terms can be included in a single function through the use of the expandable PTSA OR capability. Figu the graphical representation of the PTSA.

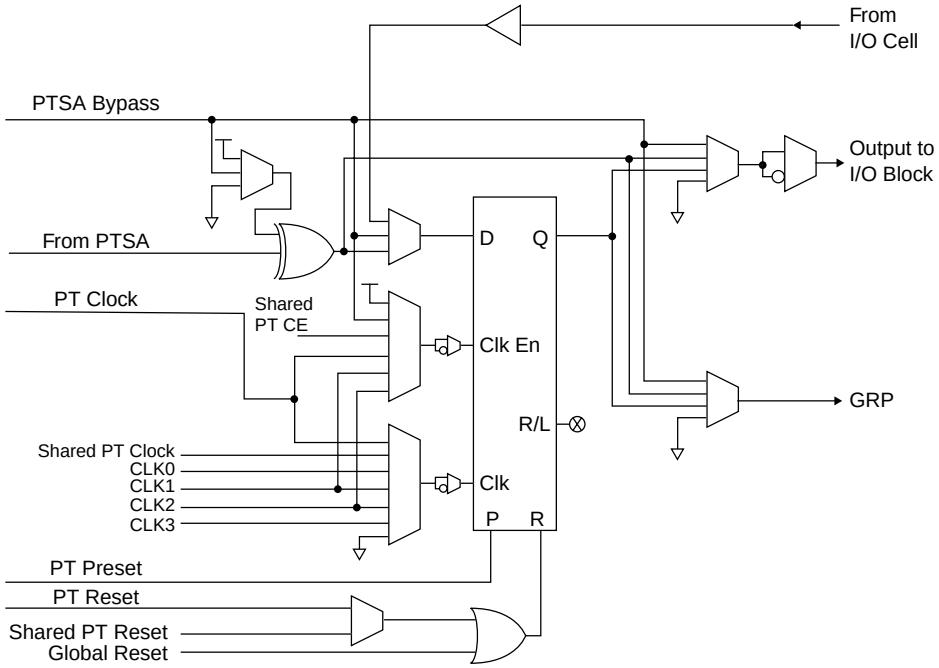
Figure 7. Product Term Sharing Array (PTSA)



Macrocell

The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA by macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the neces and control logic to allow combinatorial or registered operation. All macrocells have an output that fee Selected macrocells have an additional output that feeds the OSA and hence I/Os. This dual or concu capability from the macrocell gives efficient use of the hardware resources. One output can be a registe for example, while the other output can be an unrelated combinatorial function. A direct register input cell facilitates efficient use of the macrocell to construct high-speed input registers. Macrocell regis clocked from one of several global or product term clocks available on the device. A global and produc enable is also provided, eliminating the need to gate the clock to the macrocell registers directly. Rese for the macrocell register is provided from both global and product term signals. The macrocell register grammed to operate as a D-type register or a D-type latch. Figure 8 is a graphical representation of the

Figure 8. Macrocell



Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks as Table 4. The remainder of this section details operation of each of the memory modes. Additional regarding the memory modes can also be found in technical note number TN1030, *Using Memory 5000MX Devices.*

Table 4. MFB Memory Configuration

Memory Mode	Max. Configuration Size[1]
Dual-port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 8 512 x 16
Single-port, Pseudo Dual Port, FIFO	16,384 x1 8,192 x 2 4,096 x 4 2,048 x 8 1,024 x 16 512 x 32
CAM	128 x 48

1. Smaller configurations are possible.

Input and Output

The data input and control signals to a MFB in memory mode are generated from inputs from the routin nals are only available in the true non-inverted format. True or complemented versions of the inputs a for generating the control signals. Data and flag outputs are fed from the MFB to the GRP and OSA. Ur and outputs are not accessible in memory mode.

ROM Operation

In each of the memory modes it is possible to specify the power-on state of each bit in the memory allows the memory to be used as ROM if desired.

Increased Depth And Width

Designs that require a memory depth or width that is greater than that support by a single MFB can b by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width i vided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIF modes additional width is supported through the cascading of MFBs.

The Lattice design tools automatically combine blocks to support the memory size specified in the use

Bus Size Matching

All of the memory modes apart from CAM mode support different widths on each of the ports. The R mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1 and so on. Although the word size an words for each port varies this mapping scheme applies to each port.

True Dual-Port SRAM Mode

In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two i read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are suppo MFB. Figure 9 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The outp nals can be synchronous or asynchronous. Resets are asynchronous. All inputs on the same port sha clock, clock enable, and reset selections. All outputs on the same port share the same clock, clock reset selections. Selections may be made independently between both inputs and outputs and po shows the possible sources for the clock, clock enable and initialization signals for the various registers

Figure 9. Dual-Port SRAM Block Diagram

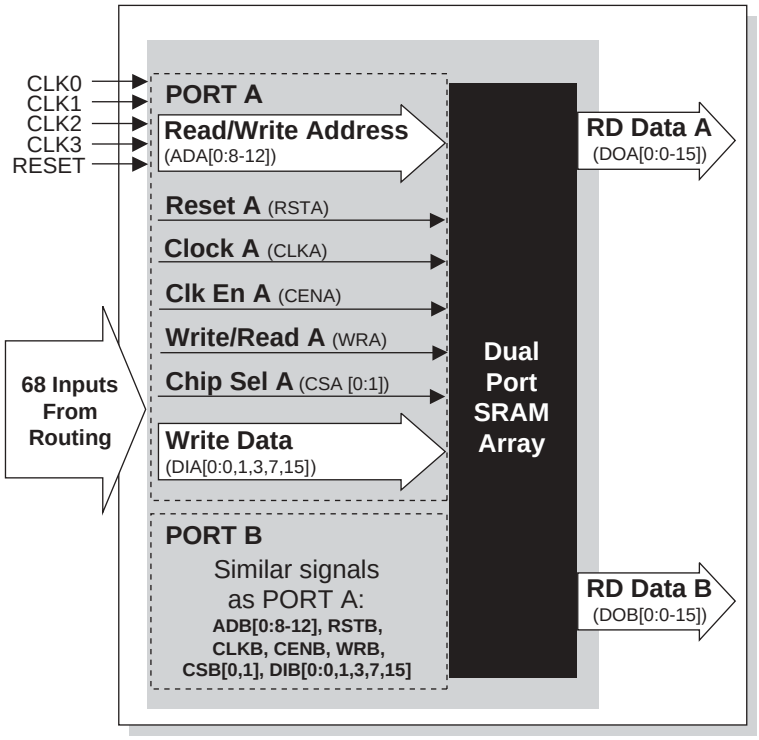


Table 5. Register Clock, Clock Enable, and Reset in Dual-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLKA (CLKB) or one of the global clocks (CLK0 - CLK3). The selecte nal can be inverted if desired.
	Clock Enable	CENA (CENB) or one of the global clocks (CLK1 - CLK 2). The selec nal can be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RSTA (RSTB RSTA (RSTB) can be inverted is desired.

Pseudo Dual-Port SRAM Mode

In Pseudo Dual-Port SRAM Mode the multi-function array is configured as a SRAM with an independe write ports that access the same 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supp MFB. Figure 10 shows the block diagram of the Pseudo Dual-Port SRAM.

Write data, write address, chip select and write enable signals are always synchronous (registered). Th and read address signals can be synchronous or asynchronous. Reset is asynchronous. All write signa same clock, and clock enable. All read signals share the same clock and clock enable. Reset is sha read and write signals. Table 6 shows the possible sources for the clock, clock enable and initializatio the various registers.

Figure 10. Pseudo Dual-Port SRAM Block Diagram

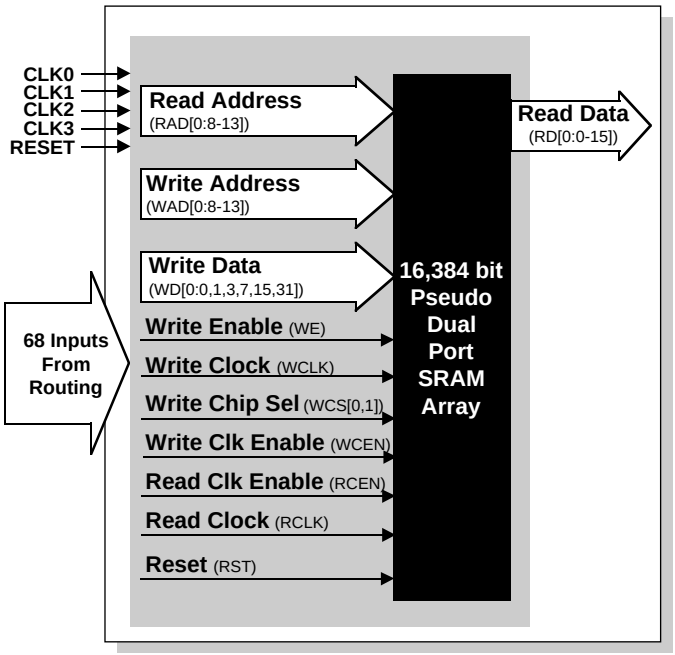


Table 6. Register Clock, Clock Enable, and Reset in Pseudo Dual-Port SRAM Mode

Register	Input	Source
Write Address, Write Data, Write Enable, and Write Chip Select	Clock	WCLK or one of the global clocks (CLK0 - CLK3). The selected signa be inverted if desired.
	Clock Enable	WCEN or one of the global clocks (CLK1 - CLK2). The selected sign be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST ma inversion if desired.
Read Data and Read Address	Clock	RCLK or one of the global clocks (CLK0 - CLK3). The selected signal inverted if desired.
	Clock Enable	RCEN or one of the global clocks (CLK1 - CLK2). The selected signa be inverted if desired.
	Reset	Created by the logical OR of the global reset signal and RST. RST ma inversion if desired.

Single-Port SRAM Mode

In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mod accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supported by the MFB. Figu the block diagram of the single-port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The outp nals can be synchronous or asynchronous. Reset is asynchronous. All signals share a common enable, and reset. Table 7 shows the possible sources for the clock, clock enable and reset signals.

Figure 11. Single-Port SRAM Block Diagram

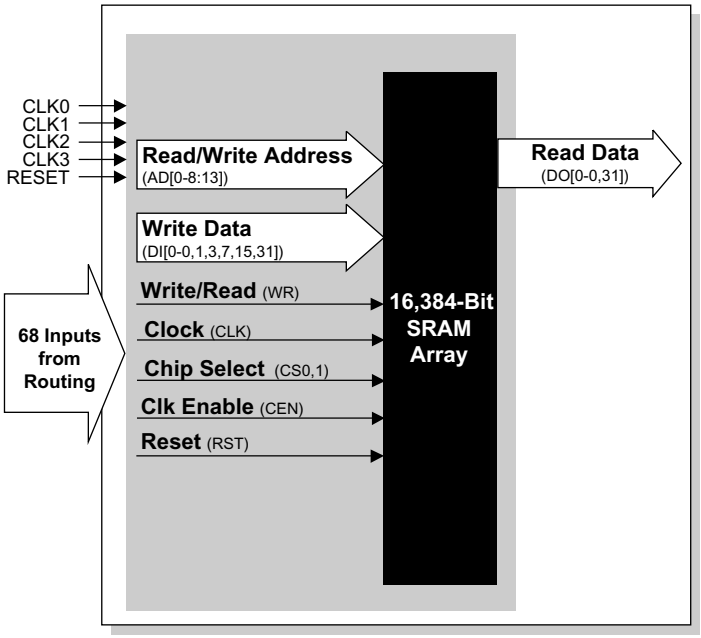


Table 7. Register Clock, Clock Enable, and Reset in Single-Port SRAM Mode

Register	Input	Source
Address, Write Data, Read Data, Read/ Write, and Chip Select	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these signal be inverted if required.
	Clock Enable	CEN or one of the global clocks (CLK1 - CLK 2). Each of these signa be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. RST is by the multifunction array from GRP, with inversion if desired.

FIFO Mode

In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in read and write clocks can be different or the same dependent on the application. Four flags show the s FIFO; Full, Empty, Almost Full, and Almost Empty. The thresholds for Full, Almost full and Almost em grammable by the user. It is possible to reset the read pointer, allowing support of frame retransmit in tions applications. If desired, the block can be used in show ahead mode allowing the early reading of th address.

In this mode one ports accesses 16,384-bits of memory. Data widths of 1, 2, 4, 8, 16 and 32 are supp MFB. Figure 12 shows the block diagram of the FIFO.

Write data, write enable, flag outputs and read enable are synchronous. The Write Data, Almost Full an the same clock and clock enables. Read outputs are synchronous although these can be configured in mode. The Read Data, Empty and Almost Empty signals share the same clock and clock enables. Res by all signals. Table 8 shows the possible sources for the clock, clock enable and reset signals for the isters.

Figure 12. FIFO Block Diagram

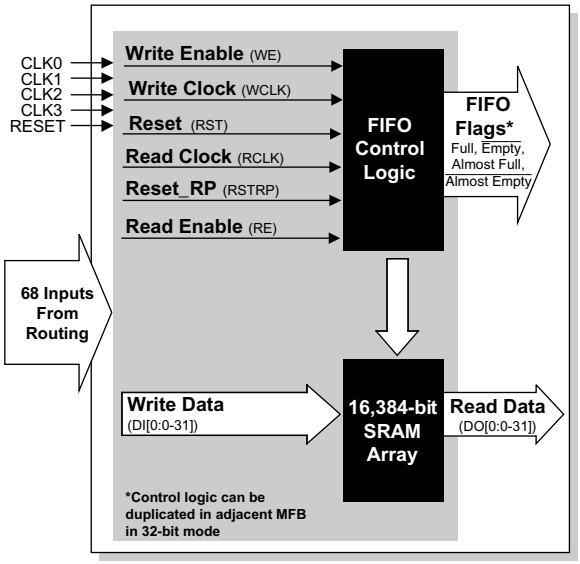


Table 8. Register Clocks, Clock Enables, and Initialization in FIFO Mode

Register	Input	Source
Write Data, Write Enable	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverte
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted
	Reset	N/A
Full and Almost Full Flags	Clock	WCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverte
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the mul array from GRP, with inversion if desired.
Read Data, Empty and Almost Empty Flags	Clock	RCLK or one of the global clocks (CLK0 - CLK3). Each of these signals can be inverte
	Clock Enable	RE or one of the global clocks (CLK1 - CLK 2). Each of these signals can be inverted i
	Reset	Created by the logical OR of the global reset signal and RST. RST is routed by the mul array from GRP, with inversion if desired.

CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (C behaves like a reverse memory where the input is data and the output is an address. It can be used t variety of high-performance look-up functions. As such, CAM has two modes of operation. In write or u the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations plied to the CAM and if this matches any of the data in the array the Match and Multiple Match (if there i one match) flags are set to true and the lowest address with matching data is output. The CAM c entries of 48 bits. Figure 13 shows the block diagram of the CAM.

To further enhance the flexibility of the CAM a mask register is available. If enabled during updates sponding with those set to 1 in the mask register are not updated. If enabled during compare operations sponding to those set to 1 in the mask register are not included in the compare. A write don't care s don't cares to be programmed into the CAM if desired. Like other write operations the mask register co

The write/comp data, write address, write enable, write chip select, and write don't care signals are sy The CAM Output signals, match flag, and multimatch flag can be synchronous or asynchronous. The E register input is not latched but must meet setup and hold times relative to the write clock. All inputs m same clock and clock enable signals. All outputs must use the same clock and clock enable signals. Re mon for both inputs and outputs. Table 9 shows the allowable sources for clock, clock enable, and rese ious CAM registers.

Figure 13. CAM Mode

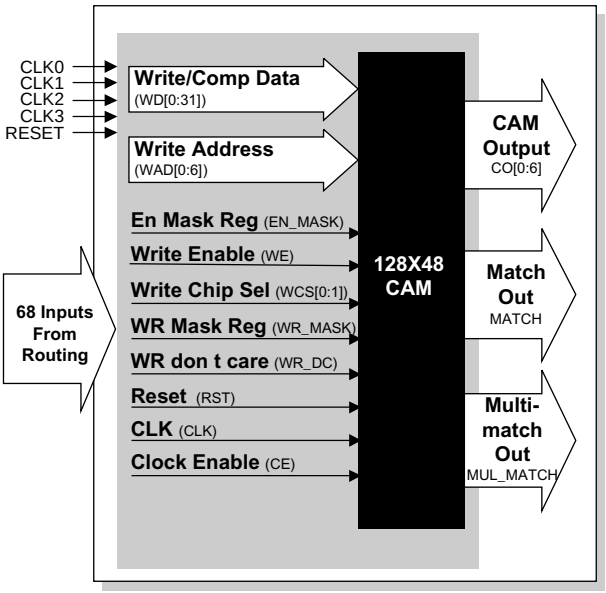


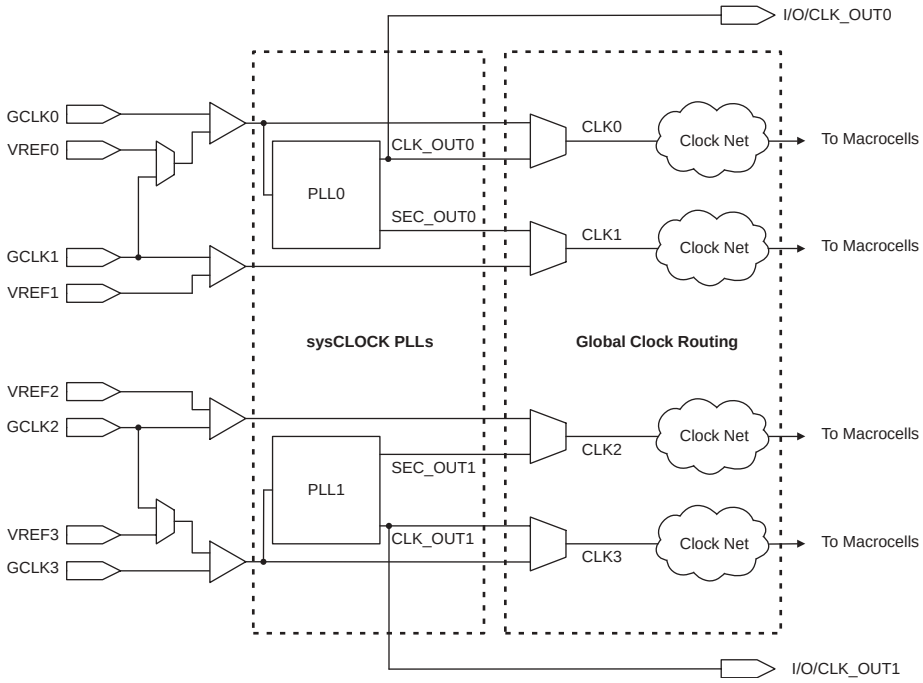
Table 9. Register Clocks, Clock Enables, and Initialization in CAM Mode

Register	Input	Source
Write data, Write address, Enable mask register, Write enable, write chip select, and write don't care, CAM Output, Match, and Multimatch	Clock	CLK or one of the global clocks (CLK0 - CLK3). Each of these s be inverted if required.
	Clock Enable	WE or one of the global clocks (CLK1 - CLK 2). Each of these s be inverted if required.
	Reset	Created by the logical OR of the global reset signal and RST. R by the multifunction array from GRP, with inversion if desired

Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GC routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sys cuit). These feed the registers in the MFBs. Note at each register there is the option of inverting required. Figure 14 shows the clock distribution network.

Figure 14. Clock Distribution Network



sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset a signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies ate multiple clock signals for routing within the device. Furthermore, it can generate clock signals skewed either at the board level or the device level.

The ispXPLD 5000MX devices provide two PLL circuits. PLL0 receives its clock inputs from GCLK 0 a outputs to CLK 0 (CLK 1 when using the secondary clock). PLL1 operates with signals from GCLK 3 (CLK 2 when using the secondary clock). The optional outputs CLK_OUT can be routed to an I/O pin. PLL_LOCK output is routed into the GRP. The optional input PLL_RST can be routed either from directly from an I/O pin. The optional PLL_FBK into can be routed directly from a pin. Figure 15 shows t 5000MX PLL block diagram. Figure 16 shows the connection of optional inputs and outputs.

Figure 15. PLL Block Diagram

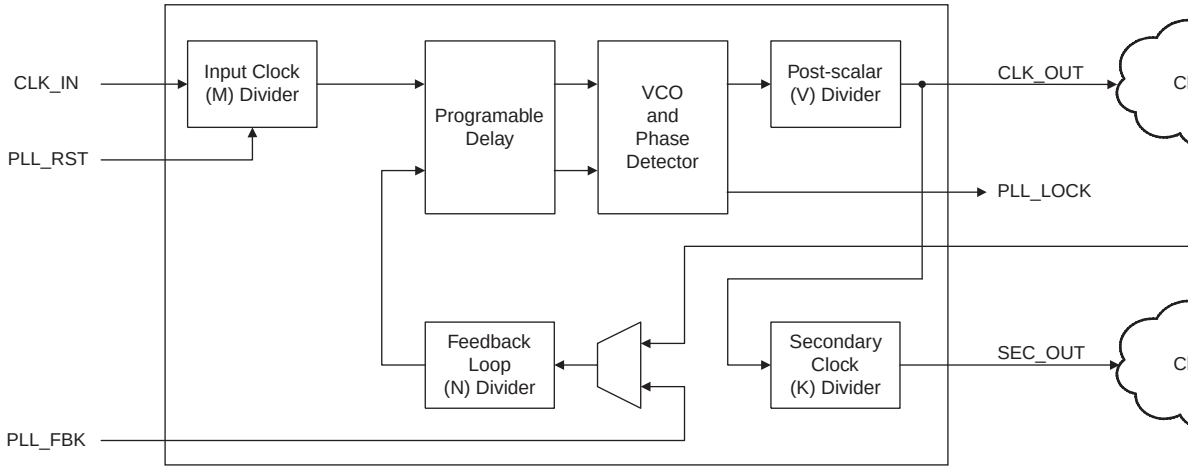
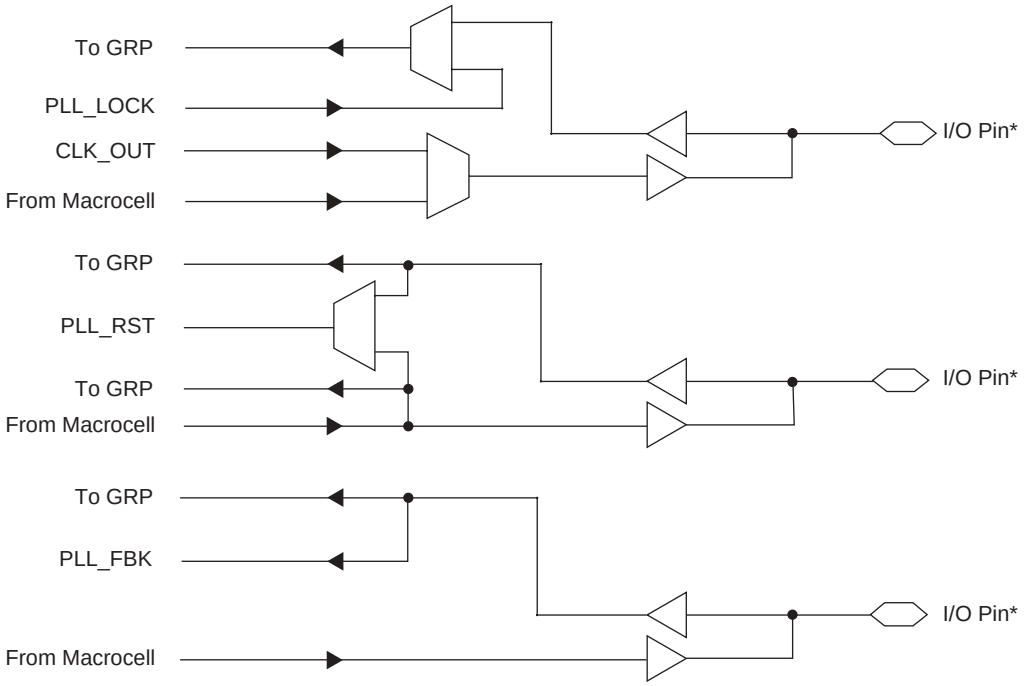


Figure 16. Connection of Optional PLL Inputs and Outputs



*See pinout table for details

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock K divider is only used when a secondary clock output is needed. This divider divides the primary clock feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, whi ing a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that all put clock to be advanced or delayed to improve set-up and clock-to-out times for better performanc information on the PLL, please refer to Lattice technical note number TN1003, *Lattice sysCLOCK Guidelines.*

Output Sharing Array (OSA)

A number of I/O pads are available in each sysIO bank to route the selected number of macrocells fro outputs directly to the I/O pads in logic mode. In the ispXPLD 5000MX, the large number of inputs and MFB as well as the presence of the PTSA can cover most routing flexibility of signals to I/O cells. The O ing Array gives additional routing capability and I/O access to an MFB when a wide output function t whole MFB and cannot be easily divided across multiple MFBs. By using the OSA, the wide output fu as 32-bit FIFO, can have all of its output signals from the one MFB routed to I/O cells. In a given I/O blo output functions must share the I/O pads with other logic functions.

The OSA bypass option routes the MFB signal directly to the I/O cell, allowing a direct connection to The logic functions use the option to provide faster speed to the outputs. The Logic Signal Connectio the OSA bypass as the primary macrocell and OSA options as alternate macrocells. Similarly, the Alt listing in the table shows the alternate macrocell input connection for a given I/O pin. Figure 17 shows t macrocell connections in an I/O cell.

sysIO Banks

The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) an voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri- buffer, a programmable input buffer, and programmable bus-maintenance circuitry.

The I/O cell receives inputs from its associated macrocells and the device pin. The I/O cell has a feedba associated macrocells and a direct path to GRP. The output enable (OE) MUX selects the OE signal The inputs to the OE MUX are the four global PTOE signals, PTOE and the two GOE signals. The O has the ability to choose either the true or inverse of each of these signals. The output of the OE MUX g a logical AND with the TOE signal to allow easy tri-stating of the outputs for testing purposes. The grouped into segments of four for the purpose of generating Shared PTOE signals. Each Shared PT derived from PT 163 from one of the four MFBs. Table 10 shows the segments. The PTOE signal is d the first product term in each macrocell cluster, which is directly routed to the OE MUX. Therefore, ev can have a different OE signal. Figure 17 is a graphical representation of the I/O cell.

Figure 17. I/O Cell

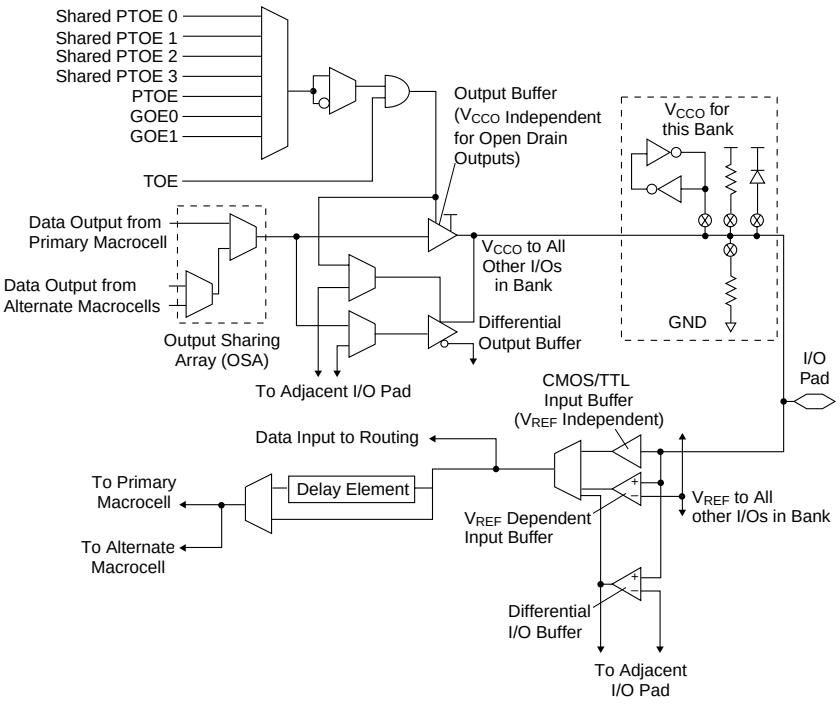


Table 10. Shared PTOE Segments

Device	MFBs Associated With Segments
ispXPLD 5256MX	(A, B, C, D) (E, F, G, H)
ispXPLD 5512MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P)
ispXPLD 5768MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z)
ispXPLD 51024MX	(A, B, C, D) (E, F, G, H) (I, J, K, L) (M, N, O, P) (Q, R, S, T) (U, V, W, Z) (Y, Z, AA, AB) (AC, AD, AE, AF)

sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some sta require the use of an external termination voltage. Table 12 lists the sysIO standards with the typica $V_{CCO,}$ V_{REF} and $V_{TT.}$ For more information on the sysIO capability, please refer to Lattice technical n TN1000, *sysIO Usage Guidelines for Lattice Devices,* available at www.latticesemi.com.

Table 11. Number of I/Os per Bank

Device	Maximum Number of I/Os per Bank (n)
ispXPLD 5256MX	36
ispXPLD 5512MX	68
ispXPLD 5768MX	96
ispXPLD 51024MX	96

Table 12. ispXPLD 5000MX Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75V
HSTL, Class IV	1.5V	0.9V	0.75V
GTL+	N/A	1.0V	1.5V
LVPECL, Differential	2.5V, 3.3V	N/A	N/A
LVDS	2.5V, 3.3V	N/A	N/A

Table 13. Differential Interface Standard Support[1]

		sysIO Buffer
LVDS	Driver	Supported
	Receiver	Supported with standard termination
LVPECL	Driver	Supported with external resistor network
	Receiver	Supported with termination

1. For more information, refer to Lattice technical note TN1000, *sysIO Usage Guidelines for Lattice Devices,* available
www.latticesemi.com.

Control, Clock, sysCONFIG and JTAG Signals

Global clock pins support the same sysIO standards as general purpose I/O. When required the V_R
derived from the adjacent bank. When differential standards are supported two adjacent clock pins a
form the input. The TOE, PROGRAM, CFG0 and DONE pins of the ispXPLD 5000MX device are the o
do not have sysIO capabilities. The JTAG TAP pins support only LVCMOS 3.3, 2.5 and 1.8V standards.
is controlled by $V_{CCJ.}$ These pins only support the LVTTL and LVCMOS standards applicable to the p
voltage of the device. The global reset global output enable pins are associated with Bank 2 and supp
sysIO standards.

Hotsocketing

The I/O on the ispXPLD 5000MX devices are well suited for those applications that require hot socketin
when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powere
tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the e
powered-down device be minimal on active signals.

Programmable Drive Strength

The drive strength of I/Os that are programmed as LVCMOS is tightly controlled and can be programm
ety of different values. Thus the impedance an output driver can be closely match to the characteristic
of the line it is driving. This allows users to eliminate the need for external series termination resistors.

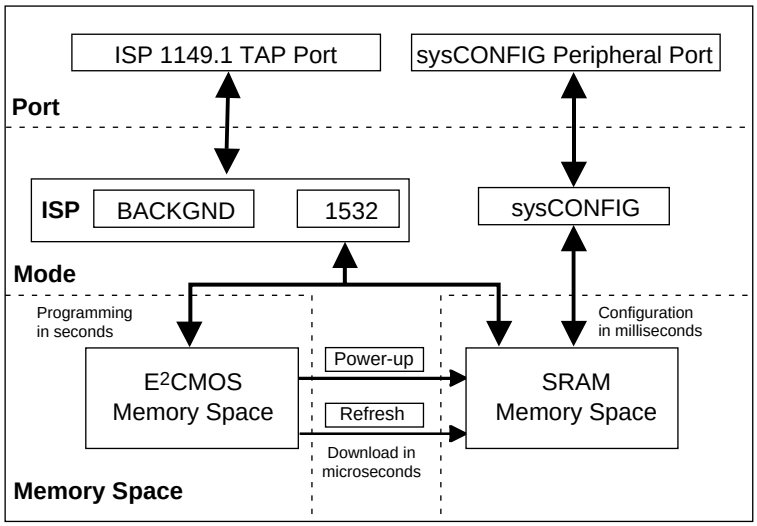
Programmable Slew Rate
The slew rate of outputs is carefully controlled. When outputs are configured as LVCMOS the devices slew rates. This allows system noise and performance to be balanced in a design.

Programmable Bus-Maintenance
All general-purpose inputs have programmable bus maintenance circuitry. These are intended to mai logic level into a device when driving devices go into the tri-state mode. Four options are available for up, pull-down, bus-keeper, or nothing.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technolo a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capa nite reconfiguration. A non-volatile array distributed within the device stores the device configuration. this information is transferred in a massively parallel fashion into SRAM bits that control the operation o Figure 18 shows the different ports and modes that are used in the configuration and programming of t 5000MX devices.

Figure 18. ispXP Block Diagram



IEEE 1532 ISP

In-system programming of devices provides a number of significant benefits including rapid prototy inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX dev in-system programmability through their Boundary Scan Test Access Port. This capability has been imp a manner that ensures that the port remains compliant to the IEEE 1532 standard. By using IEEE communication interface through which ISP is achieved, customers get the benefit of a standard, well-d face.

The IEEE1532 programming interface allows programming of either the non-volatile array or reconfigu SRAM bits.

The ispXPLD 5000MX devices can be programmed across the commercial temperature and voltage PC-based Lattice software facilitates in-system programming of ispXPLD 5000MX devices. The softwa JEDEC file output produced by the design implementation software, along with information about the and creates a set of vectors used to drive the scan chain. The software can use these vectors to drive a via the parallel port of a PC. Alternatively, the software can output files in formats understood by co mated test equipment. This equipment can then be used to program ispXPLD 5000MX devices during of a circuit board.

sysCONFIG Interface

In addition to being able to program the device through the IEEE 1532 interface a microprocessor sty (sysCONFIG interface) allows reconfiguration of the SRAM bits within the device. For more informa sysCONFIG capability, please refer to technical note number TN1026, *ispXP Configuration Usage Guid*

Security Scheme

A programmable security scheme is provided on the ispXPLD 5000MX devices as a deterrent to u copying of the array configuration patterns. Once programmed, this bit prevents readback of the progr tern by a device programmer, securing proprietary designs from competitors. The security bit also p gramming and verification. The entire device must be erased in order to erase the security bit.

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provid power consumption. The 1.8V core reduces dynamic power consumption compared with devices with voltages. For information on estimating power consumption, please refer to Lattice technical note numb *Power Estimation in ispXPLD 5000MX Devices.*

Density Migration

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same pa compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing desig from lower density parts to higher density parts. In many cases, it is possible to shift a lower utilization geted for a high-density device to a lower density device. However, the exact details of the final resourc will impact the likely success in each case.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 sta allows functional testing of the circuit board on which the device is mounted through a serial scan pa access all critical logic notes. Internal boundary scan registers are linked internally, allowing test data t in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. these devices can be linked into a board-level serial scan path for board-level testing. The test access own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

sysIO Quick Configuration

To facilitate the most efficient board test, the physical nature of the I/O cells must be set before running a ity tests. As these tests are fast, by nature, the overhead and time that is required for configuration physical nature should be minimal so that board test time is minimized. The ispXPLD 5000MX family allows this by offering the user the ability to quickly configure the physical nature of the sysIO cells. Thi figuration takes milliseconds to complete, whereas it takes seconds for the entire device to be progra tice's ispVM™ System programming software can either perform the quick configuration through the port, or can generate the ATE or test vectors necessary for a third-party test system.

Absolute Maximum Ratings[1, 2, 3]

	ispXPLD 5000MC 1.8V	ispXPLD 5000MB/V 2.5V/3.3V
Supply Voltage (V_{CC})	-0.5 to 2.5V	-0.5 to 5.5V
PLL Supply Voltage (V_{CCP})	-0.5 to 2.5V	-0.5 to 5.5V
Output Supply Voltage (V_{CCO})	-0.5 to 4.5V	-0.5 to 4.5V
IEEE 1149.1 TAP Supply Voltage (V_{CCJ})	-0.5 to 4.5V	-0.5 to 4.5V
Input Voltage Applied[4, 5]	-0.5 to 5.5V	-0.5 to 5.5V
Storage Temperature	-65 to 150°C	-65 to 150°C
Junction Temperature (T_J) with Power Applied	-55 to 150°C	-55 to 150°C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the devic operation of the device at these or any other conditions above those indicated in the operational sections of this is not implied (while programming, following the programming specifications).
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and Undershoot of -2V to (V_{IHMAX} +2) volts not to exceed 6V is permitted for a duration of <20ns.
5. A maximum of 64 I/Os per device with V_{IN} > 3.6V is allowed.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.
V_{CC}	Supply Voltage for 1.8V Devices (ispXPLD 5000MC)	1.65	1.95
	Supply Voltage for 2.5V Devices (ispXPLD 5000MB)	2.3	2.7
	Supply Voltage for 3.3V Devices (ispXPLD 5000MV)	3	3.6
V_{CCP}	PLL Block Supply Voltage for PLL 1.8V Devices	1.65	1.95
	PLL Block Supply Voltage for PLL 2.5V Devices	2.3	2.7
	PLL Block Supply Voltage for PLL 3.3V Devices	3	3.6
T_J	Junction Temperature (Commercial Operation)	0	90
	Junction Temperature (Industrial Operation)	-40	105

E²CMOS Erase Reprogram Specifications

Parameter	Min.	Max.
Erase/Reprogram Cycle[1]	1,000	—

1. Valid over commercial temperature range.

Hot Socketing Characteristics[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.
I_{DK}	Input or I/O Leakage Current	0 ≤ V_{IN} ≤ 3.0V	—	+/-50	+/-800

1. Insensitive to sequence of V_{CC} and V_{CCO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCO}, provided (V_{IN} - V_{CC}
2. 0 ≤ V_{CC} ≤ V_{CC} (MAX), 0 ≤ V_{CCO} ≤ V_{CCO} (MAX)
3. I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}. Device defaults to pull-up until non-volatile cells are active.
4. LVTTL, LVCMOS only.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Ma
I_{IL}, I_{IH}[1]	Input or I/O Leakage	$0 \le V_{IN} \le (V_{CCO} - 0.2V)$	—	—	10
		$(V_{CCO} - 0.2V) < V_{IN} \le 3.6V$	—	—	40
I_{IH}[4]	Input High Leakage Current	$3.6V < V_{IN} \le 5.5V$ and $3.0V \le V_{CCO} \le 3.6V$	—	—	3
I_{PU}[3]	I/O Active Pullup Current	$0 \le V_{IN} \le 0.7\ V_{CCO}$	-30	—	-15
I_{PD}	I/O Active Pulldown Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	15
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCO}$	30	—	—
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	15
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	15
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{CCO} * 0.35	—	V_{CCO} *
C1	I/O Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—
C2	Clock Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—
C3	Global Input Capacitance[2]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is
with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f=1.0MHz
3. I_{PU} on JTAG pins has a maximum of -175µA for 5512MX devices.
4. 5V tolerant inputs and I/Os should be placed in banks where $3.0V \le V_{CCO} \le 3.6V$. The JTAG and sysCONFIG ports are not in
5V tolerant interface.

Supply Current

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.
ispXPLD 5256					
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	26	—
		V_{CC} = 2.5V, f = 1.0MHz	—	26	—
		V_{CC} = 1.8V, f = 1.0MHz	—	16	—
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—
		V_{CCP} = 2.5V, f = 10MHz	—	11	—
		V_{CCP} = 1.8V, f = 10MHz	—	3	—
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—
		V_{CCJ} = 2.5V	—	1	—
		V_{CCJ} = 1.8V	—	1	—
ispXPLD 5512					
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	33	—
		V_{CC} = 2.5V, f = 1.0MHz	—	33	—
		V_{CC} = 1.8V, f = 1.0MHz	—	22	—
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—
		V_{CCP} = 2.5V, f = 10MHz	—	11	—
		V_{CCP} = 1.8V, f = 10MHz	—	3	—
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—
		V_{CCJ} = 2.5V	—	1	—
		V_{CCJ} = 1.8V	—	1	—
ispXPLD 5768					
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	40	—
		V_{CC} = 2.5V, f = 1.0MHz	—	40	—
		V_{CC} = 1.8V, f = 1.0MHz	—	30	—
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—
		V_{CCP} = 2.5V, f = 10MHz	—	11	—
		V_{CCP} = 1.8V, f = 10MHz	—	3	—
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—
		V_{CCJ} = 2.5V	—	1	—
		V_{CCJ} = 1.8V	—	1	—

Supply Current (Continued)

Symbol	Parameter	Condition	Min.	Typ.[3]	Max.
ispXPLD 51024					
I_{CC}[1,2]	Operating Power Supply Current	V_{CC} = 3.3V, f = 1.0MHz	—	75	—
		V_{CC} = 2.5V, f = 1.0MHz	—	75	—
		V_{CC} = 1.8V, f = 1.0MHz	—	55	—
I_{CCO}	Standby Power Supply Current (per I/O Bank)	V_{CCO} = 3.3V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 2.5V, f = 1.0MHz, unloaded	—	4	—
		V_{CCO} = 1.8V, f = 1.0MHz, unloaded	—	3	—
I_{CCP}	PLL Power Supply Current (per PLL Bank)	V_{CCP} = 3.3V, f = 10MHz	—	11	—
		V_{CCP} = 2.5V, f = 10MHz	—	11	—
		V_{CCP} = 1.8V, f = 10MHz	—	3	—
I_{CCJ}	Standby IEEE 1149.1 TAP Power Supply Current	V_{CCJ} = 3.3V	—	1	—
		V_{CCJ} = 2.5V	—	1	—
		V_{CCJ} = 1.8V	—	1	—

1. Device configured with 16-bit counters.
2. ICC varies with specific device configuration and operating frequency.
3. T_A = 25°C

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[2]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	
LVCMOS 3.3	3.0	3.3	3.6	—	—	
LVCMOS 2.5	2.3	2.5	2.7	—	—	
LVCMOS 1.8[1]	1.65	1.8	1.95	—	—	
LVTTL	3.0	3.3	3.6	—	—	
PCI 3.3	3.0	3.3	3.6	—	—	
AGP-1X	3.15	3.3	3.45	—	—	
SSTL 2	2.3	2.5	2.7	1.15	1.25	
SSTL 3	3.0	3.3	3.6	1.3	1.5	
CTT 3.3	3.0	3.3	3.6	1.35	1.5	
CTT 2.5	2.3	2.5	2.7	1.35	1.5	
HSTL Class I	1.4	1.5	1.6	0.68	0.75	
HSTL Class III	1.4	1.5	1.6	—	0.9	
HSTL Class IV	1.4	1.5	1.6	—	0.9	
GTL+	1.4	—	3.6	0.882	1.0	
LVDS	2.3	2.5/3.3	3.6	—	—	

1. Design tools default setting.
2. Inputs are independent of V_{CCO} setting. However, V_{CCO} must be set within the valid operating range for one of the supported

sysIO Single Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL}[2] (mA)
	Min (V)	Max (V)	Min (V)	Max (V)			
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	2.4	20, 16, 12, 8, 5.33, 4
					0.2	V_{CCO} - 0.2	0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	2.4	4
					0.2	V_{CCO} - 0.2	0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4
					0.2	V_{CCO} - 0.2	0.1
LVCMOS 1.8[1, 3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} - 0.4	8
LVCMOS 1.8[3]	-0.3	0.68	1.07	3.6	0.4	V_{CCO} -0.4	12, 5.33, 4
					0.2	V_{CCO} - 0.2	0.1
PCI 3.3[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5
AGP-1X[4]	-0.3	1.08	1.5	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5
SSTL3 class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8
SSTL3 class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16
SSTL2 class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6
SSTL2 class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8
CTT 2.5	-0.3	V_{REF} - 0.3	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8
HSTL class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8
HSTL class III	-0.3	V_{REF} - 0.2	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24
HSTL class IV	-0.3	V_{REF} - 0.3	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	n/a	36

1. Software default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank ar the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between connections or between the last GND in a bank and the end of a bank.
3. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.35 * V_{CC} and V_{IH} = 0.65 * V_{CC}.
4. For 1.8V devices (ispXPLD 5000MC) these specifications are V_{IL} = 0.3 * V_{CC} * 3.3/1.8, V_{IH} = 0.5 * V_{CC} * 3.3/1.8.

sysIO Differential DC Electrical Characteristics

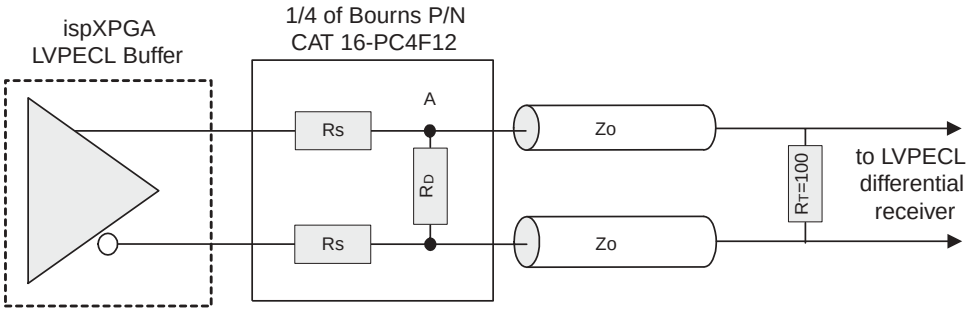
Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.
LVDS				
V_{INP}	Input Voltage		0V	—
V_{THD}	Differential Input Threshold	$0.2 \le V_{CM} \le 1.8V$	+/-100mV	—
I_{IN}	Input Current	Power On	—	—
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V
V_{OD}	Output Voltage Differential	$(V_{OP} - V_{OM})$, R_T = 100 Ohm	250mV	350mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—
V_{OS}	Output Voltage Offset	$(V_{OP} - V_{OM})/2$, R_T = 100 Ohm	1.125V	1.20V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—
I_{OSD}	Output Short Circuit Current	V_{OD} = 0V Driver outputs shorted	—	—

LVPECL[1]							
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**
V_{CCO}		**3.0**		**3.3**		**3.6**	
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125
V_{OH}	Output Voltage High	1.7	2.11	1.92	2.28	2.03	2.41
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57
V_{DIFF}[2]	Differential Input voltage	0.3	—	0.3	—	0.3	—

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see
The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common m
2. Valid for $0.2 \le V_{CM} \le 1.8V$

Figure 19. LVPECL Driver with Three Resistor Pack



ispXPLD 5000MX Family External Switching Characteristics [1, 2, 3]

Over Recommended Operating Conditions

Parameter	Description	-4		-45		-5		-52		-75	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	
t_{PD}	Data Propagation Delay, 5-PT Bypass	—	4.0	—	4.5	—	5.0	—	5.2	—	
t_{PD_PTSA}	Data propagation delay	—	4.8	—	5.7	—	6.0	—	6.5	—	
t_S	MFB Register Setup Time Before Clock, 5-PT Bypass	2.2	—	2.8	—	2.8	—	3.0	—	4.5	
t_{S_PTSA}	MFB Register Setup Time Before Clock	2.5	—	3.1	—	3.1	—	3.6	—	5.5	
t_{SIR}	MFB Register Setup Time Before Clock, Input Register Path	1.0	—	1.0	—	1.0	—	0.5	—	1.7	
t_H	MFB Register Hold Time Before Clock, 5-PT Bypass	0.0	—	0.0	—	0.0	—	0.0	—	0.0	
t_{H_PTSA}	MFB Register Hold Time Before Clock	0.0	—	0.0	—	0.0	—	0.0	—	0.0	
t_{HIR}	MFB Register Hold Time Before Clock, Input Register Path	0.5	—	0.5	—	0.5	—	1.0	—	1.3	
t_{CO}	MFB Register Clock-to-Output Delay	—	2.8	—	3.0	—	3.2	—	3.7	—	
t_R	External Reset Pin to Output Delay	—	4.0	—	4.5	—	5.0	—	5.0	—	
t_{RW}	Reset Pulse Duration	1.8	—	1.8	—	1.8	—	2.0	—	3.0	
$t_{LPTOE/DIS}$	Input to Output Local Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	
$t_{SPTOE/DIS}$	Input to Output Shared Product Term Output Enable/Disable	—	6.0	—	7.0	—	7.5	—	8.5	—	
$t_{GOE/DIS}$	Global OE Input to Output Enable/Disable	—	4.5	—	5.5	—	5.5	—	6.5	—	
t_{CW}	Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	
t_{GW}	Gate Width Low (for Low Transparent) or High (for High Transparent)	1.5	—	1.5	—	1.5	—	1.8	—	2.5	
t_{WIR}	Input Register Clock Width, High or Low	1.5	—	1.5	—	1.5	—	1.8	—	2.5	
t_{SKEW}	Clock-to-Out Skew, Block Level	—	0.6	—	0.6	—	0.6	—	0.6	—	
f_{MAX} [4]	Clock Frequency with Internal Feedback	—	300	—	275	—	250	—	250	—	
f_{MAX} (Ext.)	Clock Frequency with External Feedback, $1/(t_S + t_{CO})$	—	200	—	171	—	166	—	149	—	
f_{MAX} (Tog.)	Clock Frequency Max. Toggle	—	333	—	333	—	333	—	277	—	
f_{MAX} (CAMC) [5]	Clock Frequency to CAM (Configure Mode)	—	280	—	280	—	230	—	230	—	
f_{MAX} (CAM) [5]	Clock Frequency to CAM (Compare Mode)	—	150	—	150	—	150	—	135	—	

ispXPLD 5000MX Family External Switching Characteristics (Continu

Over Recommended Operating Conditions

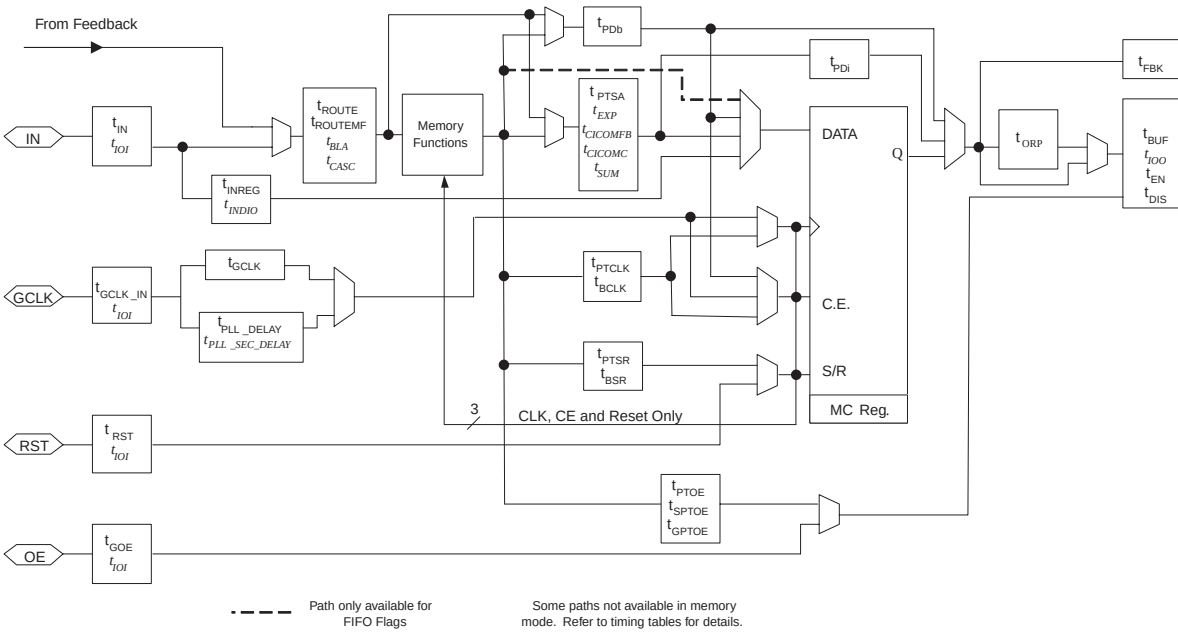
Parameter	Description	-4		-45		-5		-52		-75
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
f_{MAX} (RAM)[5]	Clock Frequency to RAM in:									
	Single Port Mode	—	155	—	155	—	155	—	155	—
	Dual Port Mode	—	155	—	155	—	155	—	155	—
	Pseudo Dual Port Mode	—	180	—	180	—	160	—	160	—
f_{MAX} (FIFO)[5]	Clock Frequency to FIFO	—	225	—	220	—	210	—	210	—
t_{PWR_ON}	Power-on Time	—	200	—	200	—	200	—	200	—

1. Timing numbers are based on default LVCMOS 1.8 I/O buffers. Use timing adjusters provided to calculate timing for other sta
2. Measured using standard switching circuit, global routing loading of 1, worst case PTSA loading and 1 output switching.
3. Pulse widths and clock widths less than minimum will cause unknown behavior.
4. Standard 16-bit counter using GRP feedback.
5. CAM, FIFO, RAM f_{MAX} specification used shared PT Clk.

Timing Model

The task of determining timing in a ispXPLD 5000MX device is relatively simple. The timing mo Figure 20 shows the specific delay paths. Once the implementation of a given function is determined ceptually or from the software report file, the delay path of a function can easily be determined fro model. The Lattice design tools report the timing delays based on the same timing model. Note that int parameters are for reference only, and are not tested. The external timing parameters are tested and for every device.

Figure 20. ispXPLD 5000MX Timing Model Diagram



ispXPLD 5000MX Family Internal Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
In/Out Delays											
t_{IN}	Input Buffer Delay	—	—	0.70	—	0.91	—	0.96	—	1.11	—
t_{GCLK_IN}	Global Clock Input Buffer Delay	—	—	0.40	—	0.35	—	0.35	—	0.35	—
t_{RST}	Global RESET Pin Delay	—	—	3.77	—	4.24	—	4.71	—	4.71	—
t_{GOE}	Global OE Pin Delay	—	—	1.98	—	2.66	—	2.34	—	2.87	—
t_{BUF}	Delay through Output Buffer	—	—	1.16	—	1.30	—	1.45	—	1.60	—
t_{EN}	Output Enable Time	—	—	2.52	—	2.84	—	3.16	—	3.63	—
t_{DIS}	Output Disable Time	—	—	1.92	—	2.40	—	2.40	—	2.40	—
Routing Delays											
t_{ROUTE}	Delay through SRP	—	—	1.95	—	2.06	—	2.34	—	2.24	—
t_{INREG}	Input Buffer to Macrocell Register Delay	—	—	0.60	—	0.60	—	0.60	—	0.47	—
t_{PTSA}	Product Term Sharing Array Delay	—	—	0.50	—	0.50	—	0.53	—	0.83	—
t_{FBK}	Internal Feedback Delay	—	—	0.19	—	0.02	—	0.39	—	0.03	—
t_{GCLK}	Global Clock Tree Delay	—	—	0.52	—	0.32	—	0.72	—	0.82	—
t_{BCLK}	Block PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—
t_{PTCLK}	Macrocell PT Clock Delay	—	—	0.12	—	0.14	—	0.15	—	0.15	—
t_{PLL_DELAY}	Programmable PLL Delay Increment	—	—	0.30	—	0.30	—	0.30	—	0.30	—
t_{BSR}	Block PT Reset Delay	—	—	0.72	—	0.81	—	0.90	—	0.94	—
t_{PTSR}	Macrocell PT Set/ Reset Delay	—	—	0.60	—	0.75	—	0.75	—	0.75	—
t_{LPTOE}	Macrocell PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—
t_{SPTOE}	Segment PT OE Delay	—	—	0.83	—	1.19	—	1.04	—	1.52	—
t_{OSA}	Output Sharing Array Delay	—	—	0.80	—	0.90	—	1.00	—	1.00	—
t_{PTOE}	Global PT OE Delay	—	—	0.83	—	1.04	—	1.04	—	1.04	—
t_{PDB}	5-PT Bypass Propagation Delay	—	—	0.20	—	0.23	—	0.25	—	0.25	—
t_{PDI}	Macrocell Propagation Delay	—	—	0.50	—	0.93	—	0.72	—	0.72	—

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
Registered Delays											
t_S	D-Register Setup Time, Global Clock	—	0.28	—	0.31	—	0.35	—	0.55	—	0.52
t_{S_PT}	D-Register Setup Time, PT Clock	—	-0.13	—	-0.11	—	-0.10	—	-0.10	—	-0.07
t_H	D-Register Hold Time	—	1.90	—	2.56	—	2.50	—	2.40	—	4.00
t_{COi}	Register Clock to OSA Time	—	—	0.72	—	1.03	—	0.68	—	0.93	—
t_{CESi}	Clock Enable Setup Time	—	1.07	—	1.20	—	1.33	—	1.33	—	2.00
t_{CEHi}	Clock Enable Hold Time	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00
t_{SIR}	D-Input Register Setup Time, Global Clock	—	0.66	—	0.20	—	0.53	—	0.12	—	0.08
t_{SIR_PT}	D-Input Register Setup Time, PT Clock	—	0.42	—	0.37	—	0.34	—	0.34	—	0.22
t_{HIR}	D-Input Register Hold Time, Global Clock	—	0.84	—	1.31	—	1.01	—	1.41	—	2.91
t_{HIR_PT}	D-Input Register Hold Time, PT Clock	—	0.00	—	0.00	—	0.00	—	0.00	—	0.00
Latched Delays											
t_{SL}	Latch Setup Time, Global Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.00
t_{SL_PT}	Latch Setup Time, PT Clock	—	0.18	—	0.00	—	0.00	—	0.00	—	0.34
t_{HL}	Latch Hold Time	—	-0.06	—	0.00	—	0.00	—	0.00	—	-0.03
t_{GOi}	Latch Gate to OSA Time	—	—	0.07	—	0.08	—	0.08	—	0.08	—
t_{PDLi}	Propagation Delay through Latch to OSA Transparent	—	—	0.52	—	0.58	—	0.65	—	0.65	—
Reset and Set Delays											
t_{SRi}	Asynchronous Reset or Set to OSA Delay	—	—	0.23	—	0.26	—	0.29	—	0.29	—
t_{SRR}	Asynchronous Reset or Set Recovery	—	—	0.42	—	0.47	—	0.53	—	0.55	—
eXtended Function Routing Delays											
$t_{ROUTEMF}$	Delay through SRP when Implementing Memory Functions	—	—	2.00	—	2.25	—	2.51	—	2.61	—

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
t_{CASC}	Additional Delay for PT Cascading between MFBs	—	—	0.71	—	0.80	—	0.89	—	0.92	—
$t_{CICOMFB}$	Carry Chain Delay, MFB to MFB	—	—	0.35	—	0.39	—	0.44	—	0.46	—
t_{CICOMC}	Carry Chain Delay, Macro-Cell to Macro-Cell	—	—	0.10	—	0.11	—	0.13	—	0.13	—
t_{FLAG}	Routing Delay for Extended Function Flags	—	—	2.62	—	2.94	—	3.27	—	3.40	—
$t_{FLAGEXP}$	Additional Flag Delay when Expanding Data Widths	$t_{FLAGFULL}$, $t_{FLAGAFULL}$, $t_{FLAGEMPTY}$, $t_{FLAGAEMPTY}$	—	2.57	—	2.89	—	3.21	—	3.34	—
t_{SUM}	Counter Sum Delay	t_{PTSA}	—	0.80	—	0.90	—	1.00	—	1.04	—
Optional Adjusters											
t_{BLA}	Block Loading Adder	t_{ROUTE}	—	0.04	—	0.04	—	0.05	—	0.05	—
t_{EXP}	PT Expander Adder	t_{ROUTE}	—	0.53	—	0.60	—	0.66	—	0.69	—
t_{INDIO}	Additional Delay for the Input Register	t_{INREG}	—	0.50	—	0.56	—	0.63	—	0.65	—
$t_{PLL\_SEC\_DELAY}$	Secondary PLL Output Delay	t_{PLL_DELAY}	—	0.91	—	0.91	—	0.91	—	0.91	—
t_{INEXP}	MFB Input Extender	t_{ROUTE}	—	0.62	—	0.70	—	0.78	—	0.81	—
Input and Output Buffer Delays											
t_{IOI}	Input Buffer Selection Adder	t_{GCLK_IN}, t_{IN}, t_{GOE}, t_{RST}	Refer to sysIO Adjuster Tables								
t_{IOO}	Output Buffer Selection Adder	t_{BUF}									
FIFO											
$t_{FIFOWCLKS}$	Write Data Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{FIFOWCLKH}$	Write Data Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{FIFOCLKSKEW}$	Opposite Clock Cycle Delay	—	—	1.40	—	1.40	—	1.76	—	1.76	—
$t_{FIFOFULL}$	Write Clock to Full Flag Delay	—	—	3.08	—	3.08	—	3.85	—	3.85	—
$t_{FIFOAFULL}$	Write Clock to Almost Full Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—
$t_{FIFOEMPTY}$	Read Clock to Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—
$t_{FIFOAEMPTY}$	Read Clock to Almost Empty Flag Delay	—	—	3.08	—	3.08	—	3.86	—	3.86	—

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
$t_{FIFOWES}$	Write-Enable setup before Write Clock	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03
$t_{FIFOWEH}$	Write-Enable hold after Write Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27
$t_{FIFORES}$	Read-Enable setup before Read Clock	—	2.69	—	2.35	—	2.79	—	2.38	—	4.14
$t_{FIFOREH}$	Read-Enable hold after Read Clock	—	-3.17	—	-3.17	—	-2.53	—	-2.53	—	-2.44
$t_{FIFORSTO}$	Reset to Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—
$t_{FIFORSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56
$t_{FIFORSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19
$t_{FIFORCLKO}$	Read Clock to FIFO Out Delay	—	—	3.73	—	3.73	—	4.66	—	4.66	—
CAM – Update Mode											
t_{CAMMSS}	Memory Select Setup before CLK	—	1.40	—	0.70	—	1.50	—	1.40	—	1.44
t_{CAMMSH}	Memory Select Hold after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before CLK	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after CLK	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{CAMADDS}$	Address Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{CAMADDH}$	Address Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{CAMDCS}	“Don’t Care” Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
t_{CAMDCH}	“Don’t Care” Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{CAMRWS}	R/W Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
t_{CAMRWH}	R/W Enable Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{CAMCES}	Clock Enable Setup Time before Clock	—	1.55	—	1.55	—	1.94	—	1.94	—	2.02
t_{CAMCEH}	Clock Enable Hold Time after Clock	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
$t_{CAMWMSKS}$	Write Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{CAMWMSKH}$	Write Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{CAMRSTO}$	Reset to CAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—
$t_{CAMRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56
$t_{CAMRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19
CAM – Compare Mode											
$t_{CAMDATAS}$	Data Setup Time before Clock	—	-0.41	—	-0.41	—	-0.33	—	-0.33	—	-0.31
$t_{CAMDATAH}$	Data Hold Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{CAMENMSKS}$	Enable Mask Register Setup Time before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{CAMENMSKH}$	Enable Mask Register Setup Time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{CAMCASC}$	CAM Width Expansion Delay	—	—	0.40	—	0.40	—	0.50	—	0.50	—
t_{CAMCO}	Clock to Output (Address Out) Delay	—	—	6.19	—	6.13	—	6.81	—	6.61	—
$t_{CAMMATCH}$	Clock to Match Flag Delay	—	—	6.19	—	6.13	—	6.07	—	6.61	—
$t_{CAMMMATCH}$	Clock to Multi-Match Flag Delay	—	—	5.50	—	5.50	—	6.38	—	6.38	—
$t_{CAMRSTFLAG}$	CAM Reset to Flags Delay	—	—	3.16	—	3.16	—	3.95	—	3.95	—
Single Port RAM											
$t_{SPADDDATA}$	Address to Data Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—
t_{SPMSS}	Memory Select Setup Before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
t_{SPMSH}	Memory Select Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{SPCES}	Clock Enable Setup before Clock Time	—	2.30	—	2.30	—	2.30	—	2.30	—	9.80
t_{SPCEH}	Clock Enable Hold time after Clock Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27
t_{SPADDS}	Address Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
t_{SPADDH}	Address Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{SPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
t_{SPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{SPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
$t_{SPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{SPCLKO}	Clock to Output Delay	—	—	5.97	—	5.97	—	5.97	—	5.97	—
t_{SPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—
t_{SPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56
$t_{SPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19
Pseudo Dual Port RAM											
t_{PDPMSS}	Memory Select Setup Before Clock	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
t_{PDPMSH}	Memory Select Hold time after Clock	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{PDPRCES}$	Clock Enable Setup before Read Clock Time	—	2.33	—	2.33	—	2.91	—	2.91	—	3.03
$t_{PDPRCEH}$	Clock Enable Hold time after Read Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27
$t_{PDPWCES}$	Clock Enable Setup before Write Clock Time	—	1.87	—	1.87	—	2.34	—	2.34	—	2.43
$t_{PDPWCEH}$	Clock Enable Hold time after Write Clock Time	—	-2.95	—	-2.95	—	-2.36	—	-2.36	—	-2.27
$t_{PDPRADDS}$	Read Address Setup before Read Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{PDPRADDH}$	Read Address Hold after Read Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{PDPWADDS}$	Write Address Setup before Write Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{PDPWADDH}$	Write Address Hold after Write Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{PDPRWS}	R/W Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
t_{PDPRWH}	R/W Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{PDPDATAS}$	Data Setup before Clock Time	—	-0.27	—	-0.27	—	-0.22	—	-0.22	—	-0.21
$t_{PDPDATAH}$	Data Hold time after Clock Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{PDPRCLKO}$	Read Clock to Output Delay	—	—	5.08	—	5.02	—	5.66	—	5.45	—
$t_{PDPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.76	—	1.76	—	1.83
$t_{PDPRSTO}$	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	4.13	—	4.13	—
$t_{PDPRSTR}$	Reset Recovery Time	—	1.20	—	1.20	—	1.50	—	1.50	—	1.56
$t_{PDPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.18	—	0.18	—	0.19
Dual Port RAM											
t_{DPMSAS}	Memory Select A Setup Before R/W A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
t_{DPMSAH}	Memory Select Hold time after R/W A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{DPCEAS}	Clock Enable A Setup before Clock A Time	—	3.72	—	3.72	—	3.72	—	3.72	—	4.84
t_{DPCEAH}	Clock Enable A Hold time after Clock A Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27
$t_{DPADDAS}$	Address A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
$t_{DPADDAH}$	Address A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{DPRWAS}	R/W A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
t_{DPRWAH}	R/W A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{DPDATAAS}$	Write Data A Setup before Clock A Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
$t_{DPDATAAH}$	Write Data A Hold time after Clock A Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{DPMSBS}	Memory Select B Setup Before R/W B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
t_{DPMSBH}	Memory Select Hold time after R/W B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01

ispXPLD 5000MX Family Internal Switching Characteristics (Continu

Over Recommended Operating Conditions

Parameter	Description	Base Parameter	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
t_{DPCEBS}	Clock Enable B Setup before Clock B Time	—	2.33	—	2.33	—	2.33	—	2.33	—	3.03
t_{DPCEBH}	Clock Enable Hold B after Clock B Time	—	-2.95	—	-2.95	—	-2.95	—	-2.95	—	-2.27
$t_{DPADDBS}$	Address B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
$t_{DPADDBH}$	Address B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
t_{DPRWBS}	R/W B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
t_{DPRWBH}	R/W B Hold time after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{DPDATABS}$	Write Data B Setup before Clock B Time	—	-0.27	—	-0.27	—	-0.27	—	-0.27	—	-0.21
$t_{DPDATABH}$	Write Data B Hold after Clock B Time	—	-0.01	—	-0.01	—	-0.01	—	-0.01	—	-0.01
$t_{DPRCLKAO}$	Read Clock A to Output Delay	—	—	5.97	—	5.92	—	5.86	—	5.65	—
$t_{DPRCLKBO}$	Read Clock B to Output Delay	—	—	5.16	—	5.16	—	5.16	—	5.16	—
$t_{DPCLKSKEW}$	Opposite Clock Cycle Delay	—	1.40	—	1.40	—	1.40	—	1.40	—	1.83
t_{DPRSTO}	Reset to RAM Output Delay	—	—	3.30	—	3.30	—	3.30	—	3.30	—
t_{DPRSTR}	Reset Recovery Time	—	1.20	—	1.20	—	1.20	—	1.20	—	1.56
$t_{DPRSTPW}$	Reset Pulse Width	—	0.14	—	0.14	—	0.14	—	0.14	—	0.19

1. The PT-delay to clock of RAM/FIFO/CAM should be t_{BCLK} instead of t_{PTCLK}.
2. The PT-delay to set/reset of RAM/FIFO/CAM should be t_{BSR} instead of t_{PTSR}.

ispXPLD 5000MX Family Timing Adders

Parameter	Description	Base Param.	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
t_{IOI} Input Adjusters											
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	—	0.0	—
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—
HSTL_IV_in	Using HSTL 2.5V, Class IV	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	—	1.0	—
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	—	0.5	—
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.6	—	0.6	—	0.6	—	0.6	—
t_{IOO} Output Adjusters – Output Signal Modifiers											
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs Only)	t_{IOBUF}, t_{IOEN}	—	0.9	—	0.9	—	0.9	—	0.9	—
t_{IOO} Output Adjusters – Output Configurations											
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	—	0.0	—
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	—	1.0	—
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—
LVCMOS_33_4mA_out	Using 3.3V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—
LVCMOS_33_5.33mA_out	Using 3.3V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.2	—	1.2	—	1.2	—	1.2	—
LVCMOS_33_8mA_out	Using 3.3V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—
LVCMOS_33_12mA_out	Using 3.3V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—
LVCMOS_33_16mA_out	Using 3.3V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—
LVCMOS_33_20mA_out	Using 3.3V CMOS Standard, 20mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—
AGP_1X_out	Using AGP 1x Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—
CTT25_out	Using CTT 2.5V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—
CTT33_out	Using CTT 3.3V	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—
GTL+_out	Using GTL+	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—

ispXPLD 5000MX Family Timing Adders (Continued)

Parameter	Description	Base Param.	-4		-45		-5		-52		-7
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.
HSTL_I_out	Using HSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—
HSTL_III_out	Using HSTL 2.5V, Class III	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—
HSTL_IV_out	Using HSTL 2.5V, Class IV	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—
LVDS_out	Using Low Voltage Differential Signaling (LVDS)	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	—	0.8	—
LVPECL_out	Using Low Voltage PECL	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—
PCI_out	Using PCI Standard	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	—	0.6	—
SSTL2_I_out	Using SSTL 2.5V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.3	—	0.3	—	0.3	—	0.3	—
SSTL2_II_out	Using SSTL 2.5V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	—	0.5	—
SSTL3_I_out	Using SSTL 3.3V, Class I	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	—	0.2	—
SSTL3_II_out	Using SSTL 3.3V, Class II	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.4	—	0.4	—	0.4	—	0.4	—

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Ma
t_{PWH}	Input clock, high time	80% to 80%	1.2	–
t_{PWL}	Input clock, low time	20% to 20%	1.2	–
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 2
f_{MDIVIN}	M Divider input, frequency range		10	32
$f_{MDIVOUT}$	M Divider output, frequency range		10	32
f_{NDIVIN}	N Divider input, frequency range		10	32
$f_{NDIVOUT}$	N Divider output, frequency range		10	32
f_{VDIVIN}	V Divider input, frequency range		100	40
$f_{VDIVOUT}$	V Divider output, frequency range		10	32
$t_{OUTDUTY}$	Output clock, duty cycle		40	60
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 2
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 1
$T_{JIT(PERIOD)}$[2]	Output clock, period jitter (peak)	Clean reference. 10 MHz < $f_{MDIVOUT}$ < 20 MHz or 100MHz < f_{VDIVIN} < 160 MHz[1]	—	+/- 3
		Clean reference. 20 MHz < $f_{MDIVOUT}$ < 320 MHz and 160MHz < f_{VDIVIN} < 320 MHz[1]	—	+/- 1
$t_{CLK\_OUT\_DLY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.
t_{PHASE}	Input clock to external feedback delta	External feedback	—	60
t_{LOCK}	Time to acquire phase lock after input stable		—	25
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 5
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3
t_{PLL_RSTW}	Minimum reset pulse width		—	1.
t_{CLK_IN}[3]	Global clock input delay		—	1.
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay (t_{PLL_DELAY})		—	1.

1. This condition assures that the output phase jitter will remain within specification.
2. Accumulated jitter measured over 10,000 waveform samples.
3. Internal timing for reference only.

ispXP sysCONFIG Port Timing Specifications

Symbol	Timing Parameter	Min.	Max.
sysCONFIG Write Cycle Timing			
t_{SUCS}	Input setup time of CS to CCLK rise	10	—
t_{HCS}	Hold time of CS to CCLK rise	1	—
t_{SUWD}	Input setup time of write data to CCLK rise	10	—
t_{HWD}	Hold time of write data to CCLK rise	0	—
t_{PRGM}	Low time to reset device SRAM	5	50
t_{DINIT}	INIT delay time	—	5
t_{IODISS}	User I/O disable	—	—
t_{IOENSS}	User I/O enable	—	—
t_{WH}	Write clock High pulse width	18	—
t_{WL}	Write clock Low pulse width	18	—
f_{MAXW}	Write f_{MAX}	—	27
sysCONFIG Read Cycle Timing			
t_{HREAD}	Hold time of READ to CCLK rise	1	—
t_{SUREAD}	Input setup time of READ High to CCLK rise	15	—
t_{RH}	READ clock high pulse width	18	—
t_{RL}	READ clock low pulse width	18	—
f_{MAXR}	Read f_{MAX}	—	27
t_{CORD}	Clock to out for read data	—	25

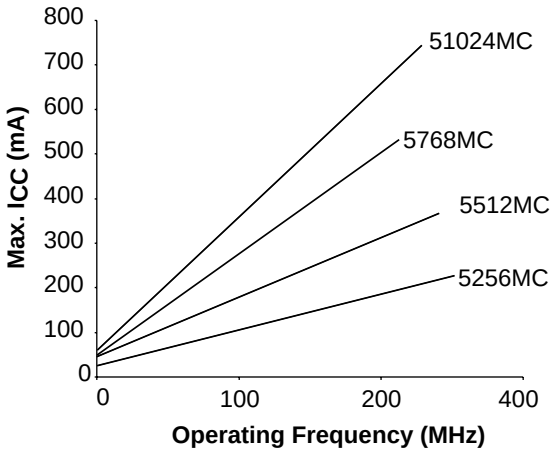
Boundary Scan Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min	Max
t_{BTCP}	TCK [BSCAN] clock pulse width	40	—
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—
t_{BTS}	TCK [BSCAN] setup time	8	—
t_{BTH}	TCK [BSCAN] hold time	10	—
t_{BTRF}	TCK [BSCAN] rise/fall time	50	—
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10
t_{BTCRS}	BSCAN test capture register setup time	8	—
t_{BTCRH}	BSCAN test capture register hold time	10	—
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25

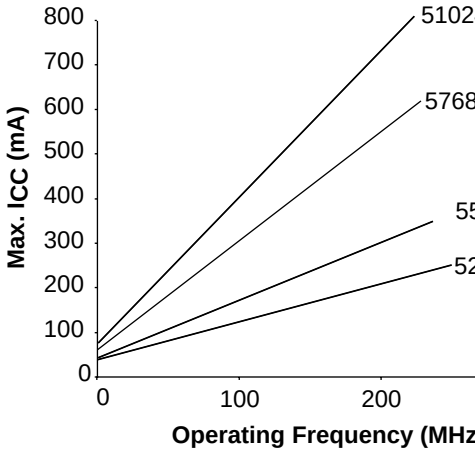
Power Consumption

ispXPLD 5000MC Typical I_{CC} vs. Frequency



Note: The device is configured with maximum number of 16-bit counters, no PLL, typical current at 1.8V, 25°C.

ispXPLD 5000MV/B Typical I_{CC} vs. Freq



Note: The device is configured with max number of 16-bit counters, no PLL, typic current at 3.3V (MV) or 2.5V (MB), 25°C

Power Estimation Coefficients

Device	K0	K1	K2	K3	K4	K5	K6	K7	DC ispXPLD 5000MC	DC i5
ispXPLD 5256	2.2	8.4	7	12	100	0.1379	0.0433	6.476	16	
ispXPLD 5512	2.2	8.4	9.4	18	151	0.1379	0.0433	6.476	17	
ispXPLD 5768	2.2	8.4	10.2	21	170	0.1379	0.0433	6.476	27	
ispXPLD 51024	2.2	8.4	13	27.6	200	0.1379	0.0433	6.476	35	

Note: For further information about the use of these coefficients, refer to technical note TN1031, *Power Estimation in ispXPL Devices.*

Memory Coefficients

Device	K8	K9	K10	K11
ispXPLD 5256	0.004719	0.0924	4.4	2.9
ispXPLD 5512	0.004719	0.0924	4.4	2.9
ispXPLD 5768	0.004719	0.0924	4.4	2.9
ispXPLD 51024	0.004719	0.0924	4.4	2.9

- K0 = Current per MFB input (µA/MHz)
- K1 = Current per Product Term (µA/MHz)
- K2 = Current per GRP from MFB (µA/MHz)
- K3 = Current per GRP from I/O (µA/MHz)
- K4 = Global clock tree current (µA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0Mhz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (µA/MHz)

- K11 = Current per column driver (µA/MHz)

Power Estimation Equations

ICC = ICC_DC + IMFB_CPLD + IMFB_ SRAM/PDPRAM/FIFO + IMFB_DPRAM + IMFB_CAM + IPLL

ICC_DC
Use the appropriate value for 5000MC (1.8V power supply) or 5000MV/B (2.5V/3.3V power supply) fr
sheet.

IMFB_CPLD
= ((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** *
from IFB) * AF+ **K4**) * FREQ / 1000µA/mA

IMFB_CAM
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

IMFB_ SRAM/PDPRAM/FIFO
= (WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (**K1** + 128 * RD_
* **K0** + 8 * OSW_PERCENT * **K2**)) * SRAM/PDPRAM/FIFO Memory MFBs * FREQ / 1000µA/mA

IMFB_ DPRAM
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1**
RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs * FREQ / 1000µA/mA

IPLL_D
= **K5** * PLL_FREQ * number of PLLs used. IPPL_D is the PLL digital component of the VCC supply cu

Analog portion of PLL supply current consumption, from PLL power pin:

IPLL_A = (**K6** * PLL_FREQ + **K7**) * number of PLLs used

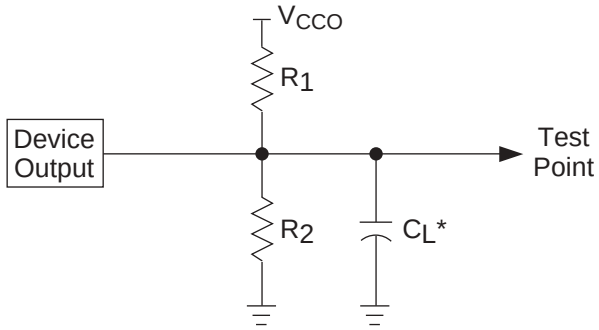
Notes:

- ICC = Current consumption of VCC power supply (mA)
- ICC-DC = ICC DC component – Current consumption at 0Mhz (mA)
- IMFB_CPLD = CPLD (non-memory logic) current consumption (mA)
- IMFB_SRAM/PDPRAM/FIFO = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- IMFB_DPRAM = Current consumption for DPRAM (mA)
- IMFB_CAM = Current consumption for CAM (mA)
- IPLL_D = PLL Current consumption of digital VCC power supply (mA)
- IPLL_A = PLL analog power pin current consumption (VCCP pin)

Switching Test Conditions

Figure 21 shows the output test load that is used for AC testing. The specific values for resistance, c
voltage, and other test conditions are shown in Table 14.

Figure 21. Output Test Load, LVTTL and LVCMOS Standards



*C_L includes test fixture and probe capacitance.

Table 14. Test Fixture Required Components

Test Condition	R_1	R_2	C_L	Timing Ref.	V_{CC}
Default LVCMOS 1.8 I/O (L -> H, H -> L)	106	106	35pF	$V_{CCO}/2$	1.8
LVCMOS I/O (L -> H, H -> L)	—	—	35pF	LVCMOS3.3 = 1.5V	LVCMOS3
				LVCMOS2.5 = $V_{CCO}/2$	LVCMOS2
				LVCMOS1.8 = $V_{CCO}/2$	LVCMOS1.
Default LVCMOS 1.8 I/O (Z -> H)	—	106	35pF	$V_{CCO}/2$	1.65
Default LVCMOS 1.8 I/O (Z -> L)	106	—	35pF	$V_{CCO}/2$	1.65
Default LVCMOS 1.8 I/O (H -> Z)	—	106	5pF	V_{OH} - 0.15	1.65
Default LVCMOS 1.8 I/O (L -> Z)	106	—	5pF	V_{OL} + 0.15	1.65

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Names	Descriptions
TMS	Input – This pin is the Test Mode Select input, which is used to control the I state machine.
TCK	Input – This pin is the Test Clock input pin, used to clock the IEEE 1149.1 s machine.
TDI	Input – This pin is the IEEE 1149.1 Test Data in pin, used to load data.
TDO	Output – This pin is the IEEE 1149.1 Test Data out pin used to shift data ou
TOE	Input – Test Output Enable pin. TOE tristates all I/O pins when driven low.
GOE0, GOE1	Input – Global output enable inputs.
RESET	Input – This pin resets all the registers in the device. The global polarity (ac active low) for this pin is selectable on a global basis.
yzz	Input/Output – These are the general purpose I/O used by the logic array. y reference (alpha) and z is the macrocell reference (numeric) y: A-X (768 macrocells) y: A-P (512 macrocells) y: A-H (256 macrocells) z: 0-31
GND	GND – Ground
NC	No connect
V_{CC}	V_{CC} – The power supply pins for core logic.
V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}	V_{CC} – The power supply pins for I/O banks 0, 1, 2, and 3.
V_{REF0}, V_{REF1}, V_{REF2}, V_{REF3}	Input – This pin defines the reference voltage for I/O banks 0, 1, 2, and 3.
GCLK0, GCLK1, GCLK2, GCLK3	Input – Global clock/clock enable inputs (see Figure 14 for differential pairi
CLK_OUT0, CLK_OUT1	Output – Optional clock output from PLL 0 and 1.
PLL_RST0, PLL_RST1	Input – Optional input resets the M divider in PLL 0 and 1.
PLL_FBK0, PLL_FBK1	Input – Optional feedback input for PLL 0 and 1.
GNDP	GND – Ground for PLLs.
V_{CCP}	V_{CC} – The power supply pin for PLLs.
V_{CCJ}	V_{CC} – The power supply for the IEEE 1149.1 interface.
DATA*x*	I/O – sysCONFIG data pins, bit *x*.
CSB	Input – sysCONFIG interface chip select. Drive low to select sysCONFIG i
CFG0	Input – Defines SRAM configuration mode. Low: sysCONFIG port, high: E^2 IEEE 1149.1 TAP.
PROGRAMB	Input – Controls the programming of SRAM. Hold high for normal operation to reload SRAM from E^2 memory.
CCLK[1]	Input – Clock for sysCONFIG interface. Reads and writes occur on the risi the clock.
READ[1]	Input – Drive high to perform reads from the sysCONFIG interface.
INITB	I/O – Indicates status of configuration. Can be driven low to inhibit configur
DONE	Output (open drain) – Indicates status of configuration.

1. These inputs should not toggle during power up for proper power-up configuration.

ispXPLD 5000MX Power Supply and NC Connections[1]

Signals	208 PQFP[4]	256 fpBGA[3, 5]	484 fpBGA, 5[3]	672 fpBGA[3, 5]
VCC	10, 49, 76, 114, 153, 180	D4, D13, F6, F11, L6, L11, N4, N13	A17, A6, AA2, AA21, AB17, AB6, B2, B21, D19, D4, F1, F22, G10, G11, G12, G13, K16, K7, L16, L7, M16, M7, T10, T11, T12, T13, T14, T9, U1, U22, W19, W4	AA21, AA6, F21, F6, G20, J14, K13, K14, L13, L14, N10, N11, N12, N15, N16 N9, P10, P11, P12, P15, P18, P9, R13, R14, T13, T U14, V13, V14, Y20, Y7
VCCO0	5, 17, 189, 204	A1, F7, G6	B9, C3, G8, G9, H7, J2, J7, P4	H10, H11, H8, H9, J8, J9, N8
VCCO1	42, 57, 72	K6, L7, T1	AA9, R7, T3, T8, Y3	P8, R8, T8, U8, V8, V9, W W8, W9
VCCO2	85, 100, 107, 121	K11, L10, T16	AA14, R16, T15, T20, Y20	P19, R19, T19, U19, V18, W13, W14, W15, W16, W W19
VCCO3	146, 161, 176	A16, F10, G11	B14, C20, G14, G15, H16, J16, J21, P19	H12, H13, H14, H15, H16 H19, J18, J19, K19, L19,
VCCP	136	J16	M22	N25
VCCJ	27	J1	M1	N4
GND	15, 29, 44, 81, 119, 148, 185, 7, 19, 191, 205, 40, 56, 70, 87, 101, 109, 123, 144, 160, 174	K1, C3, C14, E5, E12, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M5, M12, P3	N1, A1, A2, A21, A22, AA1, AA22, AB1, AB22, B1, B22, C15, C8, D11, D12, E18, E5, F17, F6, G16, G7, H10, H11, H12, H13, H14, H15, H20, H3, H8, H9, J10, J11, J12, J13, J14, J15, J8, J9, K10, K11, K12, K13, K14, K15, K8, K9, L10, L11, L12, L13, L14, L15, L19, L4, L8, L9, M10, M11, M12, M13, M14, M19, M4, M9, N10, N11, N12, N13, N14, N9, P10, P11, P12, P13, P14, P9, R10, R11, R12, R13, R14, R15, R8, R9, T16, T7, W11, W12, Y15, Y8	A11, A16, A2, A25, AE1, AE26, AF11, AF16, AF2, B2, B25, B26, J10, J11, J1 J17, K10, K11, K12, K15, K18, K9, L1, L10, L11, L1 L17, L18, L26, L9, M10, M M15, M16, M17, M18, M9 P13, P14, R10, R11, R12, R17, R18, R9, T1, T10, T1 T16, T17, T18, T26, T9, U U12, U15, U16, U17, U18 V11, V12, V15, V16, V17
GNDP	134	K16	N22	P26
NC[2]	—	**5256MX**: A2, A11, A12, A15, B2, B12, B15, B16, C4, C12, C15, C16, D1, D11, D14, D15, D16, E1, E4, E10, E11, E13, E14, F4, F5, F12, F13, L1, L4, M3, M7, M13, N2, N6, P1, P2, P5, P6, P13, P14, P15, P16, R1, R2, R4, R5, R6, R16, T2, T3, T4, T5, T6 **5512MX/5768MX**: L1	**5512MX**: P1, AA19, AB2, AB21, J17, J6, K1, K17, K18, K19, K2, K20, K21, K22, K3, K4, K5, K6, L1, L17, L18, L2, L20, L21, L22, L3, L5, L6, M15, M17, M18, M2, M20, M21, M3, M5, M6, M8, N15, N17, N18, N19, N2, N20, N21, N3, N4, N5, N6, N8, P15, P17, P18, P2, P21, P22, P5, P6, P8, U17, U6, V18, V5, W6 **5768MX/51024MX**: None	A12, A13, A14, A15, AA1 AA12, AA13, AA14, AA15 AA17, AA7, AB10, AB11, AB13, AB14, AB15, AB16 AC10, AC11, AC12, AC13 AC15, AC16, AC17, AD1 AD13, AD14, AD15, AD16 AE12, AE13, AE14, AE15 AF12, AF13, AF14, AF15, B13, B14, B15, B16, C11, C14, C15, C16, C3, D10, D13, D14, D15, D16, D17 E12, E13, E14, E15, E16, E7, E8, F10, F11, F12, F1 F16, F17, G10, G11, G12 G15, G16, G17, Y10, Y11, Y14, Y15, Y16, Y17

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOX} are connected within the substrate to their respective common signals. Pin orientation A1 sta upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally
4. Pin orientation follows the conventional counter-clockwise order from pin 1 marking of the topside view.
5. Internal GNDs and I/O GNDs (Bank 0 - Bank 3) are connected inside package. V_{CCO} balls connect to four power planes with age, one each for V_{CCOX}.

ispXPLD 5256MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	25 Ba
			Macrocell 1	Macrocell 2		
0	61N	H30	G17	H17	H31	
0	61P	H28	G16	H16	H29	
0	62N	H26	G15	H15	H27	
0	62P	H24	G14	H14	H25	
0	63N	H22	G13	H13	H23	
0	63P	H21	G12	H12	-	
-	-	VCC	-	-	-	
0	64N	H20	G11	H11	-	
0	64P	H18/CLK_OUT0	G10	H10	H19	
0	65N	H16	G9	H9	H17	
0	65P	H14	G8	H8	H15	
-	-	GND	-	-	-	
0	66N	H12	G7	H7	H13	
-	-	VCCO0	-	-	-	
0	66P	H10	G6	H6	H11	
-	-	GND (Bank 0)	-	-	-	GN
0	67N	H8	G5	H5	H9	
0	67P	H6/PLL_RST0	G4	H4	H7	
0	68N	H5	-	-	-	
0	68P	H4/PLL_FBK0	-	-	-	
0	69N	H2	-	-	H3	
0	69P	H0	-	-	H1	
-	GCLK0P	GCLK0	-	-	-	
-	-	VCCJ	-	-	-	See F NC C
-	GCLK0N	GCLK1	-	-	-	
-	-	GND	-	-	-	
-	-	TDI	-	-	-	
-	-	TMS	-	-	-	
-	-	TCK	-	-	-	
-	-	TDO	-	-	-	
1	0P	A0/DATA0	A0	B0	A1	
1	0N	A2/DATA1	A1	B1	A3	
1	1P	A4/DATA2	A2	B2	-	
1	1N	A5/DATA3	A3	B3	-	
1	2P	A6/DATA4	A4	B4	A7	
1	2N	A8/DATA5	A5	B5	A9	
-	-	GND (Bank 1)	-	-	-	GN
1	3P	A10/DATA6	A6	B6	A11	
-	-	VCCO1	-	-	-	
1	3N	A12/DATA7	A7	B7	A13	
-	-	GND	-	-	-	
1	4P	A14/INITB	A8	B8	A15	

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	25 Ba
			Macrocell 1	Macrocell 2		
1	4N	A16/CSB	A9	B9	A17	
1	5P	A18/READ	A10	B10	A19	
1	5N	A20/CCLK	A11	B11	A21	
-	-	VCC	-	-	-	
-	-	DONE	-	-	-	
1	6P	A22	A12	B12	A23	
1	6N	A24	A13	B13	A25	
1	7P	A26	A14	B14	A27	
1	7N	A28	A15	B15	A29	
-	-	PROGRAMB	-	-	-	
-	-	GND (Bank 1)	-	-	-	GN
-	-	VCCO1	-	-	-	
-	-	CFG0	-	-	-	
1	8P	B2	A16	B16	B3	
1	8N	B4	A17	B17	-	
1	9P	B5	A18	B18	-	
1	9N	B6	A19	B19	B7	
1	10P	B8	A20	B20	B9	
1	10N	B10	A21	B21	B11	
1	11P	B12	A22	B22	B13	
1	11N	B14	A23	B23	B15	
1	-	B16/VREF1	-	-	B17	
1	12P	B18	A24	B24	B19	
1	12N	B20	A25	B25	-	
-	-	GND (Bank 1)	-	-	-	GN
1	13P	B21	A26	B26	-	
-	-	VCCO1	-	-	-	
1	13N	B22	A27	B27	B23	
1	14P	B24	A28	B28	B25	
1	14N	B26	A29	B29	B27	
-	-	VCC	-	-	-	
1	15P	B28	A30	B30	B29	
1	15N	B30	A31	B31	B31	
2	16P	C0	C0	D0	C1	
2	16N	C2	C1	D1	C3	
2	17P	C4	C2	D2	-	
2	17N	C5	C3	D3	-	
2	18P	C6	C4	D4	C7	
-	-	VCCO2	-	-	-	
2	18N	C8	C5	D5	C9	
-	-	GND (Bank 2)	-	-	-	GN
2	19P	C10	C6	D6	C11	
2	19N	C12	C7	D7	C13	

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	25 Ba
			Macrocell 1	Macrocell 2		
2	20P	C14	-	-	C15	
2	20N	C16/VREF2	-	-	C17	
2	21P	C18	C8	D8	C19	
2	21N	C20	C9	D9	-	
2	22P	C21	C10	D10	-	
2	22N	C22	C11	D11	C23	
2	23P	C24	C12	D12	C25	
2	23N	C26	C13	D13	C27	
2	24P	C28	C14	D14	C29	
2	24N	C30	C15	D15	C31	
-	-	VCCO2	-	-	-	
-	-	GND (Bank 2)	-	-	-	GN
2	25P	D0	-	-	D1	
2	25N	D2	-	-	D3	
2	26P	D4	C16	D16	-	
2	26N	D5	C17	D17	-	
2	27P	D6	C18	D18	D7	
2	27N	D8	C19	D19	D9	
-	-	VCC	-	-	-	
2	28P	D10	C20	D20	D11	
2	28N	D12	C21	D21	D13	
2	29P	D14	C22	D22	D15	
2	29N	D16	C23	D23	D17	
-	-	GND	-	-	-	
2	30P	D18	C24	D24	D19	
-	-	VCCO2	-	-	-	
2	30N	D20	C25	D25	-	
-	-	GND (Bank 2)	-	-	-	GN
2	31P	D21	C26	D26	-	
2	31N	D22	C27	D27	D23	
2	32P	D24	C28	D28	D25	
2	32N	D26	C29	D29	D27	
2	33P	D28	C30	D30	D29	
2	33N	D30	C31	D31	D31	
-	-	TOE	-	-	-	
-	-	RESET	-	-	-	
-	-	GOE0	-	-	-	
-	-	GOE1	-	-	-	
-	-	GNDP	-	-	-	See F NC C
-	GCLK3N	GCLK2	-	-	-	
-	-	VCCP	-	-	-	See F NC C
-	GCLK3P	GCLK3	-	-	-	

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	25 Ba
			Macrocell 1	Macrocell 2		
3	34N	E30	-	-	E31	
3	34P	E28	-	-	E29	
3	35N	E26	-	-	E27	
3	35P	E24/PLL_FBK1	-	-	E25	
3	36N	E22/PLL_RST1	E27	F27	E23	
3	36P	E21	E26	F26	-	
-	-	GND (Bank 3)	-	-	-	GN
3	37N	E20	E25	F25	-	
-	-	VCCO3	-	-	-	
3	37P	E18	E24	F24	E19	
-	-	GND	-	-	-	
3	38N	E16	E23	F23	E17	
3	38P	E14	E22	F22	E15	
3	39N	E12	E21	F21	E13	
3	39P	E10/CLK_OUT1	E20	F20	E11	
-	-	VCC	-	-	-	
3	40N	E8	E19	F19	E9	
3	40P	E6	E18	F18	E7	
3	41N	E5	E17	F17	-	
3	41P	E4	E16	F16	-	
3	42N	E2	E31	F31	E3	
3	42P	E0	E30	F30	E1	
-	-	GND (Bank 3)	-	-	-	GN
-	-	VCCO3	-	-	-	
3	43N	F30	E15	F15	F31	
3	43P	F28	E14	F14	F29	
3	44N	F26	E13	F13	F27	
3	44P	F24	E12	F12	F25	
3	45N	F22	E11	F11	F23	
3	45P	F21	E10	F10	-	
3	46N	F20	E9	F9	-	
3	46P	F18	E8	F8	F19	
3	47N	F16/VREF3	E29	F29	F17	
3	47P	F14	E28	F28	F15	
3	48N	F12	E7	F7	F13	
3	48P	F10	E6	F6	F11	
-	-	GND (Bank 3)	-	-	-	GN
3	49N	F8	E5	F5	F9	
-	-	VCCO3	-	-	-	
3	49P	F6	E4	F4	F7	
3	50N	F5	E3	F3	-	
3	50P	F4	E2	F2	-	
-	-	VCC	-	-	-	

ispXPLD 5256MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	25 Ba
			Macrocell 1	Macrocell 2		
3	51N	F2	E1	F1	F3	
3	51P	F0	E0	F0	F1	
0	52N	G30	G31	H31	G31	
0	52P	G28	G30	H30	G29	
-	-	GND	-	-	-	
0	53N	G26	G29	H29	G27	
0	53P	G24	G28	H28	G25	
0	54N	G22	G27	H27	G23	
-	-	VCCO0	-	-	-	
0	54P	G21	G26	H26	-	
-	-	GND (Bank 0)	-	-	-	GN
0	55N	G20	G25	H25	-	
0	55P	G18	G24	H24	G19	
0	56N	G16/VREF0	G3	H3	G17	
0	56P	G14	G2	H2	G15	
0	57N	G12	G23	H23	G13	
0	57P	G10	G22	H22	G11	
0	58N	G8	G21	H21	G9	
0	58P	G6	G20	H20	G7	
0	59N	G5	G19	H19	-	
0	59P	G4	G18	H18	-	
0	60N	G2	G1	H1	G3	
0	60P	G0	G0	H0	G1	
-	-	VCCO0	-	-	-	
-	-	GND (Bank 0)	-	-	-	GN

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs

ispXPLD 5512MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
0	109N	O30	O11	P18	O31	208	C4	
0	109P	O28	O10	P16	O29	1	E4	
0	110N	O26	M17	O17	O27	2	B1	
0	110P	O24	M16	O16	O25	3	C1	
0	111N	O22	M15	O15	O23	4	D3	
—	—	V_{CCO0}	—	—	—	5	V_{CCO0}	
0	111P	O20	M14	O14	O21	6	C2	
—	—	GND (Bank 0)	—	—	—	7	GND (Bank 0)	G
0	112N	O18	M13	O13	O19	8	E3	
0	112P	O16	M12	O12	O17	9	D2	
0	113N	O14	O9	P14	O15	—	—	
0	113P	O12	O8	P12	O13	—	—	
0	114N	O10	O7	P10	O11	—	—	
0	114P	O8	O6	P8	O9	—	—	
0	115N	O6	O5	P6	O7	—	—	
0	115P	O4	O4	P4	O5	—	—	
0	116N	O2	O3	P2	O3	—	—	
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	
0	116P	O0	O2	P0	O1	—	—	
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	G
0	117N	P30	O1	—	P31	—	D1	
0	117P	P28	O0	—	P29	—	E1	
0	118N	P26	O31	—	P27	—	F4	
—	—	V_{CC}	—	—	—	10	V_{CC}	
0	118P	P24	O30	—	P25	—	F5	
0	119N	P22	M11	O11	P23	11	E2	
0	119P	P20/CLK_OUT0	M10	O10	P21	12	F2	
0	120N	P18	M9	O9	P19	13	F1	
0	120P	P16	M8	O8	P17	14	G1	
—	—	GND	—	—	—	15	GND	
0	121N	P14	M7	O7	P15	16	F3	
—	—	V_{CCO0}	—	—	—	17	V_{CCO0}	
0	121P	P12	M6	O6	P13	18	G5	
—	—	GND (Bank 0)	—	—	—	19	GND (Bank 0)	G
0	122N	P10	M5	O5	P11	20	H5	
0	122P	P8/PLL_RST0	M4	O4	P9	21	G4	
0	123N	P6	—	—	P7	22	G3	
0	123P	P4/PLL_FBK0	—	—	P5	23	H3	
0	124N	P2	—	—	P3	24	G2	
0	124P	P0	—	—	P1	25	H1	
—	GCLK0P	GCLK0	—	—	—	26	H2	
—	—	V_{CCJ}	—	—	—	See Power Supply a NC Connections Tab		

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
—	GCLK0N	GCLK1	—	—	—	28	J2	
—	—	GND	—	—	—	29	GND	
—	—	TDI	—	—	—	30	H6	
—	—	TMS	—	—	—	31	H4	
—	—	TCK	—	—	—	32	J6	
—	—	TDO	—	—	—	33	K2	
1	0P	A0/DATA0	B0	D0	A1	34	K3	
1	0N	A2/DATA1	B1	D1	A3	35	J3	
1	1P	A4/DATA2	B2	D2	A5	36	J5	
1	1N	A6/DATA3	B3	D3	A7	37	J4	
1	2P	A8/DATA4	B4	D4	A9	38	L2	
1	2N	A10/DATA5	B5	D5	A11	39	M1	
—	—	GND (Bank 1)	—	—	—	40	GND (Bank 1)	G
1	3P	A12/DATA6	B6	D6	A13	41	K4	
—	—	V_{CCO1}	—	—	—	42	V_{CCO1}	
1	3N	A14/DATA7	B7	D7	A15	43	L3	
—	—	GND	—	—	—	44	GND	
1	4P	A16/INITB	B8	D8	A17	45	K5	
1	4N	A18/CSB	B9	D9	A19	46	L5	
1	5P	A20/READ	B10	D10	A21	47	N1	
1	5N	A22/CCLK	B11	D11	A23	48	M2	
1	6P	A24	—	—	A25	—	—	
—	—	VCC	—	—	—	49	VCC	
1	6N	A26	—	—	A27	—	P1[1]	
1	7P	A28	—	—	A29	—	M3	
1	7N	A30	—	—	A31	—	L4	
1	8P	B0	A0	—	B1	—	N2	
1	8N	B2	A2	—	B3	—	P2	
—	—	GND (Bank 1)	—	—	—	—	GND (Bank 1)	G
1	9P	B4	A4	—	—	—	R1	
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	
1	9N	B5	A6	—	—	—	R2	
1	10P	B6	A8	—	B7	—	T2	
1	10N	B8	A10	—	B9	—	T3	
1	—	B10	A12	—	B11	—	—	
—	—	DONE	—	—	—	50	M4	
1	11P	B14	B12	D12	B15	51	N3	
1	11N	B16	B13	D13	B17	52	P4	
1	12P	B18	B14	D14	B19	53	N5	
1	12N	B20	B15	D15	B21	54	M6	
—	—	PROGRAMB	—	—	—	55	R3	
1	—	B22	A14	—	B23	—	P5	
—	—	GND (Bank 1)	—	—	—	56	GND (Bank 1)	G

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
1	13P	B24	A16	—	B25	—	T4	
—	—	V_{CCO1}	—	—	—	57	V_{CCO1}	
1	13N	B26	A18	—	B27	—	T5	
1	14P	B28	A20	—	B29	—	R4	
1	14N	B30	A22	—	B31	—	N6	
1	15P	C0	—	—	C1	—	R5	
1	15N	C2	—	—	C3	—	P6	
1	16P	C4	—	—	C5	—	—	
1	16N	C8	—	—	C9	—	—	
1	17P	C10	—	—	C11	—	—	
1	17N	C12	—	—	C13	—	M7[1]	
1	18P	C16	—	—	C17	—	T6	
1	18N	C18	—	—	C19	—	R6	
—	—	GND0 (Bank 1)	—	—	—	—	GND (Bank 1)	G
—	—	CFG0	—	—	—	58	L8	
—	—	V_{CCO1}	—	—	—	—	V_{CCO1}	
1	19P	C24	B16	D16	C25	59	T7	
1	19N	C26	B17	D17	C27	60	R7	
1	20P	C28	B18	D18	C29	61	N7	
1	20N	D0	B19	D19	D1	62	P7	
1	21P	D2	B20	D20	D3	63	T8	
1	21N	D4	B21	D21	D5	64	R8	
1	22P	D6	B22	D22	D7	65	M8	
1	22N	D8	B23	D23	D9	66	P8	
1	—	D10/V_{REF1}	—	—	D11	67	L9	
1	23P	D12	B24	D24	D13	68	N8	
1	23N	D16	B25	D25	D17	69	M9	
—	—	GND (Bank 1)	—	—	—	70	GND (Bank 1)	G
1	24P	D18	B26	D26	D19	71	N10	
—	—	VCCO1	—	—	—	72	V_{CCO1}	
1	24N	D20	B27	D27	D21	73	T9	
1	25P	D22	B28	D28	D23	74	T10	
1	25N	D24	B29	D29	D25	75	R9	
—	—	VCC	—	—	—	76	VCC	
1	26P	D26	B30	D30	D27	77	P9	
1	26N	D28	B31	D31	D29	78	N9	
2	27P	E0	F0	H0	E1	79	T11	
2	27N	E2	F1	H1	E3	80	T12	
—	—	GND	—	—	—	81	NC	
—	—	GND	—	—	—	—	GND	
2	28P	E4	F2	H2	E5	82	P10	
2	28N	E6	F3	H3	E7	83	R10	
2	29P	E8	F4	H4	E9	84	R11	

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
—	—	V_{CCO2}	—	—	—	85	V_{CCO2}	
2	29N	E10	F5	H5	E11	86	M10	
—	—	GND (Bank 2)	—	—	—	87	GND (Bank 2)	G
2	30P	E12	F6	H6	E13	88	M11	
2	30N	E16	F7	H7	E17	89	T13	
2	31P	E18	—	—	E19	90	P11	
2	31N	E20/V_{REF2}	—	—	E21	91	T14	
2	32P	E22	F8	H8	E23	92	R12	
2	32N	E24	F9	H9	E25	93	R13	
2	33P	E26	F10	H10	E27	94	N11	
2	33N	E28	F11	H11	E29	95	T15	
2	34P	F0	F12	H12	F1	96	R14	
2	34N	F2	F13	H13	F3	97	N12	
2	35P	F4	F14	H14	F5	98	P12	
—	—	V_{CCO2}	—	—	—	—	V_{CCO2}	
2	35N	F6	F15	H15	F7	99	R15	
—	—	GND (Bank 2)	—	—	—	—	GND (Bank 2)	G
2	36P	F8	E0	—	F9	—	—	
2	36N	F10	E2	—	F11	—	—	
2	37P	F12	E4	—	F13	—	—	
2	37N	F16	E6	—	F17	—	—	
2	38P	F18	E8	—	F19	—	—	
2	38N	F20	E10	—	F21	—	—	
2	39P	F22	E12	—	F23	—	—	
2	39N	F24	E16	—	F25	—	—	
2	40P	F26	E20	—	F27	—	—	
2	40N	F28	E22	—	F29	—	—	
2	41P	G0	—	—	G1	—	—	
—	—	V_{CCO2}	—	—	—	100	V_{CCO2}	
2	41N	G2	—	—	G3	—	—	
—	—	GND (Bank 2)	—	—	—	101	GND (Bank 2)	G
2	42P	G4	—	—	G5	102	P13	
2	42N	G6	—	—	G7	103	P15	
2	43P	G8	—	—	G9	—	M13	
2	43N	G10	—	—	G11	—	P14	
2	44P	G12	—	—	G13	—	—	
2	44N	G14	—	—	G15	—	—	
2	45P	G16	—	—	G17	—	—	
2	45N	G18	—	—	G19	—	—	
2	46P	G20	—	—	G21	104	R16	
2	46N	G22	—	—	G23	105	P16	
2	47P	G24	—	—	G25	106	N15	
—	—	V_{CCO2}	—	—	—	107	V_{CCO2}	

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
2	47N	G26	—	—	G27	108	N14	
—	—	GND (Bank 2)	—	—	—	109	GND (Bank 2)	G
2	48P	G28	F16	H16	G29	110	N16	
2	48N	G30	F17	H17	G31	111	M16	
2	49P	H0	F18	H18	H1	112	M14	
2	49N	H2	F19	H19	H3	113	M15	
2	50P	H4	E24	—	H5	—	—	
—	—	V_{CC}	—	—	—	114	VCC	
2	50N	H6	E26	—	H7	—	NC	
2	51P	H8	F20	H20	H9	115	L13	
2	51N	H10	F21	H21	H11	116	L12	
2	52P	H12	F22	H22	H13	117	L15	
2	52N	H14	F23	H23	H15	118	L16	
—	—	GND	—	—	—	119	GND	
2	53P	H16	F24	H24	H17	120	L14	
—	—	V_{CCO2}	—	—	—	121	V_{CCO2}	
2	53N	H18	F25	H25	H19	122	K15	
—	—	GND (Bank 2)	—	—	—	123	GND (Bank 2)	G
2	54P	H20	F26	H26	H21	124	K14	
2	54N	H22	F27	H27	H23	125	K12	
2	55P	H24	F28	H28	H25	126	K13	
2	55N	H26	F29	H29	H27	127	J13	
2	56P	H28	F30	H30	H29	128	J14	
2	56N	H30	F31	H31	H31	129	J12	
—	—	TOE	—	—	—	130	J15	
—	—	RESET	—	—	—	131	J11	
—	—	GOE0	—	—	—	132	H11	
—	—	GOE1	—	—	—	133	H13	
—	—	GNDP	—	—	—	See Power Supply and NC Conne		
—	GCLK3N	GCLK2	—	—	—	135	H15	
—	—	V_{CCP}	—	—	—	See Power Supply and NC Conne		
—	GCLK3P	GCLK3	—	—	—	137	H16	
3	57N	I30	—	—	I31	138	H14	
3	57P	I28	—	—	I29	139	G16	
3	58N	I26	—	—	I27	140	G15	
3	58P	I24/PLL_FBK1	—	—	I25	141	F15	
3	59N	I22/PLL_RST1	I27	K27	I23	142	H12	
3	59P	I20	I26	K26	I21	143	G14	
—	—	GND (Bank 3)	—	—	—	144	GND (Bank 3)	G
3	60N	I18	I25	K25	I19	145	F16	
—	—	VCCO3	—	—	—	146	V_{CCO3}	
3	60P	I16	I24	K24	I17	147	E16	
—	—	GND	—	—	—	148	GND	

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
3	61N	I14	I23	K23	I15	149	G13	
3	61P	I12	I22	K22	I13	150	G12	
3	62N	I10	I21	K21	I11	151	F14	
3	62P	I8/CLK_OUT1	I20	K20	I9	152	E15	
3	63N	I6	K31	—	I7	—	F12	
—	—	V_{CC}	—	—	—	153	VCC	
3	63P	I4	K30	L30	I5	—	F13	
3	64N	I2	K29	L28	I3	—	D16	
3	64P	I0	K28	L26	I1	—	D15	
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	G
3	65N	J30	K27	—	J31	—	—	
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	
3	65P	J28	K26	—	J29	—	—	
3	66N	J26	K25	—	J27	—	—	
3	66P	J24	K24	—	J25	—	—	
3	67N	J22	K23	—	J23	—	—	
3	67P	J20	K22	—	J21	—	—	
3	68N	J18	K21	—	J19	—	—	
3	68P	J16	K20	—	J17	—	—	
3	69N	J14	K19	—	J15	—	C16	
3	69P	J12	K18	—	J13	—	B16	
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	G
3	70N	J10	K17	—	J11	—	C15	
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	
3	70P	J8	K16	—	J9	—	B15	
3	71N	J6	K15	—	J7	—	E14	
3	71P	J4	K14	—	J5	—	D14	
3	72N	J2	K13	—	J3	—	E13	
3	72P	J0	K12	—	J1	—	A15	
3	73N	K30	I19	K19	K31	154	D12	
3	73P	K28	I18	K18	K29	155	B14	
3	74N	K26	I17	K17	K27	156	C13	
3	74P	K24	I16	K16	K25	157	A14	
3	75N	K22	I31	K31	K23	158	A13	
3	75P	K21	I30	K30	—	159	B13	
—	—	GND (Bank 3)	—	—	—	160	GND (Bank 3)	G
3	76N	K20	K11	L21	—	—	D11	
—	—	V_{CCO3}	—	—	—	161	V_{CCO3}	
3	76P	K18	K10	L20	K19	—	B12	
3	77N	K16	K9	L18	K17	—	C12	
3	77P	K14	K8	L16	K15	—	E11	
3	78N	K12	K7	L12	K13	—	—	
3	78P	K10	K6	L10	K11	—	—	

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
3	79N	K8	K5	L8	K9	—	—	
3	79P	K6	K4	L6	K7	—	—	
3	80N	K5	K3	L5	—	—	—	
3	80P	K4	K2	L4	—	—	E10[1]	
3	81N	K2	K1	L2	K3	—	A12	
3	81P	K0	K0	L0	K1	—	A11	
—	—	GND (Bank 3)	—	—	—	—	GND (Bank 3)	G
3	82N	L30	I15	K15	L31	162	B11	
—	—	V_{CCO3}	—	—	—	—	V_{CCO3}	
3	82P	L28	I14	K14	L29	163	C11	
3	83N	L26	I13	K13	L27	164	B10	
3	83P	L24	I12	K12	L25	165	A10	
3	84N	L22	I11	K11	L23	166	C10	
3	84P	L21	I10	K10	—	167	D10	
3	85N	L20	I9	K9	—	168	C9	
3	85P	L18	I8	K8	L19	169	E9	
3	86N	L16/VREF3	I29	K29	L17	170	D9	
3	86P	L14	I28	K28	L15	171	F9	
3	87N	L12	I7	K7	L13	172	A9	
3	87P	L10	I6	K6	L11	173	F8	
—	—	GND (Bank 3)	—	—	—	174	GND (Bank 3)	G
3	88N	L8	I5	K5	L9	175	E8	
—	—	V_{CCO3}	—	—	—	176	V_{CCO3}	
3	88P	L6	I4	K4	L7	177	A8	
3	89N	L5	I3	K3	—	178	B9	
3	89P	L4	I2	K2	—	179	D8	
—	—	VCC	—	—	—	180	VCC	
3	90N	L2	I1	K1	L3	181	B8	
3	90P	L0	I0	K0	L1	182	C8	
0	91N	M30	M31	O31	M31	183	B7	
0	91P	M28	M30	O30	M29	184	A7	
—	—	GND	—	—	—	185	—	
—	—	GND	—	—	—	—	GND	
0	92N	M26	M29	O29	M27	186	D7	
0	92P	M24	M28	O28	M25	187	C7	
0	93N	M22	M27	O27	M23	188	B6	
—	—	V_{CCO0}	—	—	—	189	V_{CCO0}	
0	93P	M21	M26	O26	M22	190	E7	
—	—	GND (Bank 0)	—	—	—	191	GND (Bank 0)	G
0	94N	M20	M25	O25	M21	192	E6	
0	94P	M18	M24	O24	M19	193	A6	
0	95N	M16/V_{REF0}	M3	O3	M17	194	A5	
0	95P	M14	M2	O2	M15	195	A4	

ispXPLD 5512MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Input	208 PQFP Pin Number	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2				
0	96N	M12	M23	O23	M13	196	B5	
0	96P	M10	M22	O22	M11	197	A3	
0	97N	M8	M21	O21	M9	198	B4	
0	97P	M6	M20	O20	M7	199	B3	
0	98N	M5	M19	O19	—	200	C5	
0	98P	M4	M18	O18	—	201	C6	
0	99N	M2	M1	O1	M3	202	D5	
—	—	V_{CCO0}	—	—	—	—	V_{CCO0}	
0	99P	M0	M0	O0	M1	203	D6	
—	—	GND (Bank 0)	—	—	—	—	GND (Bank 0)	G
0	100N	N30	O29	—	N31	—	—	
0	100P	N28	O28	—	N29	—	—	
0	101N	N26	O27	—	N27	—	—	
0	101P	N24	O26	—	N25	—	—	
0	102N	N22	O25	—	N23	—	—	
0	102P	N21	O24	—	—	—	—	
0	103N	N20	O23	—	—	—	—	
0	103P	N18	O22	—	N19	—	—	
0	104N	N16	O21	—	N17	—	—	
0	104P	N14	O20	—	N15	—	—	
0	105N	N12	O19	—	N13	—	—	
—	—	V_{CCO0}	—	—	—	204	V_{CCO0}	
0	105P	N10	O18	—	N11	—	—	
—	—	GND (Bank 0)	—	—	—	205	GND (Bank 0)	G
0	106N	N8	O17	—	N9	—	—	
0	106P	N6	O16	—	N7	—	—	
0	107N	N5	O15	—	—	206	A2	
0	107P	N4	O14	—	—	207	B2	
0	108N	N2	O13	—	N3	—	—	
0	108P	N0	O12	—	N1	—	—	

1. Not available for differential pair.

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired
receive differential clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 5768MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
0	127N	S22	S11	T18	S23	C4	
0	127P	S20	S10	T16	S21	E4	
0	128N	S18	Q17	S17	S19	B1	
0	128P	S16	Q16	S16	S17	C1	
0	129N	S14	Q15	S15	S15	D3	
-	-	VCCO0	-	-	-	VCCO0	
0	129P	S12	Q14	S14	S13	C2	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	130N	S10	Q13	S13	S11	E3	
0	130P	S8	Q12	S12	S9	D2	
0	131N	S6	S9	T14	S7	—	
0	131P	S4	S8	T12	S5	—	
0	132N	S2	S7	T10	S3	—	
-	-	VCC	-	-	-	VCC	
0	132P	S0	S6	T8	S1	—	
-	-	GND	-	-	-	GND	
0	133N	T30	S5	T6	T31	—	
0	133P	T28	S4	T4	T29	—	
0	134N	T26	S3	T2	T27	—	
-	-	VCCO0	-	-	-	VCCO0	
0	134P	T24	S2	T0	T25	—	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	135N	T22	S1	-	T23	D1	
0	135P	T20	S0	-	T21	E1	
0	136N	T18	S31	-	T19	F4	
-	-	VCC	-	-	-	VCC	
0	136P	T16	S30	-	T17	F5	
0	137N	T14	Q11	S11	T15	E2	
0	137P	T12/CLK_OUT0	Q10	S10	T13	F2	
0	138N	T10	Q9	S9	T11	F1	
0	138P	T8	Q8	S8	T9	G1	
-	-	GND	-	-	-	GND	
0	139N	T6	Q7	S7	T7	F3	
-	-	VCCO0	-	-	-	VCCO0	
0	139P	T4	Q6	S6	T5	G5	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	140N	T2	Q5	S5	T3	H5	
0	140P	T0/PLL_RST0	Q4	S4	T1	G4	
0	141N	U30	U31	W31	U31	G3	
0	141P	U28/PLL_FBK0	U30	W30	U29	H3	
0	142N	U26	U29	W29	U27	—	
0	142P	U24	U28	W28	U25	—	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
0	143N	U22	U27	W27	U23	—	
-	-	VCCO0	-	-	-	VCCO0	
0	143P	U20	U26	W26	U21	—	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	144N	U18	U25	W25	U19	—	
0	144P	U16	U24	W24	U17	—	
0	145N	U14	U23	W23	U15	—	
0	145P	U12	U22	W22	U13	—	
0	146N	U10	U21	W21	U11	—	
0	146P	U8	U20	W20	U9	—	
0	147N	U6	U19	W19	U7	—	
0	147P	U4	U18	W18	U5	—	
0	148N	U2	U17	W17	U3	—	
-	-	VCCO0	-	-	-	VCCO0	
0	148P	U0	U16	W16	U1	—	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	149N	W30	U15	W15	W31	—	
0	149P	W28	U14	W14	W29	—	
0	150N	W26	U13	W13	W27	—	
-	-	VCC	-	-	-	VCC	
0	150P	W24	U12	W12	W25	—	
0	151N	W22	U11	W11	W23	—	
0	151P	W20	U10	W10	W21	—	
0	152N	W18	U9	W9	W19	—	
0	152P	W16	U8	W8	W17	—	
-	-	GND	-	-	-	GND	
0	153N	W14	U7	W7	W15	—	
-	-	VCCO0	-	-	-	VCCO0	
0	153P	W12	U6	W6	W13	—	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	154N	W10	U5	W5	W11	—	
0	154P	W8	U4	W4	-	—	
0	155N	W6	U3	W3	W7	—	
0	155P	W4	U2	W2	W5	—	
0	156N	W2	U1	W1	W3	G2	
0	156P	W0	U0	W0	W1	H1	
-	GCLK0P	GCLK0	-	-	-	H2	
-	-	VCCJ	-	-	-	See Power Su NC Connectio	
-	GCLK0N	GCLK1	-	-	-	J2	
-	-	GND	-	-	-	GND	
-	-	TDI	-	-	-	H6	
-	-	TMS	-	-	-	H4	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	J6	
-	-	TDO	-	-	-	K2	
1	0P	A30/DATA0	C0	A0	A31	K3	
1	0N	A28/DATA1	C1	A1	A29	J3	
1	1P	A26/DATA2	C2	A2	A27	J5	
1	1N	A24/DATA3	C3	A3	A25	J4	
1	2P	A22/DATA4	C4	A4	A23	L2	
1	2N	A20/DATA5	C5	A5	A21	M1	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	3P	A18/DATA6	C6	A6	A19	K4	
-	-	VCCO1	-	-	-	VCCO1	
1	3N	A16/DATA7	C7	A7	A17	L3	
-	-	GND	-	-	-	GND	
1	4P	A14/INITB	C8	A8	A15	K5	
1	4N	A12/CSB	C9	A9	A13	L5	
1	5P	A10/READ	C10	A10	A11	N1	
1	5N	A8/CCLK	C11	A11	A9	M2	
1	6P	A6	-	-	A7	—	
-	-	VCC	-	-	-	VCC	
1	6N	A4	-	-	A5	P1	
1	7P	A2	-	-	A3	M3	
1	7N	A0	-	-	A1	L4	
1	8P	B30	D0	-	B31	N2	
1	8N	B28	D2	-	B29	P2	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	9P	B26	D4	-	B27	R1	
-	-	VCCO1	-	-	-	VCCO1	
1	9N	B24	D6	-	B25	R2	
1	10P	B22	D8	-	B23	T2	
1	10N	B20	D10	-	B21	T3	
1	-	B18	D12	-	B19	—	
-	-	DONE	-	-	-	M4	
1	11P	B14	-	-	B15	—	
1	11N	B12	-	-	B13	—	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	12P	B10	-	-	B11	—	
-	-	VCCO1	-	-	-	VCCO1	
1	12N	B8	-	-	B9	—	
1	13P	B6	C12	A12	B7	N3	
1	13N	B4	C13	A13	B5	P4	
1	14P	B2	C14	A14	B3	N5	
1	14N	B0	C15	A15	B1	M6	
-	-	PROGRAMB	-	-	-	R3	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
1	-	C28	D14	-	C29	P5	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	15P	C26	D16	-	C27	T4	
-	-	VCCO1	-	-	-	VCCO1	
1	15N	C24	D18	-	C25	T5	
-	-	GND	-	-	-	GND	
1	16P	C22	D20	-	C23	R4	
-	-	VCC	-	-	-	VCC	
1	16N	C20	D22	-	C21	N6	
1	17P	C18	-	-	C19	R5	
1	17N	C16	-	-	C17	P6	
1	18P	C14	-	-	C15	—	
1	18N	C12	-	-	C13	—	
1	19P	C10	-	-	C11	—	
1	19N	C8	-	-	C9	M7	
1	20P	C6	-	-	C7	T6	
1	20N	C4	-	-	C5	R6	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
-	-	CFG0	-	-	-	L8	
-	-	VCCO1	-	-	-	VCCO1	
1	21P	C0	C16	A16	C1	T7	
1	21N	D30	C17	A17	D31	R7	
1	22P	D28	C18	A18	D29	N7	
1	22N	D26	C19	A19	D27	P7	
1	23P	D24	C20	A20	D25	T8	
1	23N	D22	C21	A21	D23	R8	
1	24P	D20	C22	A22	D21	M8	
1	24N	D18	C23	A23	D19	P8	
1	-	D16/VREF1	-	-	D17	L9	
1	25P	D14	C24	A24	D15	N8	
1	25N	D12	C25	A25	D13	M9	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	26P	D10	C26	A26	D11	N10	
-	-	VCCO1	-	-	-	VCCO1	
1	26N	D8	C27	A27	D9	T9	
1	27P	D6	C28	A28	D7	T10	
-	-	GND	-	-	-	GND	
1	27N	D4	C29	A29	D5	R9	
-	-	VCC	-	-	-	VCC	
1	28P	D2	C30	A30	D3	P9	
1	28N	D0	C31	A31	D1	N9	
2	29P	E0	F0	H0	E1	T11	
-	-	VCC	-	-	-	VCC	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
2	29N	E2	F1	H1	E3	T12	
-	-	GND	-	-	-	GND	
2	30P	E4	F2	H2	E5	P10	
2	30N	E6	F3	H3	E7	R10	
2	31P	E8	F4	H4	E9	R11	
-	-	VCCO2	-	-	-	VCCO2	
2	31N	E10	F5	H5	E11	M10	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	32P	E12	F6	H6	E13	M11	
2	32N	E14	F7	H7	E15	T13	
2	33P	E16	H0	-	E17	P11	
2	33N	E18/VREF2	H1	-	E19	T14	
2	34P	E20	F8	H8	E21	R12	
2	34N	E22	F9	H9	E23	R13	
2	35P	E24	F10	H10	E25	N11	
2	35N	E26	F11	H11	E27	T15	
2	36P	E28	F12	H12	E29	R14	
2	36N	E30	F13	H13	E31	N12	
2	37P	F0	F14	H14	F1	P12	
-	-	VCCO2	-	-	-	VCCO2	
2	37N	F2	F15	H15	F3	R15	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	38P	F4	H2	E0	F5	—	
2	38N	F6	H3	E2	F7	—	
2	39P	F8	H4	E4	F9	—	
2	39N	F10	H5	E6	F11	—	
2	40P	F12	H6	E8	F13	—	
2	40N	F14	H7	E10	F15	—	
2	41P	F16	H8	E12	F17	—	
2	41N	F18	H9	E16	F19	—	
2	42P	F20	H10	E20	F21	—	
-	-	VCC	-	-	-	VCC	
2	42N	F22	H11	E22	F23	—	
-	-	GND	-	-	-	GND	
2	43P	F24	H12	-	F25	—	
-	-	VCCO2	-	-	-	VCCO2	
2	43N	F26	H13	-	F27	—	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	44P	F28	H14	-	F29	P13	
2	44N	F30	H15	-	F31	P15	
2	45P	G0	H16	-	G1	M13	
2	45N	G2	H17	-	G3	P14	
2	46P	G4	H18	-	G5	—	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
2	46N	G6	H19	-	G7	—	
2	47P	G8	H20	-	G9	—	
-	-	VCCO2	-	-	-	VCCO2	
2	47N	G10	H21	-	G11	—	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	48P	G12	H22	-	G13	—	
2	48N	G14	H23	-	G15	—	
2	49P	G16	H24	-	G17	—	
2	49N	G18	H25	-	G19	—	
2	50P	G20	H26	-	G21	R16	
2	50N	G22	H27	-	G23	P16	
2	51P	G24	H28	-	G25	N15	
-	-	VCCO2	-	-	-	VCCO2	
2	51N	G26	H29	-	G27	N14	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	52P	G28	F16	H16	G29	N16	
2	52N	G30	F17	H17	G31	M16	
2	53P	H0	F18	H18	H1	M14	
2	53N	H2	F19	H19	H3	M15	
2	54P	H4	H30	E24	H5	—	
-	-	VCC	-	-	-	VCC	
2	54N	H6	H31	E26	H7	—	
2	55P	H8	F20	H20	H9	L13	
2	55N	H10	F21	H21	H11	L12	
2	56P	H12	F22	H22	H13	L15	
2	56N	H14	F23	H23	H15	L16	
-	-	GND	-	-	-	GND	
2	57P	H16	F24	H24	H17	L14	
-	-	VCCO2	-	-	-	VCCO2	
2	57N	H18	F25	H25	H19	K15	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	58P	H20	F26	H26	H21	K14	
2	58N	H22	F27	H27	H23	K12	
2	59P	H24	F28	H28	H25	K13	
2	59N	H26	F29	H29	H27	J13	
2	60P	H28	F30	H30	H29	J14	
2	60N	H30	F31	H31	H31	J12	
-	-	TOE	-	-	-	J15	
-	-	RESETB	-	-	-	J11	
-	-	GOE0	-	-	-	H11	
-	-	GOE1	-	-	-	H13	
-	-	GNDP	-	-	-	See Power Su NC Connectio	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
-	GCLK3N	GCLK2	-	-	-	H15	
-	-	VCCP	-	-	-	See Power Su NC Connectio	
-	GCLK3P	GCLK3	-	-	-	H16	
3	61N	J0	L31	J31	-	H14	
3	61P	J2	L30	J30	J3	G16	
3	62N	J4	L29	J29	J5	—	
3	62P	J6	L28	J28	J7	—	
3	63N	J8	L27	J27	J9	—	
3	63P	J10	L26	J26	J11	—	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	64N	J12	L25	J25	J13	—	
-	-	VCCO3	-	-	-	VCCO3	
3	64P	J14	L24	J24	J15	—	
-	-	GND	-	-	-	GND	
3	65N	J16	L23	J23	J17	—	
3	65P	J18	L22	J22	J19	—	
3	66N	J20	L21	J21	J21	—	
3	66P	J22	L20	J20	J23	—	
3	67N	J24	L19	J19	J25	—	
-	-	VCC	-	-	-	VCC	
3	67P	J26	L18	J18	J27	—	
3	68N	J28	L17	J17	J29	—	
3	68P	J30	L16	J16	J31	—	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	69N	L0	L15	J15	-	—	
-	-	VCCO3	-	-	-	VCCO3	
3	69P	L2	L14	J14	L3	—	
3	70N	L4	L13	J13	L5	—	
3	70P	L6	L12	J12	L7	—	
3	71N	L8	L11	J11	L9	—	
3	71P	L10	L10	J10	L11	—	
3	72N	L12	L9	J9	L13	—	
3	72P	L14	L8	J8	L15	—	
3	73N	L16	L7	J7	L17	—	
3	73P	L18	L6	J6	L19	—	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	74N	L20	L5	J5	L21	—	
-	-	VCCO3	-	-	-	VCCO3	
3	74P	L22	L4	J4	L23	—	
3	75N	L24	L3	J3	L25	—	
3	75P	L26	L2	J2	L27	—	
3	76N	L28	L1	J1	L29	G15	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
3	76P	L30/PLL_FBK1	L0	J0	L31	F15	
3	77N	M0/PLL_RST1	P27	N27	M1	H12	
3	77P	M2	P26	N26	M3	G14	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	78N	M4	P25	N25	M5	F16	
-	-	VCCO3	-	-	-	VCCO3	
3	78P	M6	P24	N24	-	E16	
-	-	GND	-	-	-	GND	
3	79N	M8	P23	N23	M9	G13	
3	79P	M10	P22	N22	M11	G12	
3	80N	M12	P21	N21	M13	F14	
3	80P	M14/CLK_OUT1	P20	N20	M15	E15	
3	81N	M16	N31	-	M17	F12	
-	-	VCC	-	-	-	VCC	
3	81P	M18	N30	M30	M19	F13	
3	82N	M20	N29	M28	M21	D16	
3	82P	M22	N28	M26	M23	D15	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	83N	M24	N27	-	M25	—	
-	-	VCCO3	-	-	-	VCCO3	
3	83P	M26	N26	-	M27	—	
3	84N	M28	N25	-	M29	—	
3	84P	M30	N24	-	M31	—	
-	-	GND	-	-	-	GND	
3	85N	N0	N23	-	N1	—	
-	-	VCC	-	-	-	VCC	
3	85P	N2	N22	-	N3	—	
3	86N	N4	N21	-	-	—	
3	86P	N6	N20	-	-	—	
3	87N	N8	N19	-	N9	C16	
3	87P	N10	N18	-	N11	B16	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	88N	N12	N17	-	N13	C15	
-	-	VCCO3	-	-	-	VCCO3	
3	88P	N14	N16	-	N15	B15	
3	89N	N16	N15	-	N17	E14	
3	89P	N18	N14	-	N19	D14	
3	90N	N20	N13	-	N21	E13	
3	90P	N22	N12	-	N23	A15	
3	91N	N24	P19	N19	N25	D12	
3	91P	N26	P18	N18	N27	B14	
3	92N	N28	P17	N17	N29	C13	
3	92P	N30	P16	N16	N31	A14	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
3	93N	O0	P31	N31	O1	A13	
3	93P	O2	P30	N30	O3	B13	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	94N	O4	N11	M21	O5	D11	
-	-	VCCO3	-	-	-	VCCO3	
3	94P	O6	N10	M20	O7	B12	
-	-	GND	-	-	-	GND	
3	95N	O8	N9	M18	O9	C12	
-	-	VCC	-	-	-	VCC	
3	95P	O10	N8	M16	O11	E11	
3	96N	O12	N7	M12	O13	—	
3	96P	O14	N6	M10	O15	—	
3	97N	O16	N5	M8	O17	—	
3	97P	O18	N4	M6	O19	—	
3	98N	O20	N3	M5	O21	—	
3	98P	O22	N2	M4	O23	E10	
3	99N	O24	N1	M2	O25	A12	
3	99P	O26	N0	M0	O27	A11	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	100N	O28	P15	N15	O29	B11	
-	-	VCCO3	-	-	-	VCCO3	
3	100P	O30	P14	N14	O31	C11	
3	101N	P0	P13	N13	P1	B10	
3	101P	P2	P12	N12	P3	A10	
3	102N	P4	P11	N11	P5	C10	
3	102P	P6	P10	N10	P7	D10	
3	103N	P8	P9	N9	P9	C9	
3	103P	P10	P8	N8	P11	E9	
3	104N	P12/VREF3	P29	N29	P13	D9	
3	104P	P14	P28	N28	P15	F9	
3	105N	P16	P7	N7	P17	A9	
3	105P	P18	P6	N6	P19	F8	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	106N	P20	P5	N5	P21	E8	
-	-	VCCO3	-	-	-	VCCO3	
3	106P	P22	P4	N4	P23	A8	
3	107N	P24	P3	N3	P25	B9	
-	-	GND	-	-	-	GND	
3	107P	P26	P2	N2	P27	D8	
-	-	VCC	-	-	-	VCC	
3	108N	P28	P1	N1	P29	B8	
3	108P	P30	P0	N0	P31	C8	
0	109N	Q30	Q31	S31	Q31	B7	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	-	VCC	-	-	-	VCC	
0	109P	Q28	Q30	S30	Q29	A7	
-	-	GND	-	-	-	GND	
0	110N	Q26	Q29	S29	Q27	D7	
0	110P	Q24	Q28	S28	Q25	C7	
0	111N	Q22	Q27	S27	Q23	B6	
-	-	VCCO0	-	-	-	VCCO0	
0	111P	Q20	Q26	S26	Q21	E7	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	112N	Q18	Q25	S25	Q19	E6	
0	112P	Q16	Q24	S24	Q17	A6	
0	113N	Q14/VREF0	Q3	S3	Q15	A5	
0	113P	Q12	Q2	S2	Q13	A4	
0	114N	Q10	Q23	S23	Q11	B5	
0	114P	Q8	Q22	S22	Q9	A3	
0	115N	Q6	Q21	S21	Q7	B4	
0	115P	Q4	Q20	S20	Q5	B3	
0	116N	Q2	Q19	S19	Q3	C5	
0	116P	Q0	Q18	S18	Q1	C6	
0	117N	R30	Q1	S1	R31	D5	
-	-	VCCO0	-	-	-	VCCO0	
0	117P	R28	Q0	S0	R29	D6	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	118N	R26	S29	-	R27	—	
0	118P	R24	S28	-	R25	—	
0	119N	R22	S27	-	R23	—	
0	119P	R20	S26	-	R21	—	
0	120N	R18	S25	-	R19	—	
0	120P	R16	S24	-	R17	—	
0	121N	R14	S23	-	R15	—	
0	121P	R12	S22	-	R13	—	
0	122N	R10	S21	-	R11	—	
-	-	VCC	-	-	-	VCC	
0	122P	R8	S20	-	R9	—	
-	-	GND	-	-	-	GND	
0	123N	R6	S19	-	R7	—	
-	-	VCCO0	-	-	-	VCCO0	
0	123P	R4	S18	-	R5	—	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	124N	R2	S17	-	R3	—	
0	124P	R0	S16	-	R1	—	
0	125N	S30	S15	-	S31	A2	
0	125P	S28	S14	-	S29	B2	

ispXPLD 5768MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/ Function	Alternate Outputs		Alternate Inputs	256 fpBGA Ball Number	4 B
			Macrocell 1	Macrocell 2			
0	126N	S26	S13	-	S27	—	
0	126P	S24	S12	-	S25	—	

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired receive differencial clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

ispXPLD 51024MX Logic Signal Connections

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
0	159N	AA22	AA11	AB18	AA23	B4	
0	159P	AA20	AA10	AB16	AA21	A4	
0	160N	AA18	Y17	AA17	AA19	B3	
0	160P	AA16	Y16	AA16	AA17	A3	
0	161N	AA14	Y15	AA15	AA15	F5	
-	-	VCCO0	-	-	-	VCCO0	
0	161P	AA12	Y14	AA14	AA13	G6	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	162N	AA10	Y13	AA13	AA11	H6	
0	162P	AA8	Y12	AA12	AA9	G5	
0	163N	AA6	AA9	AB14	AA7	D3	
0	163P	AA4	AA8	AB12	AA5	D2	
0	164N	AA2	AA7	AB10	AA3	E4	
-	-	VCC	-	-	-	VCC	
0	164P	AA0	AA6	AB8	AA1	E3	
-	-	GND	-	-	-	GND	
0	165N	AB30	AA5	AB6	AB31	F4	
0	165P	AB28	AA4	AB4	AB29	G4	
0	166N	AB26	AA3	AB2	AB27	C2	
-	-	VCCO0	-	-	-	VCCO0	
0	166P	AB24	AA2	AB0	AB25	C1	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	167N	AB22	AA1	-	AB23	F3	
0	167P	AB20	AA0	-	AB21	G3	
0	168N	AB18	AA31	-	AB19	H4	
-	-	VCC	-	-		VCC	
0	168P	AB16	AA30	-	AB17	J4	
0	169N	AB14	Y11	AA11	AB15	H5	
0	169P	AB12/CLK_OUT0	Y10	AA10	AB13	J5	
0	170N	AB10	Y9	AA9	AB11	E2	
0	170P	AB8	Y8	AA8	AB9	F2	
-	-	GND	-	-	-	GND	
0	171N	AB6	Y7	AA7	AB7	D1	
-	-	VCCO0	-	-	-	VCCO0	
0	171P	AB4	Y6	AA6	AB5	E1	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	172N	AB2	Y5	AA5	AB3	J3	
0	172P	AB0/PLL_RST0	Y4	AA4	AB1	H2	
0	173N	AC30	AC31	AE31	AC31	G2	
0	173P	AC28/PLL_FBK0	AC30	AE30	AC29	G1	
0	174N	AC26	AC29	AE29	AC27	J6	
0	174P	AC24	AC28	AE28	AC25	K4	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
0	175N	AC22	AC27	AE27	AC23	K6	
-	-	VCCO0	-	-	-	VCCO0	
0	175P	AC20	AC26	AE26	AC21	K3	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	176N	AC18	AC25	AE25	AC19	K5	
0	176P	AC16	AC24	AE24	AC17	K2	
0	177N	AC14	AC23	AE23	AC15	L5	
0	177P	AC12	AC22	AE22	AC13	K1	
0	178N	AC10	AC21	AE21	AC11	L6	
0	178P	AC8	AC20	AE20	AC9	L1	
0	179N	AC6	AC19	AE19	AC7	M5	
0	179P	AC4	AC18	AE18	AC5	L2	
0	180N	AC2	AC17	AE17	AC3	N5	
-	-	VCCO0	-	-	-	VCCO0	
0	180P	AC0	AC16	AE16	AC1	L3	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	181N	AE30	AC15	AE15	AE31	M6	
0	181P	AE28	AC14	AE14	AE29	M2	
0	182N	AE26	AC13	AE13	AE27	P5	
-	-	VCC	-	-	-	VCC	
0	182P	AE24	AC12	AE12	AE25	P6	
0	183N	AE22	AC11	AE11	AE23	M3	
0	183P	AE20	AC10	AE10	AE21	N6	
0	184N	AE18	AC9	AE9	AE19	N2	
0	184P	AE16	AC8	AE8	AE17	P1	
-	-	GND	-	-	-	GND	
0	185N	AE14	AC7	AE7	AE15	N3	
-	-	VCCO0	-	-	-	VCCO0	
0	185P	AE12	AC6	AE6	AE13	M8	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	186N	AE10	AC5	AE5	AE11	N8	
0	186P	AE8	AC4	AE4	AE9	P2	
0	187N	AE6	AC3	AE3	AE7	P8	
0	187P	AE4	AC2	AE2	AE5	N4	
0	188N	AE2	AC1	AE1	AE3	H1	
0	188P	AE0	AC0	AE0	AE1	J1	
-	GCLK0P	GCLK0	-	-	-	N7	
-	-	VCCJ	-	-	-	See Power Sup NC Connectio	
-	GCLK0N	GCLK1	-	-	-	P7	
-	-	GND	-	-	-	GND	
-	-	TDI	-	-	-	R1	
-	-	TMS	-	-	-	R2	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	-	TCK	-	-	-	T1	
-	-	TDO	-	-	-	V1	
1	0P	A30	A0	C0	A31	—	
1	0N	A28	A1	C1	A29	—	
1	1P	A26	A2	C2	A27	—	
1	1N	A24	A3	C3	A25	—	
1	2P	A22	A4	C4	A23	—	
1	2N	A20	A5	C5	A21	—	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	3P	A18	A6	C6	A19	—	
-	-	VCCO1	-	-	-	VCCO1	
1	3N	A16	A7	C7	A17	—	
-	-	GND	-	-	-	GND	
1	4P	A14	A8	C8	A15	—	
-	-	VCC	-	-	-	VCC	
1	4N	A12	A9	C9	A13	—	
1	5P	A10	A10	C10	A11	—	
1	5N	A8	A11	C11	A9	—	
1	6P	A6	A12	C12	A7	—	
1	6N	A4	A13	C13	A5	—	
1	7P	A2	A14	C14	A3	—	
1	7N	A0	A15	C15	A1	—	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	8P	C30	A16	C16	C31	—	
-	-	VCCO1	-	-	-	VCCO1	
1	8N	C28	A17	C17	C29	—	
1	9P	C26	A18	C18	C27	—	
1	9N	C24	A19	C19	C25	—	
1	10P	C22	A20	C20	C23	—	
1	10N	C20	A21	C21	C21	—	
1	11P	C18	A22	C22	C19	—	
1	11N	C16	A23	C23	C17	—	
1	12P	C14	A24	C24	C15	—	
1	12N	C12	A25	C25	C13	—	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	13P	C10	A26	C26	C11	—	
-	-	VCCO1	-	-	-	VCCO1	
1	13N	C8	A27	C27	C9	—	
-	-	GND	-	-	-	GND	
1	14P	C6	A28	C28	C7	—	
-	-	VCC	-	-	-	VCC	
1	14N	C4	A29	C29	C5	—	
1	15P	C2	A30	C30	C3	—	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	6 B
			Macrocell 1	Macrocell 2			
1	15N	C0	A31	C31	C1	—	
1	16P	E30/DATA0	G0	E0	E31	W1	
1	16N	E28/DATA1	G1	E1	E29	Y1	
1	17P	E26/DATA2	G2	E2	E27	P3	
1	17N	E24/DATA3	G3	E3	E25	R3	
1	18P	E22/DATA4	G4	E4	E23	T2	
1	18N	E20/DATA5	G5	E5	E21	U2	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	19P	E18/DATA6	G6	E6	E19	V2	
-	-	VCCO1	-	-	-	VCCO1	
1	19N	E16/DATA7	G7	E7	E17	W2	
-	-	GND	-	-	-	GND	
1	20P	E14/INITB	G8	E8	E15	R4	
1	20N	E12/CSB	G9	E9	E13	T4	
1	21P	E10/READ	G10	E10	E11	R6	
1	21N	E8/CCLK	G11	E11	E9	R5	
1	22P	E6	-	-	E7	U3	
-	-	VCC	-	-	-	VCC	
1	22N	E4	-	-	E5	V3	
1	23P	E2	-	-	E3	Y2	
1	23N	E0	-	-	E1	W3	
1	24P	F30	H0	-	F31	U5	
1	24N	F28	H2	-	F29	T5	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	25P	F26	H4		F27	U4	
-	-	VCCO1	-	-	-	VCCO1	
1	25N	F24	H6	-	F25	V4	
1	26P	F22	H8	-	F23	AA3	
1	26N	F20	H10	-	F21	AB3	
1	-	F18	H12	-	F19	Y4	
-	-	DONE	-	-	-	AA4	
1	27P	F14	-	-	F15	AB2	
1	27N	F12	-	-	F13	U6	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	28P	F10			F11	V5	
-	-	VCCO1	-	-	-	VCCO1	
1	28N	F8			F9	W6	
1	29P	F6	G12	E12	F7	AB4	
1	29N	F4	G13	E13	F5	AB5	
1	30P	F2	G14	E14	F3	T6	
1	30N	F0	G15	E15	F1	U7	
-	-	PROGRAMB	-	-	-	W5	
1	-	G28	H14	-	G29	U8	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	31P	G26	H16	-	G27	V6	
-	-	VCCO1	-	-	-	VCCO1	
1	31N	G24	H18	-	G25	V7	
-	-	GND	-	-	-	GND	
1	32P	G22	H20	-	G23	Y5	
-	-	VCC	-	-	-	VCC	
1	32N	G20	H22	-	G21	AA5	
1	33P	G18	-	-	G19	Y6	
1	33N	G16	-	-	G17	Y7	
1	34P	G14	-	-	G15	AA6	
1	34N	G12	-	-	G13	AA7	
1	35P	G10	-	-	G11	W7	
1	35N	G8	-	-	G9	V8	
1	36P	G6	-	-	G7	W8	
1	36N	G4	-	-	G5	U9	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
-	-	CFG0	-	-	-	U10	
-	-	VCCO1	-	-	-	VCCO1	
1	37P	G0	G16	E16	G1	AB7	
1	37N	H30	G17	E17	H31	AA8	
1	38P	H28	G18	E18	H29	AB8	
1	38N	H26	G19	E19	H27	AB9	
1	39P	H24	G20	E20	H25	W9	
1	39N	H22	G21	E21	H23	Y9	
1	40P	H20	G22	E22	H21	AB10	
1	40N	H18	G23	E23	H19	AA10	
1	-	H16/VREF1	-	-	H17	W10	
1	41P	H14	G24	E24	H15	Y10	
1	41N	H12	G25	E25	H13	Y11	
-	-	GND (Bank 1)	-	-	-	GND (Bank 1)	G
1	42P	H10	G26	E26	H11	V9	
-	-	VCCO1	-	-	-	VCCO1	
1	42N	H8	G27	E27	H9	V10	
1	43P	H6	G28	E28	H7	AA11	
-	-	GND	-	-	-	GND	
1	43N	H4	G29	E29	H5	AB11	
-	-	VCC	-	-	-	VCC	
1	44P	H2	G30	E30	H3	U11	
1	44N	H0	G31	E31	H1	V11	
2	45P	I0	J0	L0	I1	AB12	
-	-	VCC	-	-	-	VCC	
2	45N	I2	J1	L1	I3	AA12	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	-	GND	-	-	-	GND	
2	46P	I4	J2	L2	I5	Y12	
2	46N	I6	J3	L3	I7	AA13	
2	47P	I8	J4	L4	I9	V12	
-	-	VCCO2	-	-	-	VCCO2	
2	47N	I10	J5	L5	I11	U12	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	48P	I12	J6	L6	I13	AB13	
2	48N	I14	J7	L7	I15	Y13	
2	49P	I16	L0	-	I17	V13	
2	49N	I18/VREF2	L1	-	I19	W13	
2	50P	I20	J8	L8	I21	V14	
2	50N	I22	J9	L9	I23	W14	
2	51P	I24	J10	L10	I25	Y14	
2	51N	I26	J11	L11	I27	AB14	
2	52P	I28	J12	L12	I29	AB15	
2	52N	I30	J13	L13	I31	AA15	
2	53P	J0	J14	L14	J1	U13	
-	-	VCCO2	-	-	-	VCCO2	
2	53N	J2	J15	L15	J3	U14	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	54P	J4	L2	I0	J5	W15	
2	54N	J6	L3	I2	J7	W16	
2	55P	J8	L4	I4	J9	Y16	
2	55N	J10	L5	I6	J11	AA16	
2	56P	J12	L6	I8	J13	AB16	
2	56N	J14	L7	I10	J15	AA17	
2	57P	J16	L8	I12	J17	Y17	
2	57N	J18	L9	I16	J19	AA18	
2	58P	J20	L10	I20	J21	W17	
-	-	VCC	-	-	-	VCC	
2	58N	J22	L11	I22	J23	W18	
-	-	GND	-	-	-	GND	
2	59P	J24	L12	-	J25	V15	
-	-	VCCO2		-	-	VCCO2	
2	59N	J26	L13	-	J27	U15	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	60P	J28	L14	-	J29	Y18	
2	60N	J30	L15	-	J31	V17	
2	61P	K0	L16	-	K1	V16	
2	61N	K2	L17	-	K3	U16	
2	62P	K4	L18	-	K5	AB18	
2	62N	K6	L19	-	K7	AB19	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
2	63P	K8	L20	-	K9	AA19	
-	-	VCCO2	-	-	-	VCCO2	
2	63N	K10	L21	-	K11	U17	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	64P	K12	L22	-	K13	V18	
2	64N	K14	L23	-	K15	AB21	
2	65P	K16	L24	-	K17	U18	
2	65N	K18	L25	-	K19	T17	
2	66P	K20	L26	-	K21	AB20	
2	66N	K22	L27	-	K23	AA20	
2	67P	K24	L28	-	K25	Y19	
-	-	VCCO2	-	-	-	VCCO2	
2	67N	K26	L29	-	K27	V19	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	68P	K28	J16	L16	K29	T18	
2	68N	K30	J17	L17	K31	R17	
2	69P	L0	J18	L18	L1	U19	
2	69N	L2	J19	L19	L3	T19	
2	70P	L4	L30	I24	L5	V20	
-	-	VCC	-	-	-	VCC	
2	70N	L6	L31	I26	L7	U20	
2	71P	L8	J20	L20	L9	W20	
2	71N	L10	J21	L21	L11	Y21	
2	72P	L12	J22	L22	L13	R18	
2	72N	L14	J23	L23	L15	R19	
-	-	GND	-	-	-	GND	
2	73P	L16	J24	L24	L17	W21	
-	-	VCCO2	-	-	-	VCCO2	
2	73N	L18	J25	L25	L19	Y22	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	74P	L20	J26	L26	L21	R20	
2	74N	L22	J27	L27	L23	P20	
2	75P	L24	J28	L28	L25	T21	
2	75N	L26	J29	L29	L27	R21	
2	76P	L28	J30	L30	L29	U21	
2	76N	L30	J31	L31	L31	V21	
2	77P	N0	P0	N0	N1	—	
2	77N	N2	P1	N1	N3	—	
2	78P	N4	P2	N2	N5	—	
-	-	VCC	-	-	-	VCC	
2	78N	N6	P3	N3	N7	—	
-	-	GND	-	-	-	GND	
2	79P	N8	P4	N4	N9	—	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	-	VCCO2	-	-	-	VCCO2	
2	79N	N10	P5	N5	N11	—	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	80P	N12	P6	N6	N13	—	
2	80N	N14	P7	N7	N15	—	
2	81P	N16	P8	N8	N17	—	
2	81N	N18	P9	N9	N19	—	
2	82P	N20	P10	N10	N21	—	
2	82N	N22	P11	N11	N23	—	
2	83P	N24	P12	N12	N25	—	
2	83N	N26	P13	N13	N27	—	
2	84P	N28	P14	N14	N29	—	
-	-	VCCO2	-	-	-	VCCO2	
2	84N	N30	P15	N15	N31	—	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	85P	P0	P16	N16	P1	—	
2	85N	P2	P17	N17	P3	—	
2	86P	P4	P18	N18	P5	—	
2	86N	P6	P19	N19	P7	—	
2	87P	P8	P20	N20	P9	—	
2	87N	P10	P21	N21	P11	—	
2	88P	P12	P22	N22	P13	—	
-	-	VCC	-	-	-	VCC	
2	88N	P14	P23	N23	P15	—	
-	-	GND	-	-	-	GND	
2	89P	P16	P24	N24	P17	—	
-	-	VCCO2	-	-	-	VCCO2	
2	89N	P18	P25	N25	P19	—	
-	-	GND (Bank 2)	-	-	-	GND (Bank 2)	G
2	90P	P20	P26	N26	P21	—	
2	90N	P22	P27	N27	P23	—	
2	91P	P24	P28	N28	P25	—	
2	91N	P26	P29	N29	P27	—	
2	92P	P28	P30	N30	P29	—	
2	92N	P30	P31	N31	P31	—	
-	-	TOE	-	-	-	W22	
-	-	RESETB	-	-	-	V22	
-	-	GOE0	-	-	-	T22	
-	-	GOE1	-	-	-	R22	
-	-	GNDP	-	-	-	See Power Sup NC Connectio	
-	GCLK3N	GCLK2	-	-	-	P16	
-	-	VCCP	-	-	-	See Power Sup NC Connectio	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	GCLK3P	GCLK3	-	-	-	N16	
3	93N	R0	T31	R31	R1	J22	
3	93P	R2	T30	R30	R3	H22	
3	94N	R4	T29	R29	R5	N19	
3	94P	R6	T28	R28	R7	P15	
3	95N	R8	T27	R27	R9	P21	
3	95P	R10	T26	R26	R11	N15	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	96N	R12	T25	R25	R13	M15	
-	-	VCCO3	-	-	-	VCCO3	
3	96P	R14	T24	R24	R15	N20	
-	-	GND	-	-	-	GND	
3	97N	R16	T23	R23	R17	P22	
3	97P	R18	T22	R22	R19	N21	
3	98N	R20	T21	R21	R21	N17	
3	98P	R22	T20	R20	R23	M20	
3	99N	R24	T19	R19	R25	P17	
-	-	VCC	-	-	-	VCC	
3	99P	R26	T18	R18	R27	P18	
3	100N	R28	T17	R17	R29	M21	
3	100P	R30	T16	R16	R31	M17	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	101N	T0	T15	R15	T1	L20	
-	-	VCCO3	-	-	-	VCCO3	
3	101P	T2	T14	R14	T3	N18	
3	102N	T4	T13	R13	T5	L21	
3	102P	T6	T12	R12	T7	M18	
3	103N	T8	T11	R11	T9	L22	
3	103P	T10	T10	R10	T11	L17	
3	104N	T12	T9	R9	T13	K22	
3	104P	T14	T8	R8	T15	L18	
3	105N	T16	T7	R7	T17	K21	
3	105P	T18	T6	R6	T19	K18	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	106N	T20	T5	R5	T21	K20	
-	-	VCCO3	-	-	-	VCCO3	
3	106P	T22	T4	R4	T23	K17	
3	107N	T24	T3	R3	T25	K19	
3	107P	T26	T2	R2	T27	J17	
3	108N	T28	T1	R1	T29	E22	
3	108P	T30/PLL_FBK1	T0	R0	T31	E21	
3	109N	U0/PLL_RST1	X27	V27	U1	G22	
3	109P	U2	X26	V26	U3	F21	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	110N	U4	X25	V25	U5	H21	
-	-	VCCO3	-	-	-	VCCO3	
3	110P	U6	X24	V24	U7	G21	
-	-	GND	-	-	-	GND	
3	111N	U8	X23	V23	U9	D22	
3	111P	U10	X22	V22	U11	D21	
3	112N	U12	X21	V21	U13	J20	
3	112P	U14/CLK_OUT1	X20	V20	U15	J19	
3	113N	U16	V31	-	U17	E20	
-	-	VCC	-	-	-	VCC	
3	113P	U18	V30	U30	U19	F20	
3	114N	U20	V29	U28	U21	H17	
3	114P	U22	V28	U26	U23	H18	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	115N	U24	V27	-	U25	J18	
-	-	VCCO3	-	-	-	VCCO3	
3	115P	U26	V26	-	U27	H19	
3	116N	U28	V25	-	U29	G20	
3	116P	U30	V24	-	U31	G19	
-	-	GND	-	-	-	GND	
3	117N	V0	V23	-	V1	C22	
-	-	VCC	-	-	-	VCC	
3	117P	V2	V22	-	V3	C21	
3	118N	V4	V21	-	V5	D20	
3	118P	V6	V20	-	V7	C19	
3	119N	V8	V19	-	V9	F19	
3	119P	V10	V18	-	V11	E19	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	120N	V12	V17	-	V13	G18	
-	-	VCCO3	-	-	-	VCCO3	
3	120P	V14	V16	-	V15	F18	
3	121N	V16	V15	-	V17	B20	
3	121P	V18	V14	-	V19	B19	
3	122N	V20	V13	-	V21	A20	
3	122P	V22	V12	-	V23	A19	
3	123N	V24	X19	V19	V25	D18	
3	123P	V26	X18	V18	V27	C18	
3	124N	V28	X17	V17	V29	G17	
3	124P	V30	X16	V16	V31	F16	
3	125N	W0	X31	V31	W1	E17	
3	125P	W2	X30	V30	W3	D17	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G

ispXPLD 51024MX Logic Signal Connections (Continued)

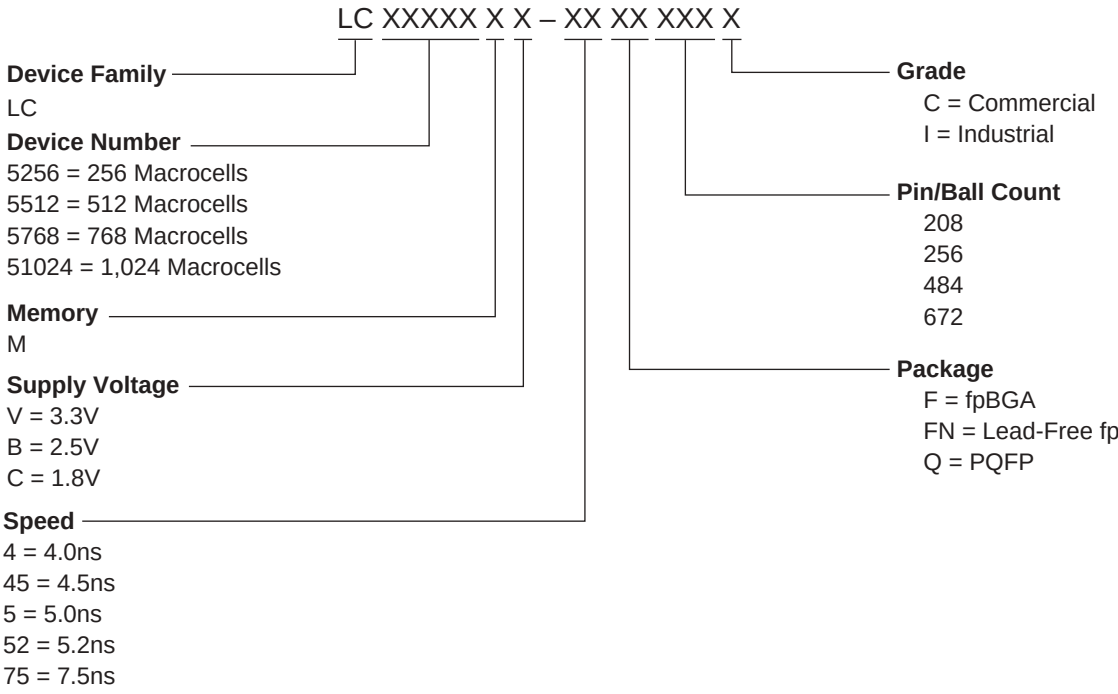
sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
3	126N	W4	V11	U21	W5	B18	
-	-	VCCO3	-	-	-	VCCO3	
3	126P	W6	V10	U20	W7	A18	
-	-	GND	-	-	-	GND	
3	127N	W8	V9	U18	W9	C17	
-	-	VCC	-	-	-	VCC	
3	127P	W10	V8	U16	W11	B17	
3	128N	W12	V7	U12	W13	C16	
3	128P	W14	V6	U10	W15	B16	
3	129N	W16	V5	U8	W17	F13	
3	129P	W18	V4	U6	W19	F15	
3	130N	W20	V3	U5	W21	D16	
3	130P	W22	V2	U4	W23	E16	
3	131N	W24	V1	U2	W25	A16	
3	131P	W26	V0	U0	W27	A15	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	132N	W28	X15	V15	W29	B15	
-	-	VCCO3	-	-	-	VCCO3	
3	132P	W30	X14	V14	W31	A14	
3	133N	X0	X13	V13	X1	D15	
3	133P	X2	X12	V12	X3	E15	
3	134N	X4	X11	V11	X5	D14	
3	134P	X6	X10	V10	X7	F14	
3	135N	X8	X9	V9	X9	A13	
3	135P	X10	X8	V8	X11	B13	
3	136N	X12/VREF3	X29	V29	X13	C14	
3	136P	X14	X28	V28	X15	E14	
3	137N	X16	X7	V7	X17	E13	
3	137P	X18	X6	V6	X19	F12	
-	-	GND (Bank 3)	-	-	-	GND (Bank 3)	G
3	138N	X20	X5	V5	X21	D13	
-	-	VCCO3	-	-	-	VCCO3	
3	138P	X22	X4	V4	X23	C13	
3	139N	X24	X3	V3	X25	E12	
-	-	GND	-	-	-	GND	
3	139P	X26	X2	V2	X27	C12	
-	-	VCC	-	-	-	VCC	
3	140N	X28	X1	V1	X29	B12	
3	140P	X30	X0	V0	X31	A12	
0	141N	Y30	Y31	AA31	Y31	E11	
-	-	VCC	-	-	-	VCC	
0	141P	Y28	Y30	AA30	Y29	C11	
-	-	GND	-	-	-	GND	

ispXPLD 51024MX Logic Signal Connections (Continued)

sysIO Bank	LVDS Pair	Primary Macrocell/Function	Alternate Outputs		Alternate Input	484 fpBGA Ball Number	
			Macrocell 1	Macrocell 2			
0	142N	Y26	Y29	AA29	Y27	B11	
0	142P	Y24	Y28	AA28	Y25	A11	
0	143N	Y22	Y27	AA27	Y23	F11	
-	-	VCCO0	-	-	-	VCCO0	
0	143P	Y20	Y26	AA26	Y21	F10	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	144N	Y18	Y25	AA25	Y19	E10	
0	144P	Y16	Y24	AA24	Y17	C10	
0	145N	Y14/VREF0	Y3	AA3	Y15	D10	
0	145P	Y12	Y2	AA2	Y13	B10	
0	146N	Y10	Y23	AA23	Y11	A10	
0	146P	Y8	Y22	AA22	Y9	A9	
0	147N	Y6	Y21	AA21	Y7	C9	
0	147P	Y4	Y20	AA20	Y5	D9	
0	148N	Y2	Y19	AA19	Y3	F9	
0	148P	Y0	Y18	AA18	Y1	E9	
0	149N	Z30	Y1	AA1	Z31	A8	
-	-	VCCO0	-	-	-	VCCO0	
0	149P	Z28	Y0	AA0	Z29	B8	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	150N	Z26	AA29	-	Z27	A7	
0	150P	Z24	AA28	-	Z25	B7	
0	151N	Z22	AA27	-	Z23	A5	
0	151P	Z20	AA26	-	Z21	B5	
0	152N	Z18	AA25	-	Z19	B6	
0	152P	Z16	AA24	-	Z17	C7	
0	153N	Z14	AA23	-	Z15	E8	
0	153P	Z12	AA22	-	Z13	E7	
0	154N	Z10	AA21	-	Z11	E6	
-	-	VCC	-	-	-	VCC	
0	154P	Z8	AA20	-	Z9	D6	
-	-	GND	-	-	-	GND	
0	155N	Z6	AA19	-	Z7	D8	
-	-	VCCO0	-	-	-	VCCO0	
0	155P	Z4	AA18	-	Z5	F8	
-	-	GND (Bank 0)	-	-	-	GND (Bank 0)	G
0	156N	Z2	AA17	-	Z3	F7	
0	156P	Z0	AA16	-	Z1	D7	
0	157N	AA30	AA15	-	AA31	C6	
0	157P	AA28	AA14	-	AA29	C5	
0	158N	AA26	AA13	-	AA27	C4	
0	158P	AA24	AA12	-	AA25	D5	

Global Clock LVDS pair options: GCLK0 and GCLK1, as well as GCLK2 and GCLK3, can be paired together to rec
tial clocks; where GCLK0 and GCLK3 are the positive LVDS inputs.

Part Number Description



Ordering Information

Note: For voltage families offered in industrial temperature grades and for all but the slowest comme grade, the speed grades on these devices are dual marked. For example, the commercial speed grade is also marked with the industrial grade -75I. The commercial grade is always one speed grade fas associated dual mark industrial grade. The slowest commercial speed grade is marked as commercial

Conventional Packaging

ispXPLD 5000MC (1.8V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/C
LC5256MC	LC5256MC-4F256C	256	1.8	4.0	fpBGA	256	14
	LC5256MC-5F256C	256	1.8	5.0	fpBGA	256	14
	LC5256MC-75F256C	256	1.8	7.5	fpBGA	256	14
LC5512MC	LC5512MC-45Q208C	512	1.8	4.5	PQFP	208	14
	LC5512MC-75Q208C	512	1.8	7.5	PQFP	208	14
	LC5512MC-45F256C	512	1.8	4.5	fpBGA	256	19
	LC5512MC-75F256C	512	1.8	7.5	fpBGA	256	19
	LC5512MC-45F484C	512	1.8	4.5	fpBGA	484	25
	LC5512MC-75F484C	512	1.8	7.5	fpBGA	484	25
LC5768MC	LC5768MC-5F256C	768	1.8	5.0	fpBGA	256	19
	LC5768MC-75F256C	768	1.8	7.5	fpBGA	256	19
	LC5768MC-5F484C	768	1.8	5.0	fpBGA	484	31
	LC5768MC-75F484C	768	1.8	7.5	fpBGA	484	31

ispXPLD 5000MC (1.8V) Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/C
LC51024MC	LC51024MC-52F484C	1024	1.8	5.2	fpBGA	484	31
	LC51024MC-75F484C	1024	1.8	7.5	fpBGA	484	31
	LC51024MC-52F672C	1024	1.8	5.2	fpBGA	672	38
	LC51024MC-75F672C	1024	1.8	7.5	fpBGA	672	38

ispXPLD 5000MC (1.8V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/C
LC5256MC	LC5256MC-5F256I	256	1.8	5.0	fpBGA	256	14
	LC5256MC-75F256I	256	1.8	7.5	fpBGA	256	14
LC5512MC	LC5512MC-75Q208I	512	1.8	7.5	PQFP	208	14
	LC5512MC-75F256I	512	1.8	7.5	fpBGA	256	19
	LC5512MC-75F484I	512	1.8	7.5	fpBGA	484	25
LC5768MC	LC5768MC-75F256I	768	1.8	7.5	fpBGA	256	19
	LC5768MC-75F484I	768	1.8	7.5	fpBGA	484	31
LC51024MC	LC51024MC-75F484I	1024	1.8	7.5	fpBGA	484	31
	LC51024MC-75F672I	1024	1.8	7.5	fpBGA	672	38

ispXPLD 5000MB (2.5V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/C
LC5256MB	LC5256MB-4F256C	256	2.5	4.0	fpBGA	256	14
	LC5256MB-5F256C	256	2.5	5.0	fpBGA	256	14
	LC5256MB-75F256C	256	2.5	7.5	fpBGA	256	14
LC5512MB	LC5512MB-45Q208C	512	2.5	4.5	PQFP	208	14
	LC5512MB-75Q208C	512	2.5	7.5	PQFP	208	14
	LC5512MB-45F256C	512	2.5	4.5	fpBGA	256	19
	LC5512MB-75F256C	512	2.5	7.5	fpBGA	256	19
	LC5512MB-45F484C	512	2.5	4.5	fpBGA	484	25
	LC5512MB-75F484C	512	2.5	7.5	fpBGA	484	25
LC5768MB	LC5768MB-5F256C	768	2.5	5.0	fpBGA	256	19
	LC5768MB-75F256C	768	2.5	7.5	fpBGA	256	19
	LC5768MB-5F484C	768	2.5	5.0	fpBGA	484	31
	LC5768MB-75F484C	768	2.5	7.5	fpBGA	484	31
LC51024MB	LC51024MB-52F484C	1024	2.5	5.2	fpBGA	484	31
	LC51024MB-75F484C	1024	2.5	7.5	fpBGA	484	31
	LC51024MB-52F672C	1024	2.5	5.2	fpBGA	672	38
	LC51024MB-75F672C	1024	2.5	7.5	fpBGA	672	38

ispXPLD 5000MB (2.5V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/C
LC5256MB	LC5256MB-5F256I	256	2.5	5.0	fpBGA	256	14
	LC5256MB-75F256I	256	2.5	7.5	fpBGA	256	14

ispXPLD 5000MB (2.5V) Industrial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5512MB	LC5512MB-75Q208I	512	2.5	7.5	PQFP	208	149
	LC5512MB-75F256I	512	2.5	7.5	fpBGA	256	193
	LC5512MB-75F484I	512	2.5	7.5	fpBGA	484	253
LC5768MB	LC5768MB-75F256I	768	2.5	7.5	fpBGA	256	193
	LC5768MB-75F484I	768	2.5	7.5	fpBGA	484	317
LC51024MB	LC51024MB-75F484I	1024	2.5	7.5	fpBGA	484	317
	LC51024MB-75F672I	1024	2.5	7.5	fpBGA	672	381

ispXPLD 5000MV (3.3V) Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5256MV	LC5256MV-4F256C	256	3.3	4.0	fpBGA	256	141
	LC5256MV-5F256C	256	3.3	5.0	fpBGA	256	141
	LC5256MV-75F256C	256	3.3	7.5	fpBGA	256	141
LC5512MV	LC5512MV-45Q208C	512	3.3	4.5	PQFP	208	149
	LC5512MV-75Q208C	512	3.3	7.5	PQFP	208	149
	LC5512MV-45F256C	512	3.3	4.5	fpBGA	256	193
	LC5512MV-75F256C	512	3.3	7.5	fpBGA	256	193
	LC5512MV-45F484C	512	3.3	4.5	fpBGA	484	253
	LC5512MV-75F484C	512	3.3	7.5	fpBGA	484	253
LC5768MV	LC5768MV-5F256C	768	3.3	5.0	fpBGA	256	193
	LC5768MV-75F256C	768	3.3	7.5	fpBGA	256	193
	LC5768MV-5F484C	768	3.3	5.0	fpBGA	484	317
	LC5768MV-75F484C	768	3.3	7.5	fpBGA	484	317
LC51024MV	LC51024MV-52F484C	1024	3.3	5.2	fpBGA	484	317
	LC51024MV-75F484C	1024	3.3	7.5	fpBGA	484	317
	LC51024MV-52F672C	1024	3.3	5.2	fpBGA	672	381
	LC51024MV-75F672C	1024	3.3	7.5	fpBGA	672	381

ispXPLD 5000MV (3.3V) Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5256MV	LC5256MV-5F256I	256	3.3	5.0	fpBGA	256	141
	LC5256MV-75F256I	256	3.3	7.5	fpBGA	256	141
LC5512MV	LC5512MV-75Q208I	512	3.3	7.5	PQFP	208	149
	LC5512MV-75F256I	512	3.3	7.5	fpBGA	256	193
	LC5512MV-75F484I	512	3.3	7.5	fpBGA	484	253
LC5768MV	LC5768MV-75F256I	768	3.3	7.5	fpBGA	256	193
	LC5768MV-75F484I	768	3.3	7.5	fpBGA	484	317
LC51024MV	LC51024MV-75F484I	1024	3.3	7.5	fpBGA	484	317
	LC51024MV-75F672I	1024	3.3	7.5	fpBGA	672	381

Lead-Free Packaging

ispXPLD 5000MC (1.8V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5256MC	LC5256MC-4FN256C	256	1.8	4.0	Lead-free fpBGA	256	14
	LC5256MC-5FN256C	256	1.8	5.0	Lead-free fpBGA	256	14
	LC5256MC-75FN256C	256	1.8	7.5	Lead-free fpBGA	256	14
LC5512MC	LC5512MC-45FN256C	512	1.8	4.5	Lead-free fpBGA	256	19
	LC5512MC-75FN256C	512	1.8	7.5	Lead-free fpBGA	256	19
	LC5512MC-45FN484C	512	1.8	4.5	Lead-free fpBGA	484	25
	LC5512MC-75FN484C	512	1.8	7.5	Lead-free fpBGA	484	25
LC5768MC	LC5768MC-5FN256C	768	1.8	5.0	Lead-free fpBGA	256	19
	LC5768MC-75FN256C	768	1.8	7.5	Lead-free fpBGA	256	19
	LC5768MC-5FN484C	768	1.8	5.0	Lead-free fpBGA	484	31
	LC5768MC-75FN484C	768	1.8	7.5	Lead-free fpBGA	484	31
LC51024MC	LC51024MC-52FN484C	1024	1.8	5.2	Lead-free fpBGA	484	31
	LC51024MC-75FN484C	1024	1.8	7.5	Lead-free fpBGA	484	31
	LC51024MC-52FN672C	1024	1.8	5.2	Lead-free fpBGA	672	38
	LC51024MC-75FN672C	1024	1.8	7.5	Lead-free fpBGA	672	38

ispXPLD 5000MC (1.8V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5256MC	LC5256MC-5FN256I	256	1.8	5.0	Lead-free fpBGA	256	14
	LC5256MC-75FN256I	256	1.8	7.5	Lead-free fpBGA	256	14
LC5512MC	LC5512MC-75FN256I	512	1.8	7.5	Lead-free fpBGA	256	19
	LC5512MC-75FN484I	512	1.8	7.5	Lead-free fpBGA	484	25
LC5768MC	LC5768MC-75FN256I	768	1.8	7.5	Lead-free fpBGA	256	19
	LC5768MC-75FN484I	768	1.8	7.5	Lead-free fpBGA	484	31
LC51024MC	LC51024MC-75FN484I	1024	1.8	7.5	Lead-free fpBGA	484	31
	LC51024MC-75FN672I	1024	1.8	7.5	Lead-free fpBGA	672	38

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5256MV	LC5256MV-4FN256C	256	3.3	4.0	Lead-free fpBGA	256	14
	LC5256MV-5FN256C	256	3.3	5.0	Lead-free fpBGA	256	14
	LC5256MV-75FN256C	256	3.3	7.5	Lead-free fpBGA	256	14
LC5512MV	LC5512MV-45FN256C	512	3.3	4.5	Lead-free fpBGA	256	19
	LC5512MV-75FN256C	512	3.3	7.5	Lead-free fpBGA	256	19
	LC5512MV-45FN484C	512	3.3	4.5	Lead-free fpBGA	484	25
	LC5512MV-75FN484C	512	3.3	7.5	Lead-free fpBGA	484	25
LC5768MV	LC5768MV-5FN256C	768	3.3	5.0	Lead-free fpBGA	256	19
	LC5768MV-75FN256C	768	3.3	7.5	Lead-free fpBGA	256	19
	LC5768MV-5FN484C	768	3.3	5.0	Lead-free fpBGA	484	31
	LC5768MV-75FN484C	768	3.3	7.5	Lead-free fpBGA	484	31

ispXPLD 5000MV (3.3V) Lead-Free Commercial Devices (Continued)

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC51024MV	LC51024MV-52FN484C	1024	3.3	5.2	Lead-free fpBGA	484	31
	LC51024MV-75FN484C	1024	3.3	7.5	Lead-free fpBGA	484	31
	LC51024MV-52FN672C	1024	3.3	5.2	Lead-free fpBGA	672	38
	LC51024MV-75FN672C	1024	3.3	7.5	Lead-free fpBGA	672	38

ispXPLD 5000MV (3.3V) Lead-Free Industrial Devices

Device	Part Number	Macrocells	Voltage (V)	t_{PD} (ns)	Package	Pin/Ball Count	I/O
LC5256MV	LC5256MV-5FN256I	256	3.3	5.0	Lead-free fpBGA	256	14
	LC5256MV-75FN256I	256	3.3	7.5	Lead-free fpBGA	256	14
LC5512MV	LC5512MV-75FN256I	512	3.3	7.5	Lead-free fpBGA	256	19
	LC5512MV-75FN484I	512	3.3	7.5	Lead-free fpBGA	484	25
LC5768MV	LC5768MV-75FN256I	768	3.3	7.5	Lead-free fpBGA	256	19
	LC5768MV-75FN484I	768	3.3	7.5	Lead-free fpBGA	484	31
LC51024MV	LC51024MV-75FN484I	1024	3.3	7.5	Lead-free fpBGA	484	31
	LC51024MV-75FN672I	1024	3.3	7.5	Lead-free fpBGA	672	38

For Further Information

In addition to this data sheet, the following technical notes may be helpful when designing with th 5000MX family:

- sysIO Usage Guidelines for Lattice Devices (TN1000)
- Lattice sysCLOCK PLL Design and Usage Guidelines (TN1003)
- Power Estimation in ispXPLD 5000MX Devices (TN1031)
- Using Memory in ispXPLD 5000MX Devices (TN1030)
- ispXP Configuration Usage Guidelines (TN1026)