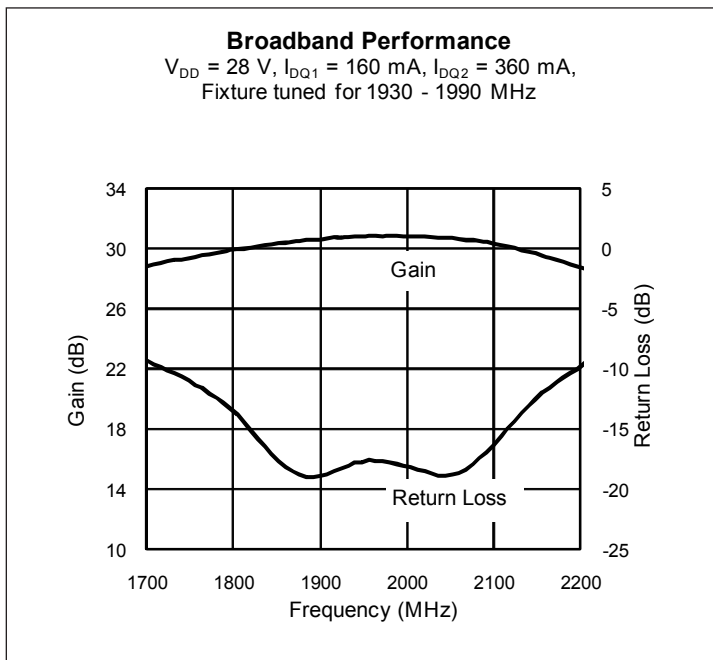


# Wideband RF LDMOS Integrated Power Amplifier 40 W, 1800 – 2100 MHz

## Description

The PTMA180402M is a matched, wideband, 2-stage, 40-watt LDMOS integrated amplifier intended for base station applications in the 1800 to 2100 MHz frequency band. This device is offered in a 20-pin, thermally-enhanced, overmolded plastic package for cool and reliable operation.

PTMA180402M  
Package PG-DSO-20-63



## Features

- Designed for wide RF bandwidth and low memory effects
- On-chip matching, integrated input DC block, 50-ohm input and ~4-ohm output
- Typical single-carrier CDMA performance at 1960 MHz, 28 V
  - Average output power = 5 W
  - Linear gain = 30 dB
  - Efficiency = 16%
  - Adjacent channel power = -52 dBc
- Typical two-tone CW performance at 1960 MHz, 28 V
  - Output power (PEP) = 40 W at IMD3 = -30 dBc
  - Efficiency = 34%
- Capable of handling 10:1 VSWR @ 28 V, 40 W (CW) output power
- Integrated ESD protection. Meets HBM Class 1B (minimum), per JESD22-A114F
- Thermally-enhanced, RoHS-compliant package

## RF Characteristics

### CDMA Measurements (tested in Infineon production test fixture)

$V_{DD} = 28\text{ V}$ ,  $I_{DQ1} = 160\text{ mA}$ ,  $I_{DQ2} = 360\text{ mA}$ ,  $P_{OUT} = 5\text{ W}$  average,  $f = 1960\text{ MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	$G_{ps}$	29.5	30	—	dB
Power Added Efficiency	PAE	14	16	—	%
Adjacent Channel Power Ratio	ACPR	—	-52	-50	dBc

*table continued next page*

All published data at  $T_{CASE} = 25^{\circ}\text{C}$  unless otherwise indicated

**ESD:** Electrostatic discharge sensitive device—observe handling precautions!

**RF Characteristics** (cont.)

**Two-tone Specifications** (not subject to production test—verified by design/characterization in Infineon test fixture)  
 $V_{DD} = 28\text{ V}$ ,  $I_{DQ1} = 160\text{ mA}$ ,  $I_{DQ2} = 360\text{ mA}$ ,  $P_{OUT} = 40\text{ W PEP}$ ,  $f = 1960\text{ MHz}$ , tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	$G_{ps}$	—	30	—	dB
Power Added Efficiency	PAE	—	34	—	%
Intermodulation Distortion	IMD3	—	-32	—	dBc

**DC Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_{DS} = 10\text{ mA}$	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	$V_{DS} = 28\text{ V}$ , $V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	1.0	$\mu\text{A}$
	$V_{DS} = 63\text{ V}$ , $V_{GS} = 0\text{ V}$	$I_{DSS}$	—	—	10.0	$\mu\text{A}$
Final Stage On-state Resistance	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0.1\text{ V}$	$R_{DS(on)}$	—	0.21	—	$\Omega$
Operating Gate Voltage	$V_{DS} = 28\text{ V}$ , $I_{DQ1} = 160\text{ mA}$ , $I_{DQ2} = 360\text{ mA}$	$V_{GS}$	2.0	2.5	3.0	V
Gate Leakage Current	$V_{GS} = 10\text{ V}$ , $V_{DS} = 0\text{ V}$	$I_{GSS}$	—	—	1.0	$\mu\text{A}$

**Maximum Ratings**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	65	V
Gate-Source Voltage	$V_{GS}$	-0.5 to +12	V
Junction Temperature	$T_J$	200	$^{\circ}\text{C}$
Total Device Dissipation	$P_D$	175	W
Above 25 $^{\circ}\text{C}$ derate by		1.0	W/ $^{\circ}\text{C}$
Storage Temperature Range	$T_{STG}$	-40 to +150	$^{\circ}\text{C}$
Overall Thermal Resistance ( $T_{CASE} = 70^{\circ}\text{C}$ , 40 W CW)	Stage 1	$R_{\theta JC}$	3.6 $^{\circ}\text{C/W}$
	Stage 2	$R_{\theta JC}$	1.5 $^{\circ}\text{C/W}$
$P_{OUT} = 40\text{ W}$ , $I_{DQ1} = 160\text{ mA}$ , $I_{DQ2} = 360\text{ mA}$			

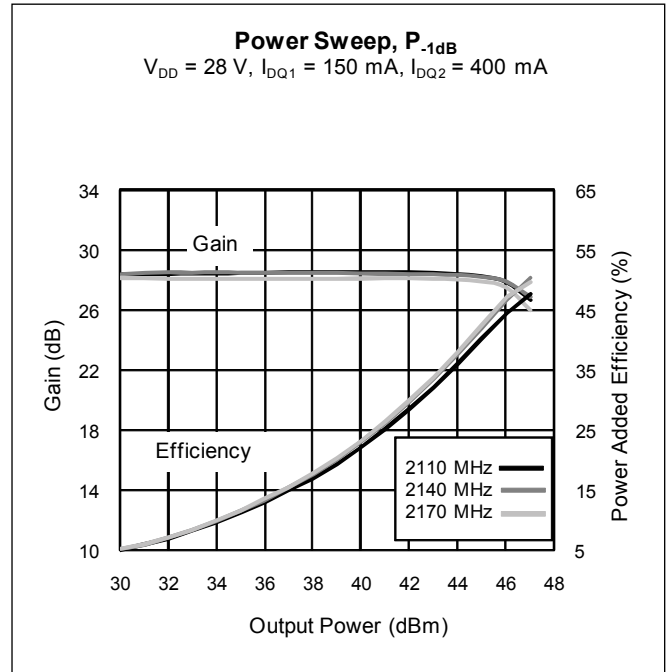
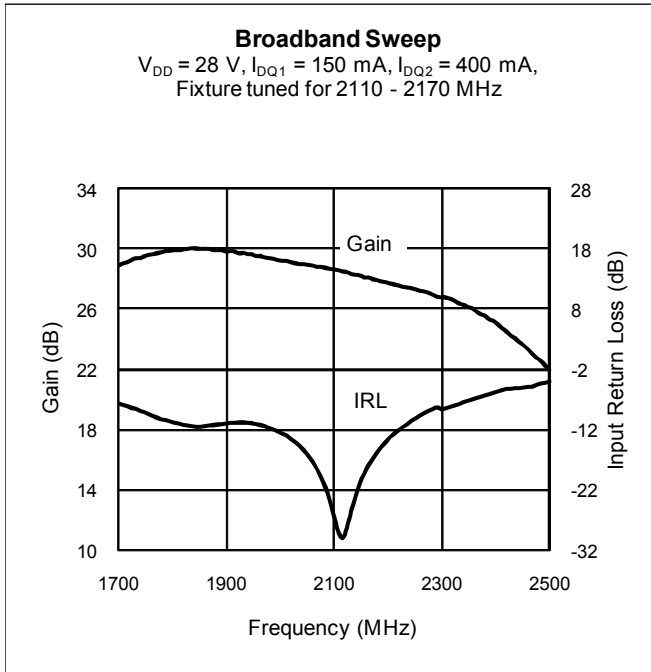
### Moisture Sensitivity Level

Level	Test Standard	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

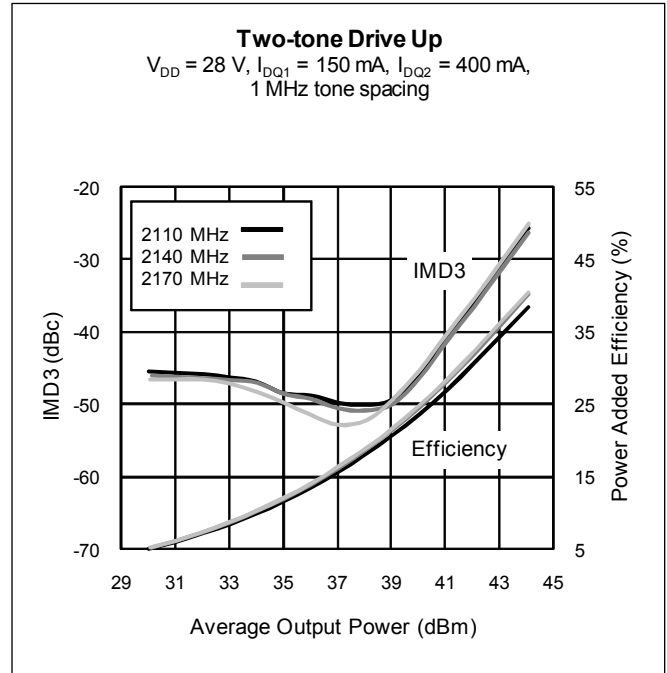
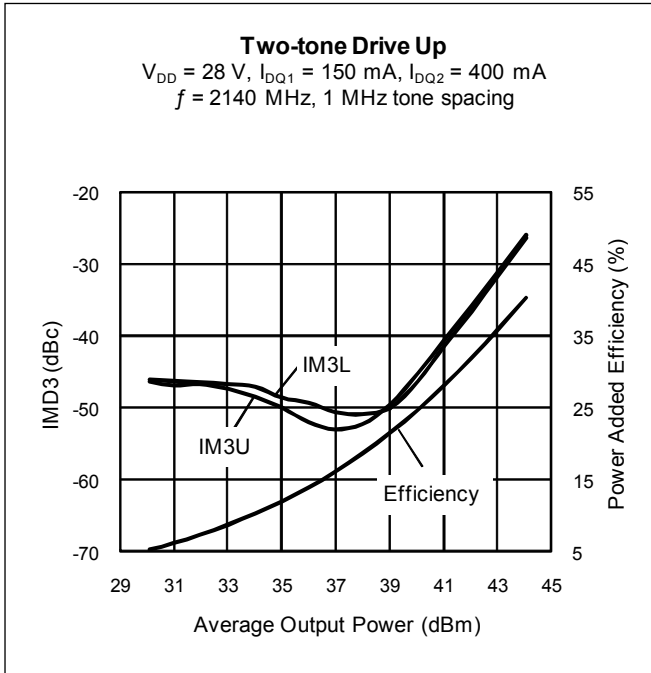
### Ordering Information

Type and Version	Package Outline	Package Description	Shipping
PTMA180402M V1	PG-DSO-20-63	Copper heat slug, plastic EMC body	Tape

### Typical Performance, circuit tuned for 2140 MHz (data taken in Infineon test fixture)

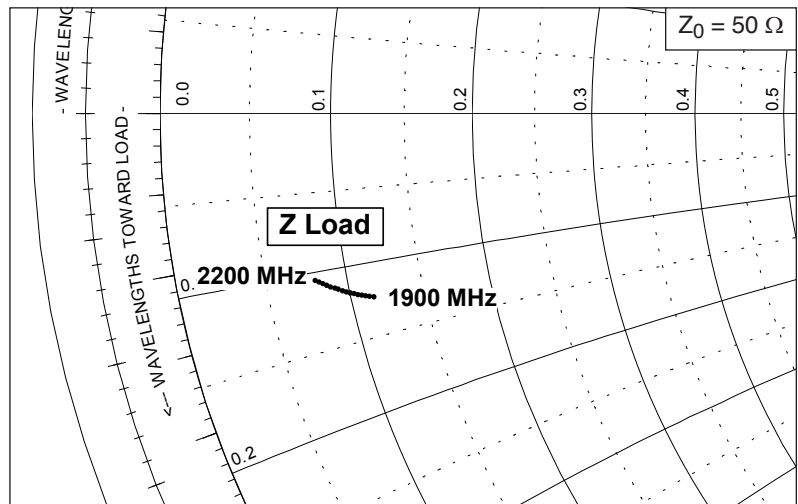
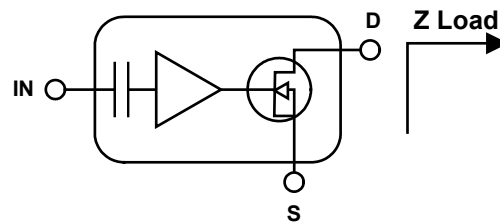


Typical Performance, circuit tuned for 2140 MHz (cont.)

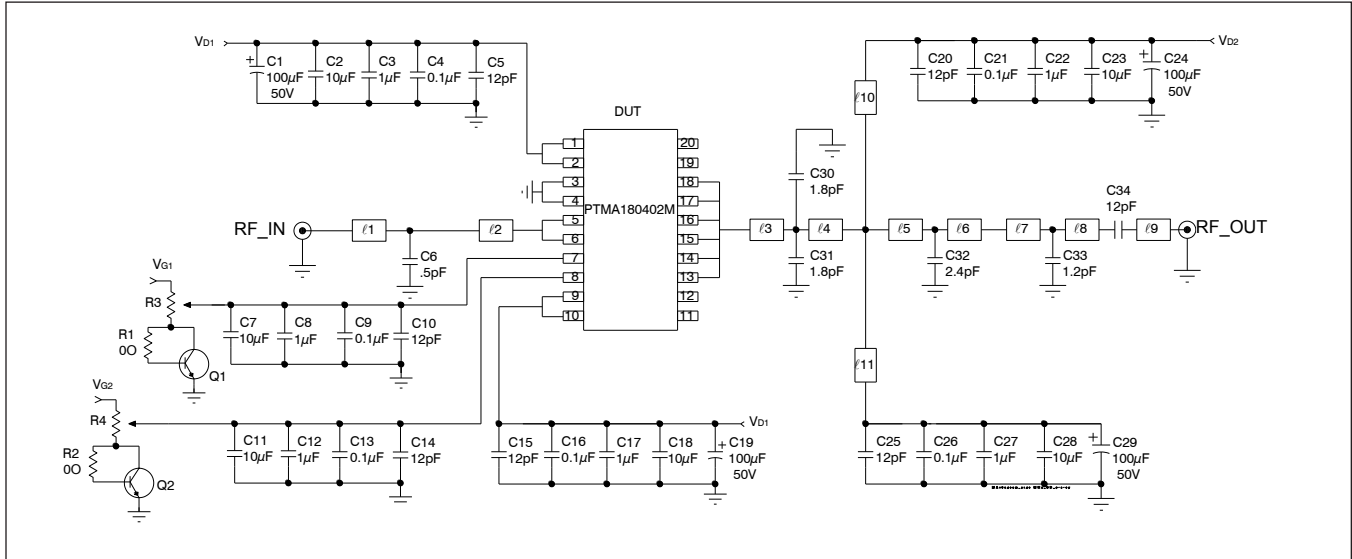


Broadband Circuit Impedance — 2140 MHz

Frequency MHz	Z Load $\Omega$	
	R	jX
1900	5.76	-6.18
1920	5.63	-6.13
1940	5.51	-6.09
1960	5.39	-6.04
1980	5.27	-5.99
2000	5.15	-5.93
2020	5.03	-5.88
2040	4.92	-5.82
2060	4.80	-5.76
2080	4.68	-5.69
2100	4.57	-5.63
2120	4.45	-5.56
2140	4.34	-5.49
2160	4.23	-5.41
2180	4.12	-5.34
2200	4.01	-5.26



Reference Circuit, tuned for 2140 MHz



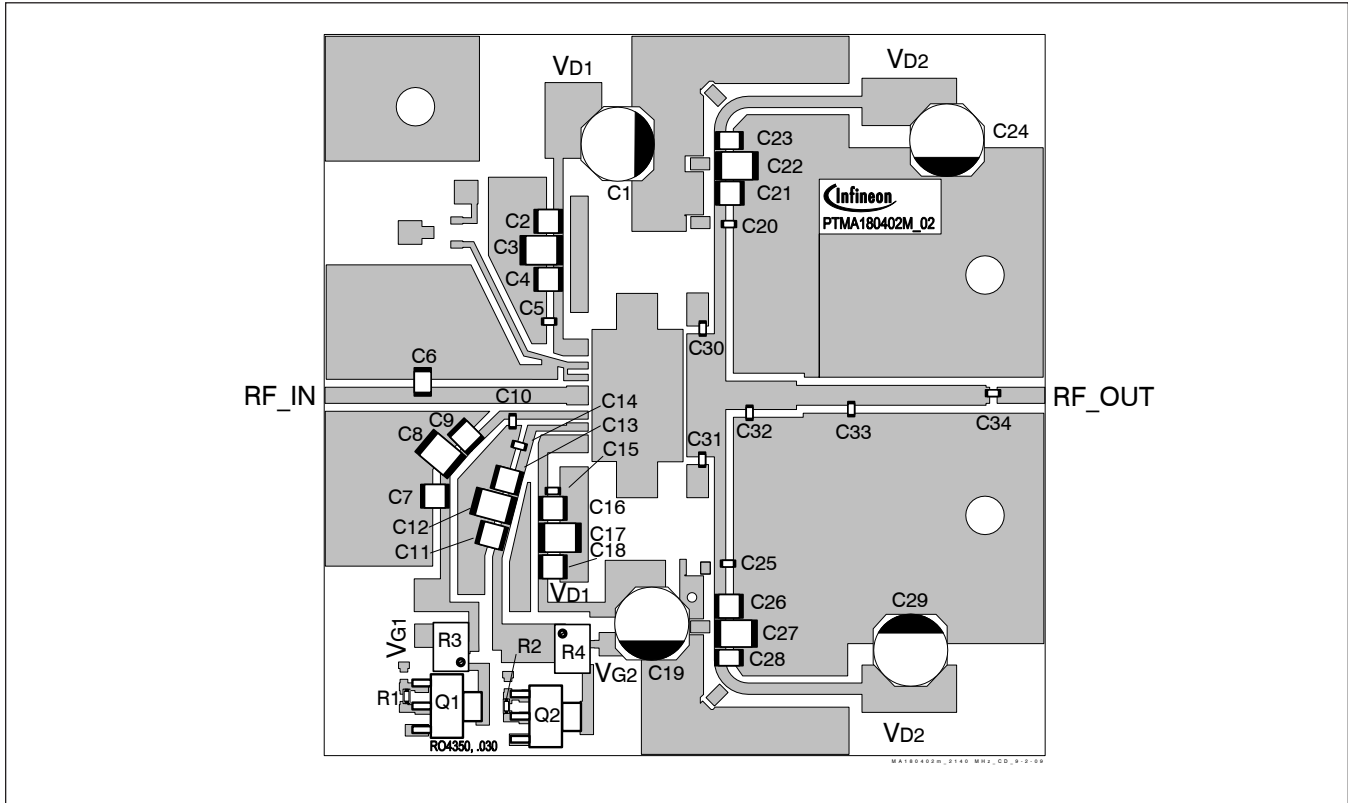
Reference circuit schematic for  $f = 2140$  MHz

Circuit Assembly Information

DUT	PTMA180402M	LDMOS IC
PCB	LTN/PTMA180402M-21	Rogers RO4350: 0.76 mm [.030"] thick, $\epsilon_r = 3.48$ , 1 oz. copper

Microstrip	Electrical Characteristics at 2140 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
l1	0.150 $\lambda$ , 50.0 $\Omega$	12.73 x 1.70	0.501 x 0.067
l2	0.177 $\lambda$ , 50.0 $\Omega$	15.04 x 1.70	0.592 x 0.067
l3	0.026 $\lambda$ , 10.4 $\Omega$	2.01 x 13.00	0.079 x 0.512
l4	0.026 $\lambda$ , 10.4 $\Omega$	2.06 x 13.00	0.081 x 0.512
l5	0.026 $\lambda$ , 34.2 $\Omega$	2.13 x 3.00	0.084 x 0.118
l6	0.054 $\lambda$ , 34.2 $\Omega$	4.45 x 3.00	0.175 x 0.118
l7	0.066 $\lambda$ , 43.5 $\Omega$	5.56 x 2.11	0.219 x 0.083
l8	0.178 $\lambda$ , 43.5 $\Omega$	14.96 x 2.11	0.589 x 0.083
l9	0.059 $\lambda$ , 50.0 $\Omega$	5.03 x 1.70	0.198 x 0.067
l10, l11	0.137 $\lambda$ , 47.8 $\Omega$	11.56 x 1.83	0.455 x 0.072

Reference Circuit — 2140 MHz (cont.)

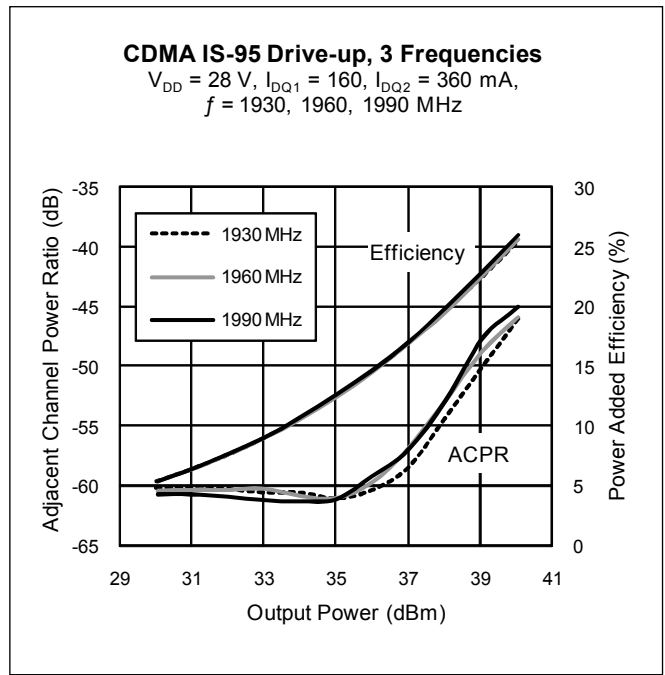
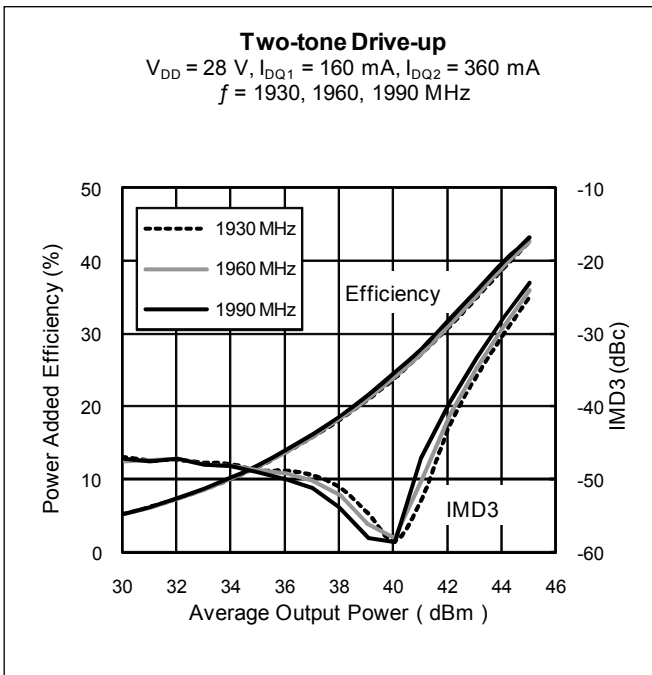
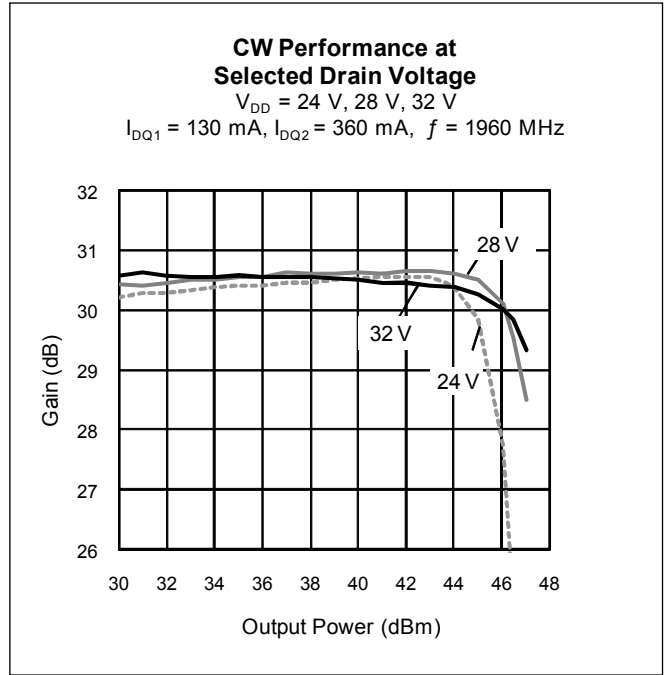
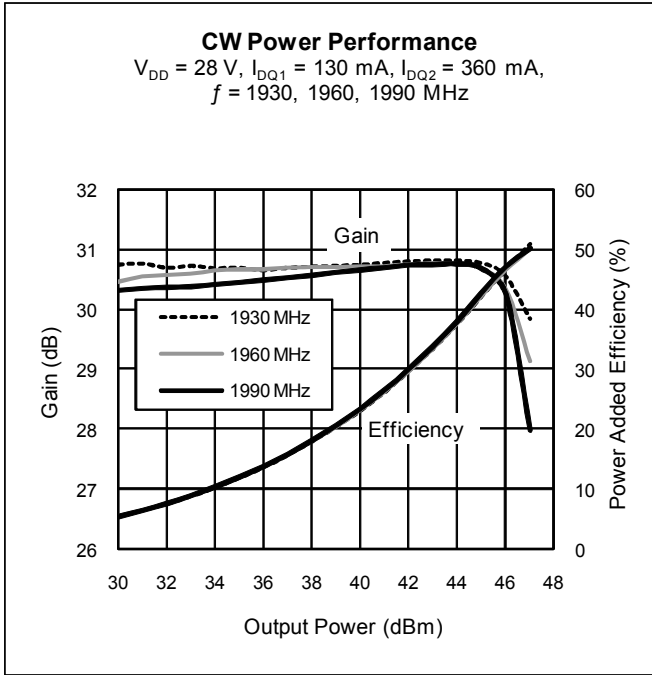


Assembly diagram for 2140 MHz reference circuit\* (not to scale)

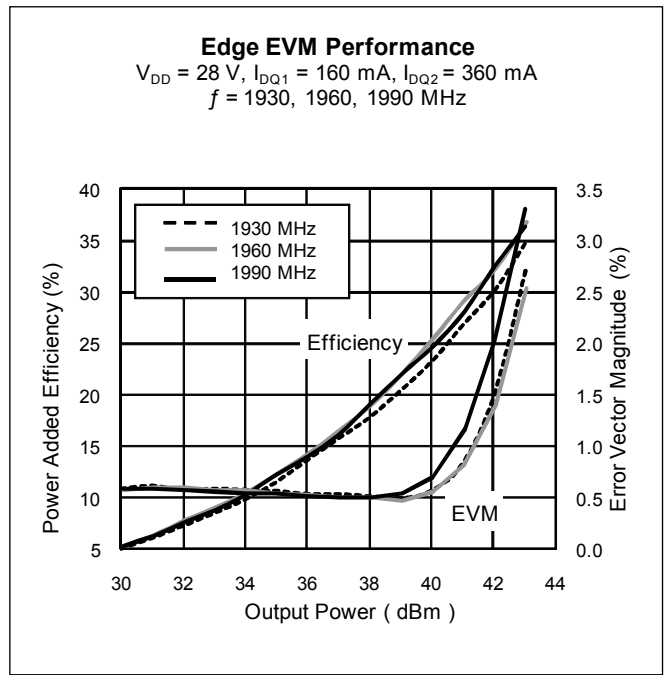
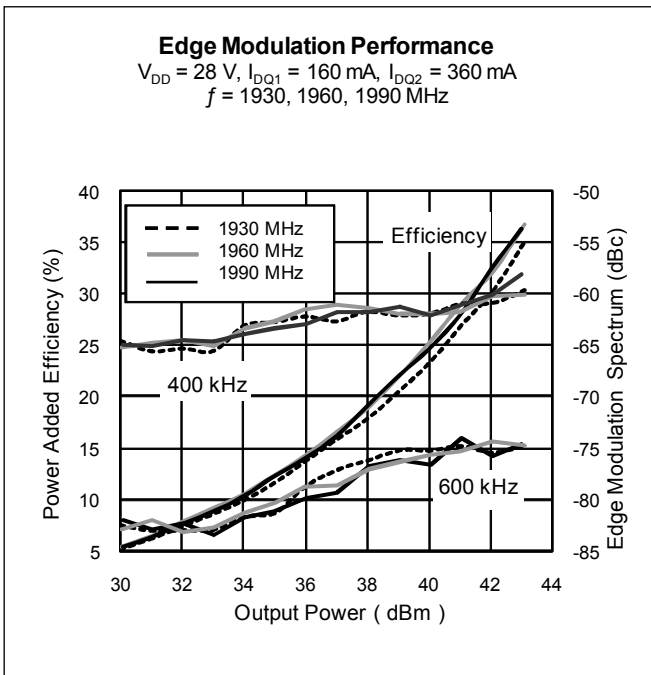
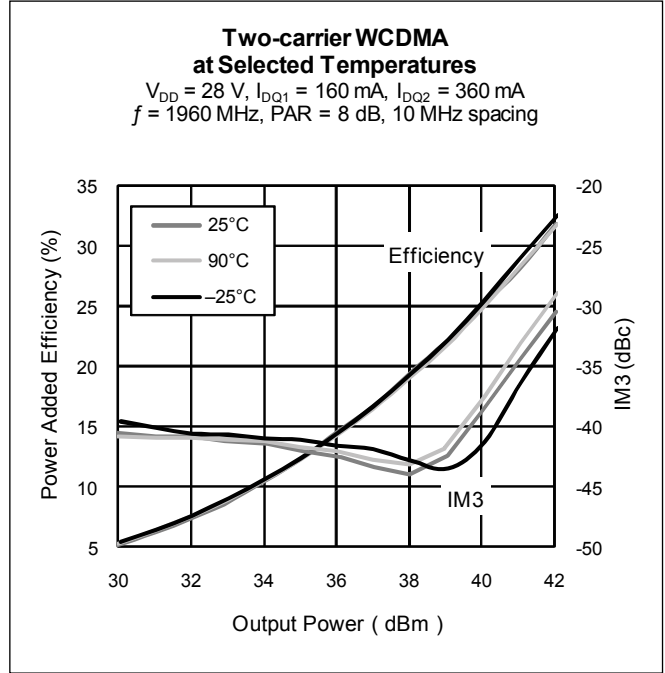
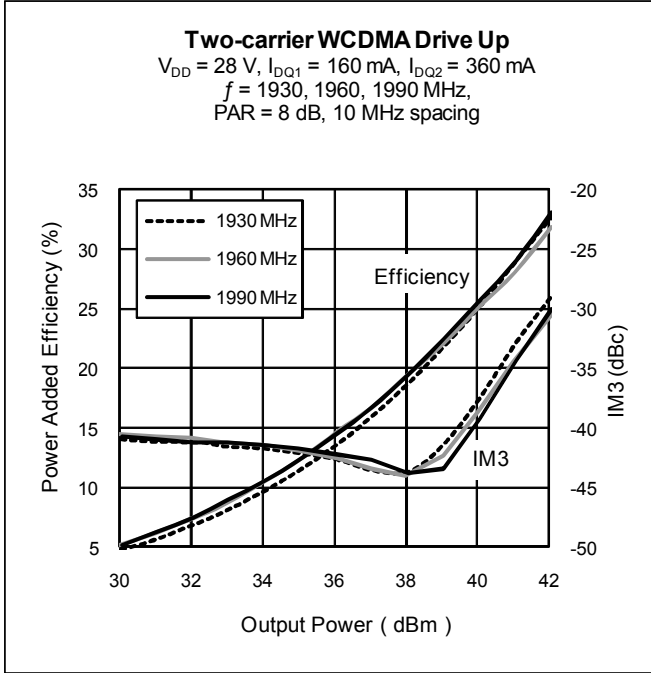
Component	Description	Suggested Manufacturer	P/N or Comment
C1, C19, C24, C29	Electrolytic capacitor, 100 $\mu$ F, 50 V	Digi-Key	PCE3718CT-ND
C2, C7, C11, C18, C23, C28	Ceramic capacitor, 10 $\mu$ F	Murata	GRM422Y5V106Z050AL
C3, C8, C12, C17, C22, C27	Ceramic capacitor, 1 $\mu$ F	Digi-Key	445-1411-2-ND
C4, C9, C13, C16, C21, C26	Capacitor, 0.1 $\mu$ F	Digi-Key	399-1267-2-ND
C5, C10, C12, C15, C20, C25, C34	Ceramic capacitor, 12 pF	ATC	600S120JT
C6	Ceramic capacitor, 0.5 pF	ATC	100B 0R5
C30, C31	Ceramic capacitor, 1.8 pF	ATC	600S1R8CT
C32	Ceramic capacitor, 2.4 pF	ATC	100B 2R4
C33	Ceramic capacitor, 1.2 pF	ATC	100B 1R2
Q1, Q2	Transistor	Infineon Technologies	BCP56
R1, R2	Resistor, 0 $\Omega$	Digi-Key	603
R3, R4	Potentiometer, 2k $\Omega$	Digi-Key	3224W-202ETR-ND

\*Gerber files for this circuit available on request

**Typical Performance, circuit tuned for 1960 MHz** (data taken in a production test fixture)



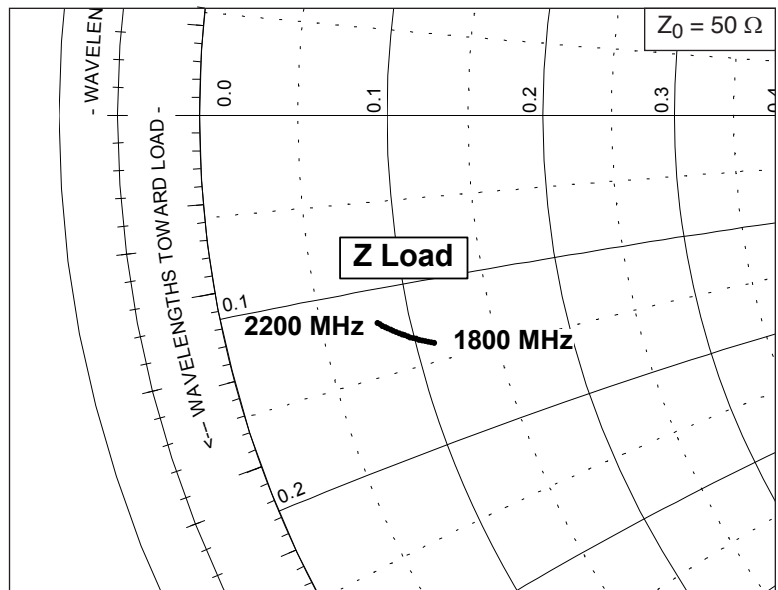
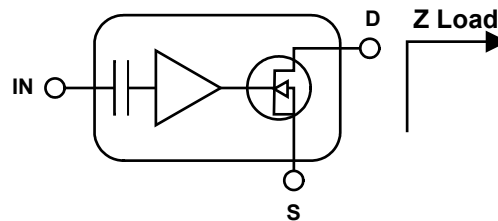
Typical Performance —1960 MHz (cont.)



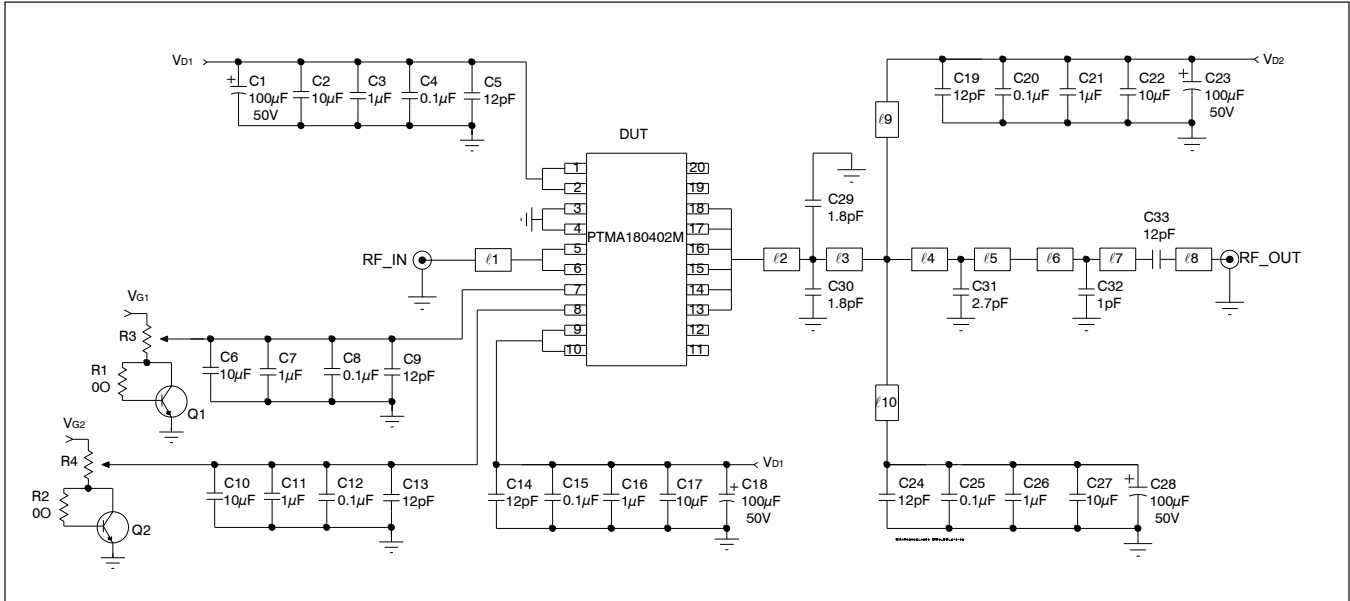


**Broadband Circuit Impedance — 1960 MHz**

Frequency MHz	Z Load $\Omega$	
	R	jX
1800	5.56	-6.95
1810	5.48	-6.91
1820	5.39	-6.87
1830	5.31	-6.83
1840	5.23	-6.79
1850	5.15	-6.75
1860	5.07	-6.70
1870	4.99	-6.66
1880	4.91	-6.61
1890	4.84	-6.56
1900	4.76	-6.51
1910	4.69	-6.47
1920	4.61	-6.42
1930	4.54	-6.36
1940	4.47	-6.31
1950	4.40	-6.26
1960	4.33	-6.21
1970	4.26	-6.15
1980	4.19	-6.10
1990	4.12	-6.04
2000	4.06	-5.99



Reference Circuit, tuned for 1960 MHz



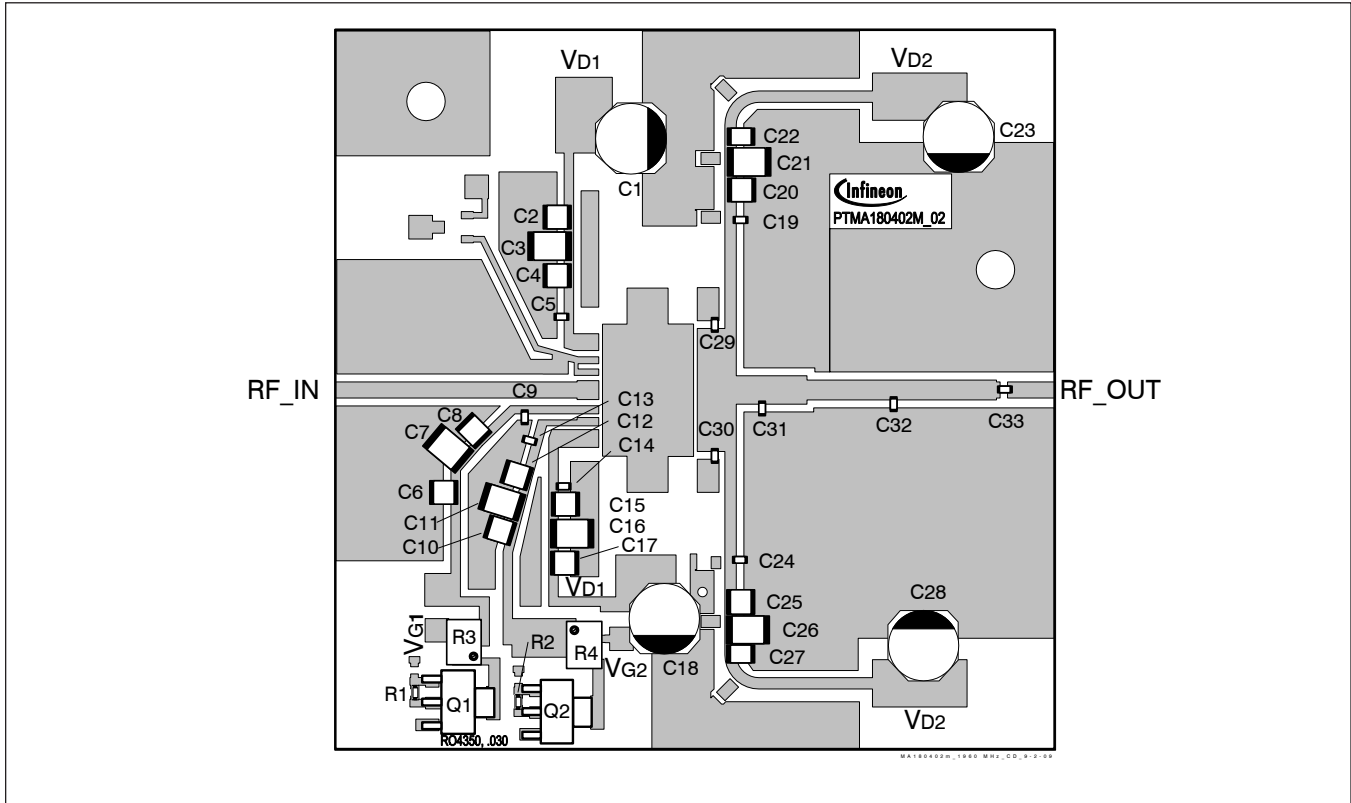
Reference circuit schematic for  $f = 1960$  MHz

Circuit Assembly Information

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PCB	LTN/PTMA180402M	Rogers RO4350: 0.76 mm [.030"] thick, $\epsilon_r = 3.48$ , 1 oz. copper

Microstrip	Electrical Characteristics at 1960 MHz	Dimensions: L x W (mm)	Dimensions: L x W (in.)
$\ell_1$	$0.300 \lambda, 50.0 \Omega$	27.76 x 1.70	1.093 x 0.067
$\ell_2$	$0.024 \lambda, 10.4 \Omega$	2.01 x 13.00	0.079 x 0.512
$\ell_3$	$0.024 \lambda, 10.4 \Omega$	2.06 x 13.00	0.081 x 0.512
$\ell_4$	$0.037 \lambda, 34.2 \Omega$	3.35 x 3.00	0.132 x 0.118
$\ell_5$	$0.046 \lambda, 34.2 \Omega$	4.11 x 3.00	0.162 x 0.118
$\ell_6$	$0.097 \lambda, 34.2 \Omega$	8.76 x 3.00	0.345 x 0.118
$\ell_7$	$0.127 \lambda, 43.6 \Omega$	11.63 x 2.11	0.458 x 0.083
$\ell_8$	$0.054 \lambda, 50.0 \Omega$	5.03 x 1.70	0.198 x 0.067
$\ell_9, \ell_{10}$	$0.125 \lambda, 47.8 \Omega$	11.56 x 1.83	0.455 x 0.072

Reference Circuit — 1960 MHz (cont.)

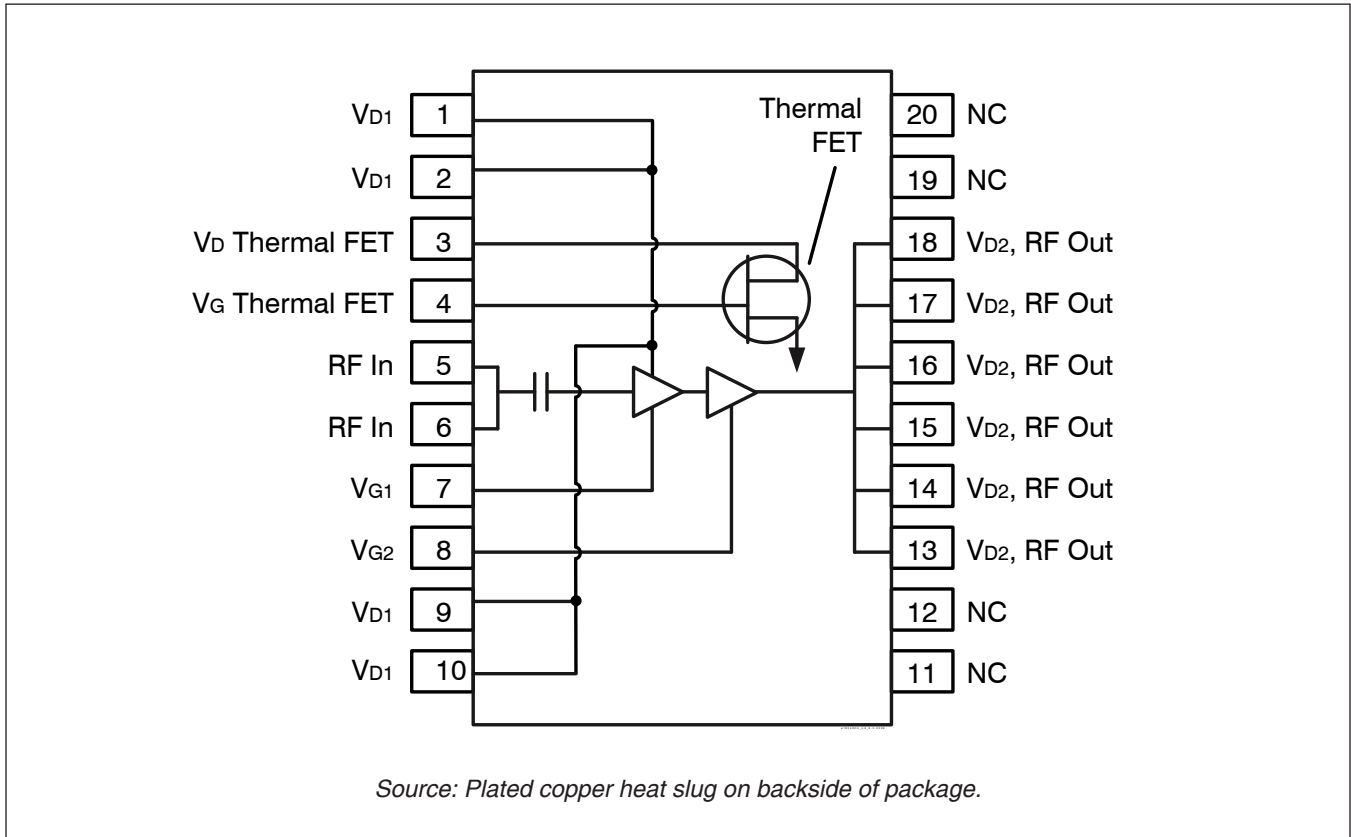


Assembly diagram for 1960 MHz reference circuit\* (not to scale)

Component	Description	Suggested Manufacturer	P/N or Comment
C1, C18, C23, C28	Electrolytic capacitor, 100 $\mu$ F, 50 V	Digi-Key	PCE3718CT-ND
C2, C6, C10, C17, C22, C27	Ceramic capacitor, 10 $\mu$ F	Murata	GRM422Y5V106Z050AL
C3, C7, C11, C16, C21, C26	Ceramic capacitor, 1 $\mu$ F	Digi-Key	445-1411-2-ND
C4, C8, C12, C15, C20, C25	Capacitor, 0.1 $\mu$ F	Digi-Key	399-1267-2-ND
C5, C9, C13, C14, C19, C24, C33	Ceramic capacitor, 12 pF	ATC	600S120JT
C29, C30, C31	Ceramic capacitor, 1.8 pF	ATC	600S1R8CT
C32	Ceramic capacitor, 1.0 pF	ATC	100B 1R0
Q1, Q2	Transistor	Infineon Technologies	BCP56
R1, R2	Resistor, 0 $\Omega$	Digi-Key	603
R3, R4	Potentiometer, 2k $\Omega$	Digi-Key	3224W-202ETR-ND

\*Gerber files for this circuit available on request

### Pinout Diagram



Package Outline Specifications

Package PG-DSO-20-63

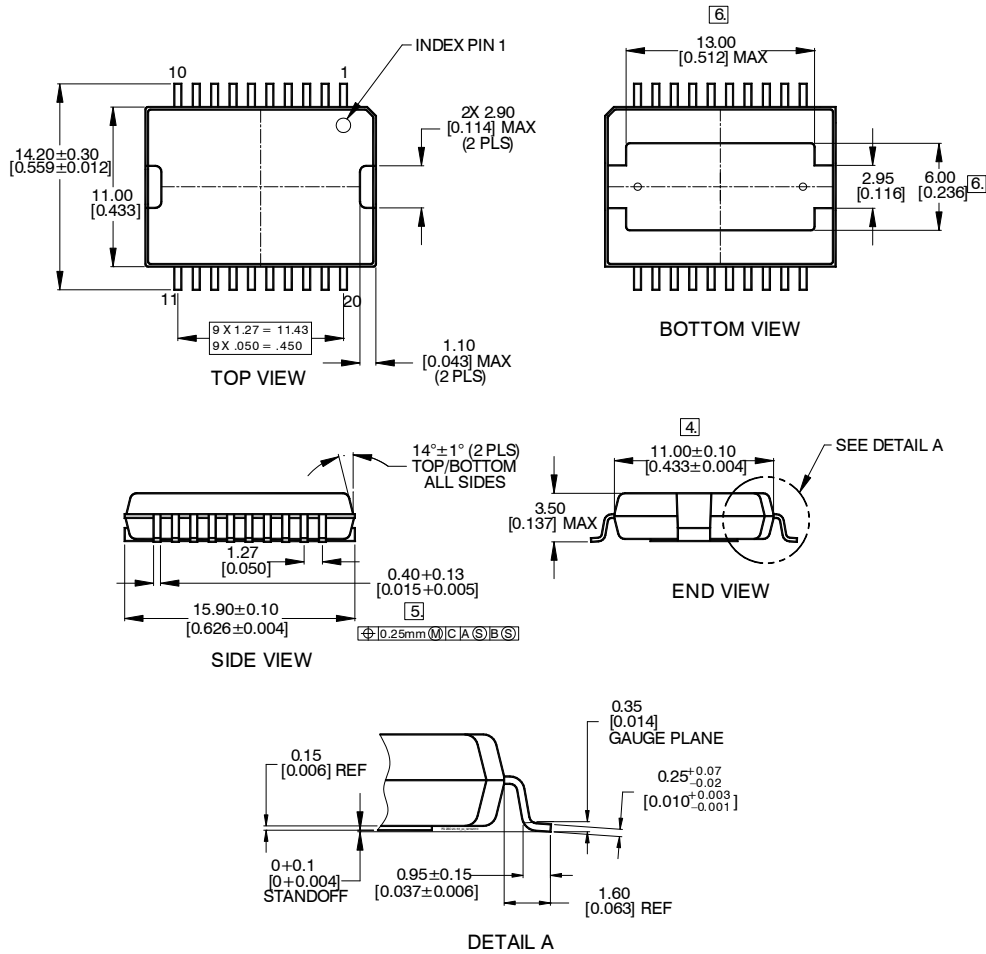


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Package dimensions: 11.0 mm by 15.9 mm by 3.35 mm.
3. JEDEC drawing number: MO-166.
- [4]. Does not include plastic or metal protrusion of 0.15 mm max per side.
- [5]. Does not include dambar protrusion; maximum allowable dambar protrusion shall be 0.08 mm.
- [6]. Bottom metallization.
7. Sn plating (matte) : 5 – 15 micron [196.85 – 590.55 microinch].

Find the latest and most complete information about products and packaging at the Infineon Internet page <http://www.infineon.com/rfpower>

Revision History: 2011-03-17

Data Sheet

Previous Version: none

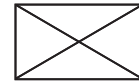
Page	Subjects (major changes since last revision)
3, 11	Corrected typo
9	Removed voltage vs. temperature graph

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