NEC

NEC Electronics Inc.

CMOS-4L 1.5-MICRON LOW-VOLTAGE CMOS GATE ARRAYS

February 1990

Description

NEC's CMOS-4L family of 1.5-micron gate arrays are high-density, low-voltage application-specific integrated circuits (ASICs) that offer unique solutions for battery-driven circuits. Supply voltages ranging from 1.0 V to 5.5 V make this family ideal for such applications as portable communications equipment and measuring instruments.

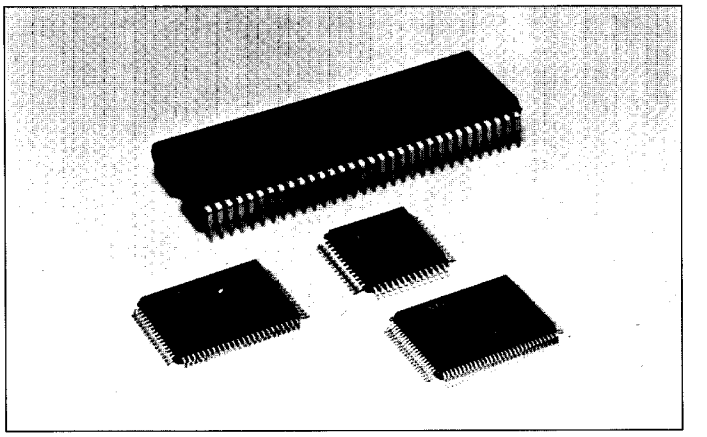
The CMOS-4L family combines NEC's proprietary circuit architecture and advanced 1.5-micron silicon-gate CMOS technology in gate array sizes from 800 to 5600 cells. A variety of package options is available.

Features

In addition to the advantages of low cost and high reliability, CMOS-4L gate arrays provide these features.

- Technology: 1.5-micron, silicon-gate CMOS; two-layer aluminum metallization
- Low power supply voltage: 1.0 to 5.5 V
- Low standby power consumption (typical): 0.01 μA (V_{DD} = 1.5 V)
- High speed
- Internal gate, 2-input NAND:
  2.2 ns (F/O = 3, L = 3 mm, V_{DD} = 5.0 V)
  10 ns (F/O = 3, L = 3 mm, V_{DD} = 1.5 V)
- High drive: I_{OL} = 3 mA (V_{DD} = 1.5 V)
- Ambient temperature: –10° to 85° C
- Block library with more than 120 macros
- Input buffers
  – CMOS
  – Schmitt
  – Oscillator/multivibrator interface
  – With pull-up or pull-down resistor
- Output buffers
  – Normal
  – Open-drain
  – Three-state
- Bidirectional buffers
- Packages
  – Plastic DIP: 40-pin, 64-pin
  – Plastic QFP: 24-pin to 120-pin
- Direct access to NEC Design Centers through communication network or telephone dial-up
- Quick turnaround time: 3 to 6 weeks

Figure 1. Sample CMOS-4L Packages



Publications

This data sheet contains specifications, package information, and operational data for CMOS-4L gate array devices. Additional design information is available in NEC's CMOS-4L Design Manual and CMOS-4L Block Library. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

Gate Array Sizes

μPD	Gates	Signal Pins (Max)
65007	858	62
65014	1656	82
65026	2457	100
65033	3360	106
65045	4320	120
65052	5632	138

Notes:

(1) Usable gate count is up to 95% of specified gate count.

(2) Actual pin count is determined by package size and type.

Figure 2. CMOS-4L Gate Array Layout

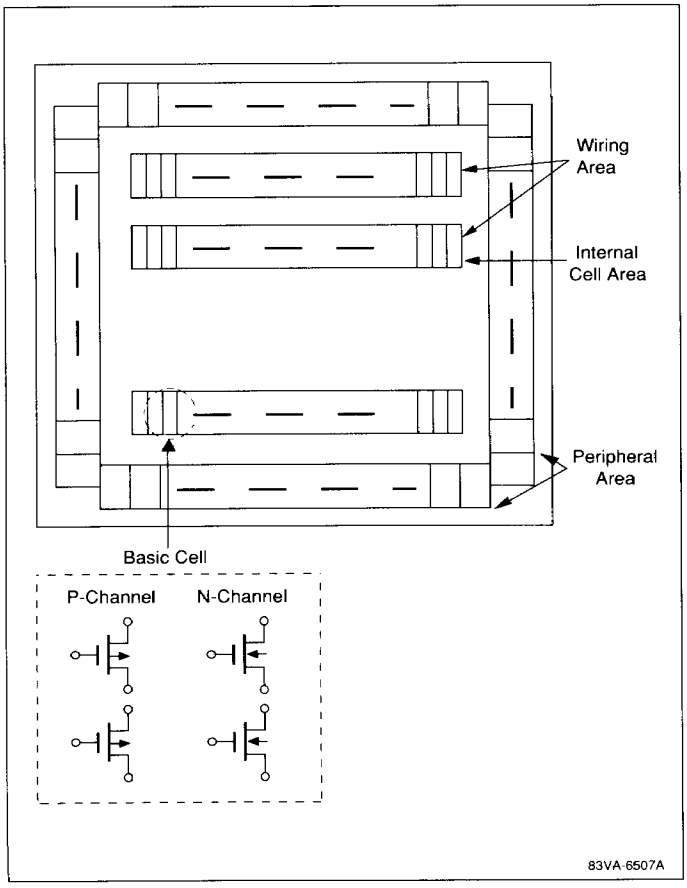
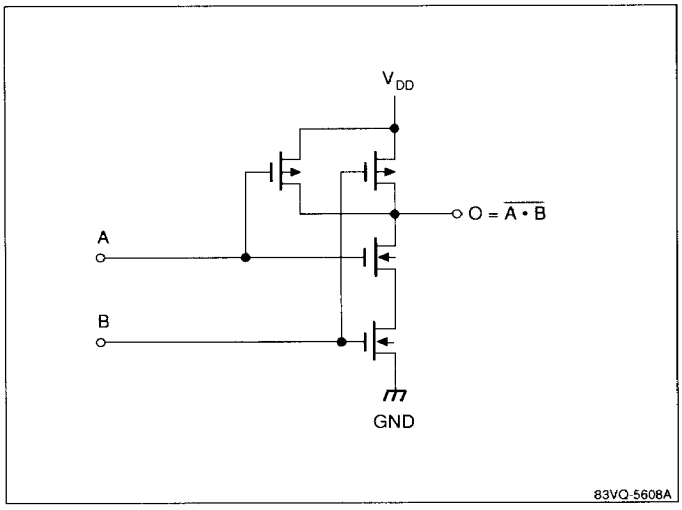


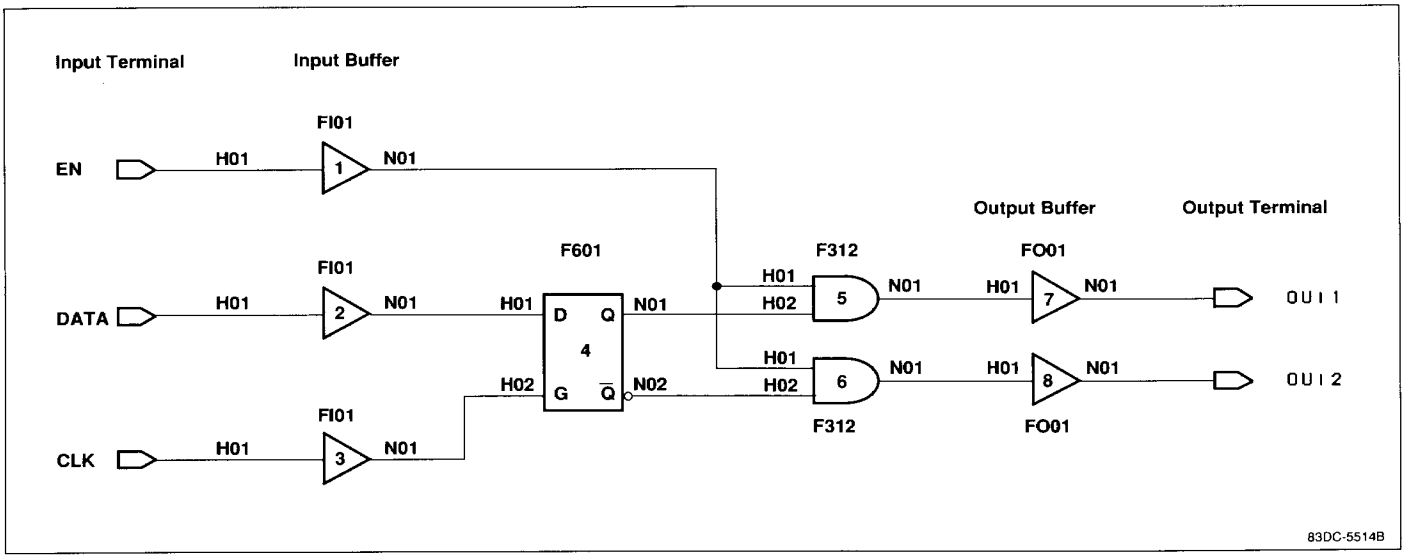
Figure 3. Cell Configured as a Two-Input NAND Gate



Circuit Architecture

CMOS-4L gate arrays are built with NEC's proven channeled architecture. As shown in figure 2, CMOS gate array chips are divided into peripheral and internal cell areas. The peripheral area contains input and output buffers that isolate the internal cells from high-energy external signals. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors. These p-channel and n-channel transistors are sized to offer a superb ratio of speed to silicon area.

Figure 4. Example of a Circuit Diagram



Recommended Operating Conditions

T_A = –10 to +85° C

Parameter	Symbol	Min	Max	Unit	Conditions
Power supply voltage	V_{DD}	1.0	5.5	V	CMOS level
Input voltage	V_I	0	V_{DD}	V	CMOS level
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	V	$V_{DD} \geq 2.0$ V
		0	0.2 V_{DD}	V	$V_{DD} < 2.0$ V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	V	$V_{DD} \geq 2.0$ V
		0.8 V_{DD}	V_{DD}	V	$V_{DD} < 2.0$ V
Input rise or fall time (Note 1)	t_R, t_F	0	300	ns	Normal input
Positive Schmitt-trigger voltage	V_P	0.35 V_{DD}	0.85 V_{DD}	V	$V_{DD} \geq 2.0$ V
Negative Schmitt-trigger voltage	V_N	0.15 V_{DD}	0.65 V_{DD}	V	$V_{DD} \geq 2.0$ V
Hysteresis voltage (Note 2)	V_H	0.2	1.8	V	$V_{DD} \geq 2.0$ V
Schmitt-trigger input rise or fall time (Note 1)	t_R, t_F	0	25	µs	

Notes:

(1) Does not apply to CLK, SET, or RESET signals.

(2) Hysteresis voltage is available only when $V_{DD} \geq 2.0$ V. V_H (min) can be determined as follows: V_H (min) = (V_{DD} – 1.5) x 0.4 V.

Input/Output Capacitance

Terminal	Symbol	Typ	Max	Unit	Conditions
Input	C_{IN}	10	20	pF	$V_{DD} = V_I = 0$ V;
Output	C_{OUT}	10	20	pF	f = 100 kHz
I/O	$C_{I/O}$	10	20	pF	

Absolute Maximum Ratings

T_A = +25°C

Power supply voltage, V_{DD}	–0.3 to +7.0 V
Input voltage, V_I	–0.3 V to V_{DD} + 0.3 V
Output current, I_O	20 mA
Operating temperature, T_{OPT}	–10 to +85° C
Storage temperature, T_{STG}	–65 to +150° C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the Recommended Operating Conditions.

AC Characteristics

T_A = 0 to +70° C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}			5	MHz	F/O = 1; V_{DD} = 1.5 V
Delay time, internal gate	t_{PD}		2.2		ns	F/O = 3; L = 3 mm; V_{DD} = 5.0 V
			10		ns	F/O = 3; L = 3 mm; V_{DD} = 1.5 V; T_A = 25° C
			88		ns	F/O = 3; L = 3 mm; V_{DD} = 1.0 V
Delay time, buffer						
Input	t_{PD}		12		ns	F/O = 3; L = 3 mm; V_{DD} = 1.5 V; T_A = 25° C
Output	t_{PD}		24		ns	C_L = 15 pF; V_{DD} = 1.5 V; T_A = 25° C

DC Characteristics

V_{DD}= 1.0 to 5.5 V; T_A= –10° to +85° C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Static current (Note 1)	I_L		0.01	80	µA	$V_I = V_{DD}$ or GND (Notes 2 and 3)
Input leakage current						
Normal input	I_I		10^{-4}	1	µA	$V_I = V_{DD}$ or GND
With pull-up	I_I	–0.01	–3	–200	µA	V_I = GND
With pull-down	I_I	0.01	3		µA	$V_I = V_{DD}$
Oscillator block	I_I		0.2		µA	$V_I = V_{DD}$ or GND
Dynamic current	I_{DD}		0.3		µA	Per cell per 100 kHz
Off-state output leakage current	I_{OZ}			1	µA	$V_O = V_{DD}$ or GND
Low-level output current	I_{OL}	0.8	3.0		mA	V_{OL} = 0.4 V; $V_{DD} \geq$ 1.2 V
	I_{OL}	0.18			mA	V_{OL} = 0.4 V; V_{DD} < 1.2 V
High-level output current	I_{OH}	–0.3	–1.0		mA	$V_{OH} = V_{DD}$ – 0.4 V; $V_{DD} \geq$ 1.2 V
	I_{OH}	–0.015			mA	$V_{OH} = V_{DD}$ – 0.4 V; V_{DD} < 1.2 V
Low-level output voltage	V_{OL}			0.1	V	I_{OL} = 0 mA
High-level output voltage	V_{OH}	V_{DD} –0.1			V	I_{OH} = 0 mA

Notes:

(1) Not applicable to designs using oscillators or to interface blocks with pull-up or pull-down resistors.

(2) Typical conditions: T_A = 25°C; V_{DD} = 1.5 V, except as noted under Conditions.

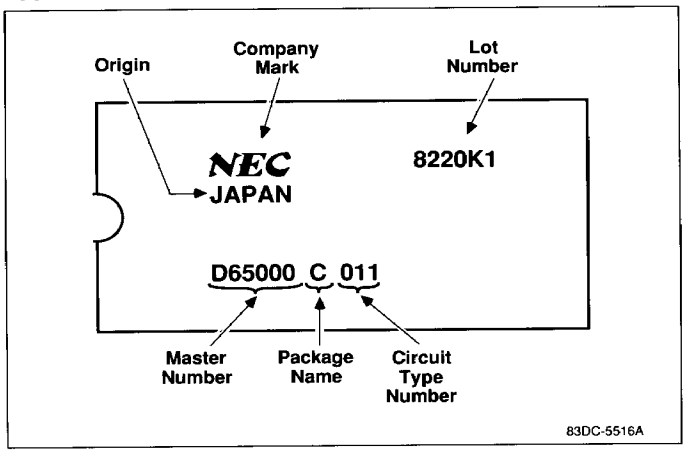
(3) Maximum conditions: T_A = 55°C; V_{DD} = 3.6 V.

Package Plan

	µPD65007	µPD65014	µPD65026	µPD65033	µPD65045	µPD65052
Plastic Shrink DIP (SDIP)						
40-pin	X	X	X			
64-pin	X	X	X	X	X	X
Small-Outline Package (SOP)						
24-pin	X	X	X			
Plastic Flatpack (QFP)						
44-pin	X	X	X			
52-pin	X	X	X	X		
64-pin	X	X	X	X	X	X
80-pin		X	X	X	X	X
100-pin			X	X	X	X
120-pin					X	X
136-pin						X
Thin Plastic Flatpack (TQFP)						
80-pin	X	X	X	X	X	X

Note: All packages may not be available. For current package availability, please contact your nearest NEC ASIC Design Center.

Typical Package Marking



NEC's ASIC Design System

CMOS-4L gate arrays are fully supported by NEC's network of ASIC Design Centers. (Design Centers are listed on the back of this data sheet.)

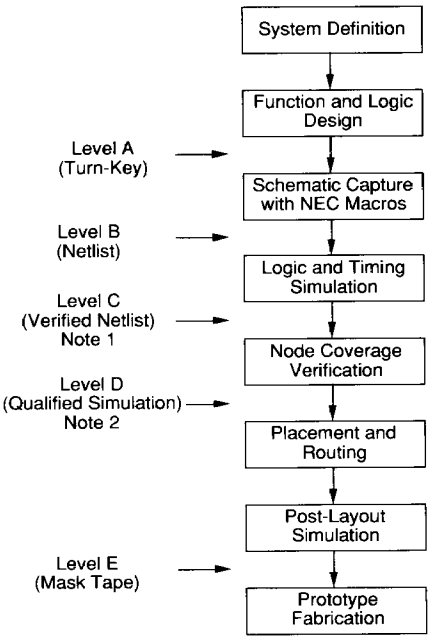
Design flow for CMOS-4L gate arrays is shown in figure 5. Users can enlist design center support at any step in the design flow before actual manufacturing. Figure 5 shows the various levels at which design center support may begin—anywhere from level A through level E. Level C, "Verified Netlist," is the most popular interface.

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semi-custom devices. NEC's OpenCAD™ integration system supports tools for floor-planning, logic synthesis, automatic test generation, accelerated fault grading and full timing simulation, and advanced place-and-route algorithms. These advanced CAD tools ensure accurate designs.

Sample design kits are available at no charge to qualified users: contact an NEC ASIC Design Center for more information. (Software licensing required—NEC reserves the right to prioritize support based on user requirements.)

OpenCAD is a trademark of NEC Electronics Inc.

Figure 5. CMOS–4L Gate Array Design Flow



Notes:

(1) NEC supports the most popular workstations, including Mentor Graphics, Valid, Daisy®, FutureNet, Viewlogic®, and HP9000 workstations, for the NEC ASIC product line. However, NEC does not support all workstations for all products. Please contact your nearest NEC ASIC Design Center for more information. (Daisy is a registered trademark of Daisy Systems Corp. Viewlogic is a registered trademark of Viewlogic Systems, Inc.)

(2) NEC provides support of System HILO®, Verilog®, and MACH 1000™ interface capability. (System HILO is a registered trademark of GenRad. Verilog is a registered trademark of Gateway Design Automation Corp. MACH 1000 is a trademark of Silicon Solutions/Zycad.)

83DC-5853A

Block Library List

Interface Blocks

Block Name	Description	Cells
Inputs		
FI01	Input buffer (CMOS level)	1
FIS1	Input buffer (CMOS-Schmitt level)	1
FID1	Input buffer (CMOS level), pull-down res.	1
FIU1	Input buffer (CMOS level), pull-up res.	1
FDS1	Input buffer (CMOS-Schmitt level), pull-down res.	1
FUS1	Input buffer (CMOS-Schmitt level), pull-up res.	1
Outputs		
B008	Output buffer (3-state)	1
FO01	Output buffer (normal), I_{OH}/I_{OL} = 0.015/0.18 mA	1

Interface Blocks (Cont.)

Block Name	Description	Cells
Open Drain Outputs		
EXT1	Output buffer (N-ch), I_{OL} = 0.18 mA	1
EXT2	Output buffer (P-ch), I_{OH} = 0.015 mA	1
EXT3	Output buffer (N-ch); pull-up res., I_{OL} = 0.18 mA	1
EXT4	Output buffer (P-ch); pull-down res., I_{OH} = 0.015 mA	1
Three-State I/Os		
B003	I/O buffer (CMOS level in)	1
BSI3	I/O buffer (CMOS-Schmitt level), I_{OH}/I_{OL} = 0.015/0.18 mA	1
B0D3	I/O buffer (CMOS level); pull-down res., I_{OH}/I_{OL} = 0.015/0.18 mA	1
B0U3	I/O buffer (CMOS level); pull-up res., I_{OH}/I_{OL} = 0.015/0.18 mA	1
BSD3	I/O buffer (CMOS-Schmitt level); pull-down res., I_{OH}/I_{OL} = 0.015/0.18 mA	1
BSU3	I/O buffer (CMOS-Schmitt level); pull-up res., I_{OH}/I_{OL} = 0.015/0.18 mA	1
Three-State Outputs		
B0D8	Output buffer, pull-down res., I_{OH}/I_{OL} = 0.015/0.18 mA	1
B0U8	Output buffer, pull-up res., I_{OH}/I_{OL} = 0.015/0.18 mA	1
Oscillators (Note 1)		
OSI1	Oscillator input buffer	1
OSO1	Oscillator output buffer	1
OSO3	Oscillator output buffer	1
Others (Note 1)		
OSF1	Feedback resistance for oscillator	1
SHT1	Monostable multivibrator	1
Inverters		
F101	Inverter, 1-in (F/O = 10)	1
F102	Inverting buffer, 1-in (F/O = 20)	1
F103	Inverting buffer, 1-in (F/O = 30)	2
F104	Inverting buffer, 1-in (F/O = 40)	2

Note:

(1) More than one oscillator pin must be used in combination. Some valid combinations are:

OSI1 + OSO1
OSI1 + OSO3 + OSF1

Function Blocks

Block Name	Description	Cells
Buffers		
F111	Non-inverting buffer, 1-in (F/O = 10)	1
F112	Non-inverting buffer, 1-in (F/O = 20)	2
F113	Non-inverting buffer, 1-in (F/O = 30)	2
F114	Non-inverting buffer, 1-in (F/O = 40)	3
F116	Non-inverting buffer, 1-in (F/O = 64)	5
NOR Gates		
F202	2-Input NOR	1
F203	3-Input NOR	2
F208	8-Input NOR	7
OR Gates		
F212	2-Input OR	2
F213	3-Input OR	2
NAND Gates		
F302	2-Input NAND	1
F303	3-Input NAND	2
F304	4-Input NAND	2
F308	8-Input NAND	7
AND Gates		
F312	2-Input AND	2
F313	3-Input AND	2
F314	4-Input AND	3
AND-NOR Gates		
F421	2-Wide, 1-2-input AND-OR inverter	2
F422	3-Wide, 1-1-2-input AND-OR inverter	2
F423	2-Wide, 1-3-input AND-OR inverter	2
F424	2-Wide, 2-2-input AND-OR inverter	2
F425	3-Wide, 2-2-2-input AND-OR inverter	3
F426	2-Wide, 3-3-input AND-OR inverter	3
F442	2-Wide, 4-4-input AND-OR inverter	4
OR-NAND Gates		
F431	2-Wide, 1-2-input OR-AND inverter	2
F432	3-Wide, 1-1-2-input OR-AND inverter	2
F433	2-Wide, 1-3-input OR-AND inverter	2
F434	2-Wide, 2-2-input OR-AND inverter	2
F435	2-Wide, 2-3-input OR-AND inverter	3
F436	2-Wide, 3-3-input OR-AND inverter	3
F454	4-Wide, 2-2-2-2-input OR-AND inverter	4

Function Blocks (Cont.)

Block Name	Description	Cells
Drivers		
F501	Clock driver	1
F502	Dual clock driver	2
Exclusive-OR, Exclusive-NOR Gates		
F511	EX-OR	3
F512	EX-NOR	3
Full Adders		
F521	Full adder	7
F523	4-Bit binary full adder	30
Three-State Buffers		
F531	Buffer with Enable	3
F532	Buffer with Enable	3
Decoders		
F561	2-to-4 Decoder	6
F981	2-to-4 Decoder with Enable	9
F982	3-to-8 Decoder with Enable	20
Multiplexers		
F569	8-1 Multiplexer	17
F570	4-1 Multiplexer	8
F571	2-1 Multiplexer	11
F572	Quad 2-1 Multiplexer	
Parity Generators		
F581	8-Bit odd	18
F582	8-Bit even	18
Latches		
F595	R-S latch	4
F601	D latch	3
F602	D latch with Reset	4
F603	D latch with Reset	4
F604	D latch with G driver	3
F605	D latch with G driver, Reset	4
F901	4-Bit latch	10
F902	8-Bit latch	18
Flip-Flops		
F596	Synchronous R-S F/F with Set-Reset	9
F611	D F/F	5

Function Blocks (Cont.)

Block Name	Description	Cells
Flip-Flops (Cont.)		
F614	D F/F with Set-Reset	7
F617	D F/F with Set-Reset	7
F631	D F/F with C	5
F637	D F/F with C, Set-Reset	5
F641	D F/F, buffered out	6
F644	D F/F with Set-Reset; buffered out	8
F647	D F/F with Set-Reset; buffered out	8
F661	D F/F with C; buffered out	6
F667	D F/F with C, Set-Reset; buffered out	8
F922	4-Bit D F/F with Reset	22
F924	4-Bit D F/F	17
Shift Registers		
F911	4-Bit register with Reset	22
F912	4-Bit serial/parallel register	24
F913	4-Bit parallel-in register with Reset	31
F914	4-Bit register	17
Toggle Flip-Flops		
F714	Toggle with Set-Reset	7
F717	Toggle with Set-Reset	7
F737	Toggle with Set-Reset	7
F744	Toggle with Set-Reset; buffered out	8
F747	Toggle with Set-Reset; buffered out	8
F767	Toggle with Set-Reset; buffered out	8
F791	Toggle with Set-Reset Toggle Enable	9
F792	Toggle with Set-Reset Toggle Enable	9
J-K Flip-Flops		
F771	F/F, buffered out	9
F774	F/F with Set-Reset; buffered out	11
F777	F/F with Set-Reset; buffered out	11
F781	F/F with C, buffered out	9
F787	F/F with C; Set-Reset, buffered out	11
Counters		
F962	4-Bit synchronous binary up, with Reset; buffered out	34
Special		
BUSA	Bus array	0
F091	H, L level generator	1
F093	Interface block for oscillator buffer	1

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