REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18															
REV STATUS				REV															
OF SHEETS				SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

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DRAWING APPROVAL DATE
01-08-08

REVISION LEVEL

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, ASIC, MULTI CHANNELS IEEE 1355 COMMUNICATION CONTROLLER, MONOLITHIC SILICON

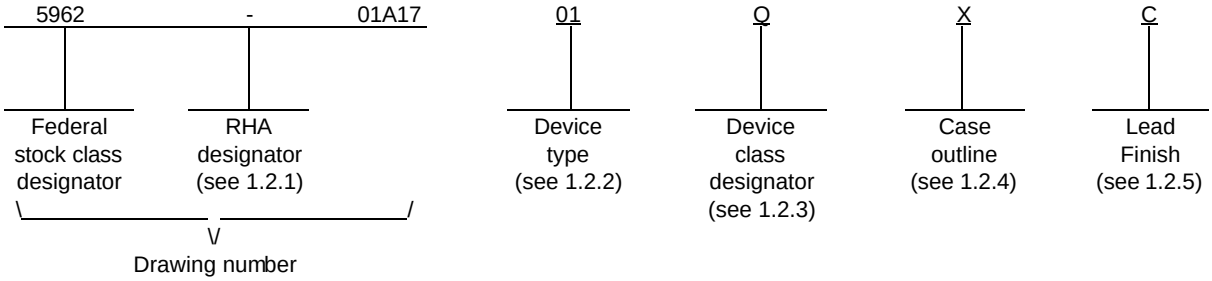
SIZE	CAGE CODE	
A	**67268**	**5962-01A17**

SHEET 1 OF 18

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TSS901E	Scaleable Multi Channels Subsystems SMCS332

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	196	Flat pack gull wing leads

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD}) ..... -0.5 V to 7.0 V
Input voltage range (V_{IN}) ..... -0.5 V to V_{DD} +0.5 V 3/
Input current (I_{IN})
Signal pin ..... -10.0 mA to 10.0 mA
Power pin ..... -50.0 mA to 50.0 mA
Output short circuit current 4/
V_{OUT} = V_{DD} ..... 110 mA
V_{OUT} = V_{SS} ..... -90 mA
Lead temperature (soldering, 10 sec) ..... +300°C
Storage temperature range ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{DD})..... 4.5 V to 5.5 V
Case temperature (T_C)..... -55°C to 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to ground unless otherwise specified.
3/ V_{DD} + 0.5 V shall not exceed 7.0 V
4/ The maximum output current of any single output in a shorted condition for a maximum duration of 1 second.
5/ Duration 10 second maximum at a distance not less than 1.6 mm

2.2 Non Government Publications. The following document(s) form a part of this document to the extent specified herin. Unless otherwise specified, the issues of the documents(s) which are DOD adopted are those listed in the DODISS cited in the solicitation

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1355 - IEEE Standard for Heterogeneous Interconnect (HIC) (Low-cost, Low Latency Scalable Serial Interconnect for Parallel System Construction)

(Applications for copies should be addressed to the Institute of Electrical and Electronic Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall test patterns defined and controlled in Atmel Nantes Device-spec. TSS901E which have been developed from customer provided vectors and simulations specific to this device.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device classes M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ V_{DD} = 5.0 V ± 10% unless otherwise specified	Group A Subgroups	Limits		Units
				Min.	Max.	
Input clamp voltage to GND 1/	V_{IC}	I_{OH} = -300 µA	1,2,3	-1.2	-0.2	V
Low level input current 2/	I_{IL}	V_{IN} = GND, V_{DD} = 5.5 V	1,2,3	-10		µA
Low level input current, pull-up 2/	I_{ILPU}	V_{IN} = GND, V_{DD} = 5.5 V	1,2,3	-250		µA
Low level input current, pull-down 2/	I_{ILPD}	V_{IN} = GND, V_{DD} = 5.5 V	1,2,3	-10		µA
High level input current 2/	I_{IH}	V_{IN} = V_{DD} = 5.5 V	1,2,3		10	µA
High level input current, pull-up 2/	I_{IHPU}	V_{IN} = V_{DD} = 5.5 V	1,2,3		10	µA
High level input current, pull-down 2/	I_{IHPD}	V_{IN} = V_{DD} = 5.5 V	1,2,3		450	µA
Output leakage low current 2/	I_{OZL}	Outputs disabled, V_{OUT} = V_{DD}	1,2,3	-10		µA
Output leakage high current, pull-down output 2/	I_{OZHPD}	Outputs disabled, V_{OUT} = V_{DD}	1,2,3		450	µA
Output leakage low current, pull-up output 2/	I_{OZLPU}	Outputs disabled, V_{OUT} = V_{DD}	1,2,3	250		µA
Output leakage high current 2/	I_{OZH}	Outputs disabled, V_{OUT} = V_{DD}	1,2,3		10	µA
Low level output voltage, BUF 2/	V_{OL1}	V_{DD} = 5.5 V, I_{OL} = 3 mA	1,2,3		0.4	V
Low level output voltage, BUF 2/	V_{OL2}	V_{DD} = 5.5 V, I_{OL} = 6 mA	1,2,3		0.4	V
Low level output voltage, BUF 2/	V_{OL3}	V_{DD} = 5.5 V, I_{OL} = 12 mA	1,2,3		0.4	V
High level output voltage, BUF 2/	V_{OH1}	V_{DD} = 4.5 V, I_{OL} = -3 mA	1,2,3	3.9		V
High level output voltage, BUF 2/	V_{OH2}	V_{DD} = 4.5 V, I_{OL} = -6 mA	1,2,3	3.9		V
High level output voltage, BUF 2/	V_{OH3}	V_{DD} = 4.5 V, I_{OL} = -12 mA	1,2,3	3.9		V
Schmitt trigger positive threshold 3/	V_{T+}		1,2,3			
CMOS input					2.2	V
TTL input					1.4	
Schmitt trigger negative threshold 3/	V_{T-}		1,2,3			
CMOS input				0.9		V
TTL input				0.9		
Low level input voltage 1/	V_{IL}	Functional verification	1,2,3		0.8	V
High level input voltage 1/	V_{IH}	Functional verification	1,2,3	2.2		V
Input capacitance 3/	C_I	V_{DD} = 0 V	4		15	PF
Output capacitance 3/	C_{IO}	V_{DD} = 0 V	4		15	pF

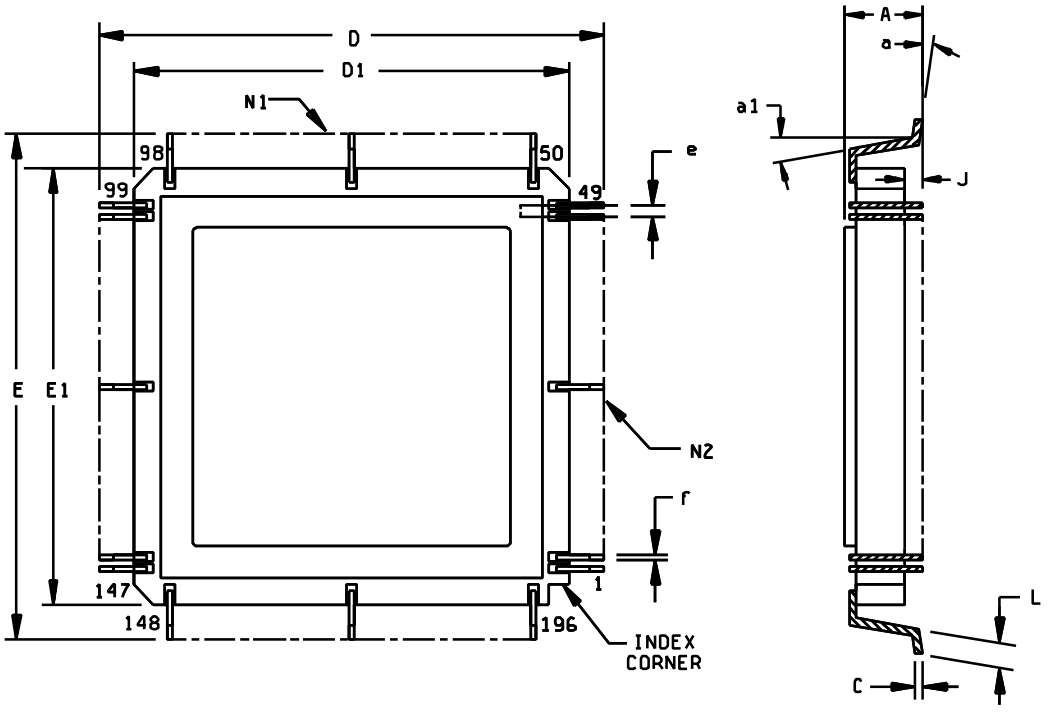
See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le 125°C$ V_{DD} = 5.0 V ±10% unless otherwise specified	Group A Subgroups	Limits		Units
				Min.	Max.	
Supply current standby for array 2/	I_{DDSBA}	V_{DD} = 5.5 V, Static mode Output = 0 mA	1,2,3		100	µA
Supply current standby operating for array 2/	I_{DDOPA}	V_{DD} = 5.5 V, F = 10 MHz Output = 0 mA	1,2,3		20	mA
Supply current standby operating for buffers 2/	I_{DDOPB}	V_{DD} = 5.5 V,F = 10 MHz Output = 0 mA	1,2,3		20	mA
Propagation delay CLK / to HACK /	D_{T1}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns
Propagation delay CLK \ to HINTR \	D_{T2}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		49	ns
Propagation delay CLK \ to HDATA0 /	D_{T3}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		45	ns
Propagation delay CLK \ to HDATA7 /	D_{T4}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		45	ns
Propagation delay CLK / to CPUR \	D_{T5}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		35	ns
Propagation delay CLK / to COCO /	D_{T6}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		40	ns
Propagation delay CLK / to CMCS0 \	D_{T7}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		22	ns
Propagation delay CLK/ to CMADR0 /	D_{T8}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		28	ns
Propagation delay CLK / to CMDATA0 /	D_{T9}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		46	ns
Propagation delay CLK10 / to IDO1 /	D_{T10}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns
Propagation delay CLK10 / to ISO1 \	D_{T11}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns
Propagation delay CLK10 / to IDO2 /	D_{T12}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns
Propagation delay CLK10 / to ISO2 /	D_{T13}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns
Propagation delay CLK10 / to IDO3 /	D_{T14}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns
Propagation delay CLK10 / to ISO3 \	D_{T15}	V_{DD} = 4.5 V, V_{DD} = 5.5 V	9,10,11		27	ns

1/ Forcing conditions of the functional test, assure that these limits are met, but they will not be recorded.
2/ Read and record measurements in accordance with MIL-PRF-38535.
3/ Tested at initial design and after major process changes, otherwise guaranteed.

CASE X



	MM		INCH	
	Min	Max	Min	Max
A	-	2.95	-	.116
C	0.20 TYP		.008 TYP	
D	-	39.75	-	1.565
D1	-	34.54	-	1 360
E	-	39.75	-	1.565
E1	-	34.54	-	1 360
e	0.635 BSC		.025 BSC	
f	0.28 REF		.011 REF	
J	0.15	0.30	.006	012
L	0.61	1.01	.024	040
N1	49		49	
N2	49		49	
	a=4°~ 4°		a1=5°~ 5°	

Figure 1. Case Outline

Pin Number	Pin Type	Pin Name	Output Load	Wired To	Comment
	VSS	PLL_XXXVEE1			Analog power supply
1	VDD	PLL_XXXVCCHF			Digital power supply
2	VSS	PLL_XXXVEEHF			Digital power supply
3	I / PD	BYPPLL		V_{CC}	
4	I / PU	CLK		S1	
5	I	RESET		V_{CC}	
6	I / PU	CLK10		S1	
7	I / PD	HOSTBIGE		S5	
8	I / PU	TCK		S1	
9	I / PU	TMS		V_{CC}	
10	I / PU	TDI		V_{CC}	
11	I / PD	TRST		GND	
12	O/Z	TDO	R		
13	VDB	VCCB0		V_{CC}	
14	VSB	VSSB0		GND	
15	I / PU	HSEL		S3	
16	I / PU	HRD		S3	
17	I / PU	HWR		V_{CC}	
18	O/Z	HACK	R		
19	O/Z	HINTR	R		
20	VDA	VCCA0		V_{CC}	
21	VSA	VSSA0		GND	
22	I / PU	HADR0		S4	
23	I / PU	HADR1		S5	
24	I / PU	HADR		S6	
25	I / PU	HADR3		S7	
26	I / PU	HADR4		S8	
27	I / PU	HADR5		S9	
28	I / PU	HADR6		S10	
29	I / PU	HADR7		S10	
30	VDA	VCCA1		V_{CC}	
31	VSA	VSSA1		GND	
32	I / PU	BOOTLINK		GND	
33	I / PU	SMCSADR0		S10	
34	I / PU	SMCSADR1		S10	
35	I / PU	SMCSADR		S10	
36	I / PU	SMCSADR3		S10	
37	I / PU	SMCSID0		S10	
38	I / PU	SMCSID1		S10	
39	I / PU	SMCSID2		S10	

Figure 2. Terminal connections and electrical circuit for power burn-in.

Pin Number	Pin Type	Pin Name	Output Load	Wired To	Comment
40	I / PU	SMCSID3		S10	
41	VDB	VCCB1		V_{CC}	
42	VSB	VSSB1		GND	
43	I/O / PU	HDATA0	R		
44	I/O / PU	HDATA1	R		
45	I/O / PU	HDATA2	R		
46	I/O / PU	HDATA3	R		
47	I/O / PU	HDATA4	R		
48	I/O / PU	HDATA5	R		
49	I/O / PU	HDATA6	R		
50	VDB	VCCB2		V_{CC}	
51	VSB	VSSB2		GND	
52	I/O / PU	HDATA7	R		
53	I/O / PU	HDATA8	R		
54	I/O / PU	HDATA9	R		
55	I/O / PU	HDATA10	R		
56	I/O / PU	HDATA11	R		
57	VDB	VCCB3		V_{CC}	
58	VSB	VSSB3		GND	
59	I/O / PU	HDATA12	R		
60	I/O / PU	HDATA13	R		
61	I/O / PU	HDATA14	R		
62	I/O / PU	HDATA15	R		
63	I/O / PU	HDATA16	R		
64	I/O / PU	HDATA17	R		
65	VDB	VCCB4		V_{CC}	
66	VSB	VSSB4		GND	
67	I/O / PU	HDATA18	R		
68	I/O / PU	HDATA19	R		
69	I/O / PU	HDATA20	R		
70	I/O / PU	HDATA21	R		
71	I/O / PU	HDATA22	R		
72	I/O / PU	HDATA23	R		
73	VDB	VCCB5		V_{CC}	
74	VSB	VSSB5		GND	
75	I/O / PU	HDATA24	R		
76	I/O / PU	HDATA25	R		
77	I/O / PU	HDATA26	R		
78	VDA	VCCA2		V_{CC}	
79	VSA	VSSA2		GND	

Figure 2. Terminal connections and electrical circuit for power burn-in – Continued.

Pin Number	Pin Type	Pin Name	Output Load	Wired To	Comment
80	I/O / PU	HDATA27	R		
81	I/O / PU	HDATA28	R		
82	I/O / PU	HDATA29	R		
83	VDB	VVCB6		V_{CC}	
84	VSB	VSSB6		GND	
85	I/O / PU	HDATA30	R		
86	I/O / PU	HDATA31	R		
87	O/Z	CPUR	R		
88	O/Z	SES0	R		
89	O/Z	SES1	R		
90	O/Z	SES2	R		
91	O/Z	SES3	R		
92	I / PU	CAM		V_{CC}	
93	I / PU	COCI		GND	
94	O/Z	COCO	R		
95	O/Z	CMCS0	R		
96	O/Z	CMCS1	R		
97	VDB	VCCB7		V_{CC}	
98	VSB	VSSB7		GND	
99	O/Z	CMRD	R		
100	O/Z	CMWR	R		
101	O/Z	CMADR0	R		
102	O/Z	CMADR1	R		
103	O/Z	CMADR2	R		
104	O/Z	CMADR3	R		
105	O/Z	CMADR4	R		
106 107	VDB VSB	VCCB8 VSSB8		V_{CC} GND	
108	O/Z	CMADR5	R		
109	O/Z	CMADR6	R		
110	O/Z	CMADR7	R		
111	O/Z	CMADR8	R		
112	O/Z	CMADR9	R		
113	O/Z	CMADR10	R		
114	O/Z	CMADR11	R		
115	VDB	VCCB9		V_{CC}	
116	VSB	VSSB9		GND	
117	O/Z	CMADR12	R		
118	O/Z	CMADR13	R		
119	O/Z	CMADR14	R		

Figure 2. Terminal connections and electrical circuit for power burn-in – Continued.

Pin Number	Pin Type	Pin Name	Output Load	Wired To	Comment
120	O/Z	CMADR15	R		
121	I/O / PU	CMDATA0	R		
122	I/O / PU	CMDATA1	R		
123	I/O / PU	CMDATA2	R		
124	VDB	VCCB10		V_{CC}	
125	VSB	VSSB10		GND	
126	I/O / PU	CMDATA3	R		
127	I/O / PU	CMDATA4	R		
128	I/O / PU	CMDATA5	R		
129	VDA	VCCA3		V_{CC}	
130	VSA	VSSA3		GND	
131	I/O / PU	CMDATA6	R		
132	I/O / PU	CMDATA7	R		
133	I/O / PU	CMDATA8	R		
134	VDB	VCCB11		V_{CC}	
135	VSB	VSSB11		GND	
136	I/O / PU	CMDATA9	R		
137	I/O / PU	CMDATA10	R		
138	I/O / PU	CMDATA11	R		
139	I/O / PU	CMDATA12	R		
140	I/O / PU	CMDATA13	R		
141	I/O / PU	CMDATA14	R		
142	VDB	VDB		V_{CC}	
143	VSB	VSB		GND	
144	I/O / PU	CMDATA15	R		
145	I/O / PU	CMDATA16	R		
146	I/O / PU	CMDATA17	R		
147	I/O / PU	CMDATA18	R		
148	I/O / PU	CMDATA19	R		
149	I/O / PU	CMDATA20	R		
150	VDB	VCCB13		V_{CC}	
151	VSB	VSSB13		GND	
152	I/O / PU	CMDATA21	R		
153	I/O / PU	CMDATA22	R		
154	I/O / PU	CMDATA23	R		
155	VDA	VCCA4		V_{CC}	
156	VSA	VSSA4		GND	
157	I/O / PU	CMDATA24	R		
158	I/O / PU	CMDATA25	R		
159	I/O / PU	CMDATA26	R		

Figure 2. Terminal connections and electrical circuit for power burn-in – Continued.

Pin Number	Pin Type	Pin Name	Output Load	Wired To	Comment
160	VDB	VCCB14		V_{CC}	
161	VSB	VSSB14		GND	
162	I/O / PU	CMDATA27	R		
163	I/O / PU	CMDATA28	R		
164	I/O / PU	CMDATA29	R		
165	I/O / PU	CMDATA30	R		
166	I/O / PU	CMDATA31	R		
167	I / PD	SCANDE	GND		
168	I	SCNCLK	GND		
169					
170	I / PD	SCAN_SET	GND		
171	I / PD	SCANCE	GND		
172	VDB	VDB		V_{CC}	
173	VSB	VSB		GND	
174	VSB	VSB		GND	
175	O/Z	LEN1	R		
176	I / PD	LDI1		S1	
177	I / PD	LSI1		S2	
178	O/Z	LDO1	R		
179	O/Z	LSO1	R		
180	I / PD	LDI2		S1	
181	I / PD	LSI2		S2	
182	O/Z	LEN2	R		
183	VDB	VCCBQ1		V_{CC}	
184	VDB	VCCBQ2		V_{CC}	
185	VDB	VCCBN2		V_{CC}	
186	O/Z	LDO2	R		
187	O/Z	LSO2	R		
188	I / PD	LDI3		S1	
189	I / PD	LSI3		S2	
190	O/Z	LDO3	R		
191	O/Z	LSO3	R		
192	O/Z	LEN3	R		
193	VSB	VSSBQ2		GND	
194	VSS	PLL_XXXVEE2			Analog Power Supply
195	VDD	PLL_XXXVCC			Analog Power Supply
196		PLL_XXXOUTF			External Filter Connection

Figure 2. Terminal connections and electrical circuit for power burn-in – Continued.

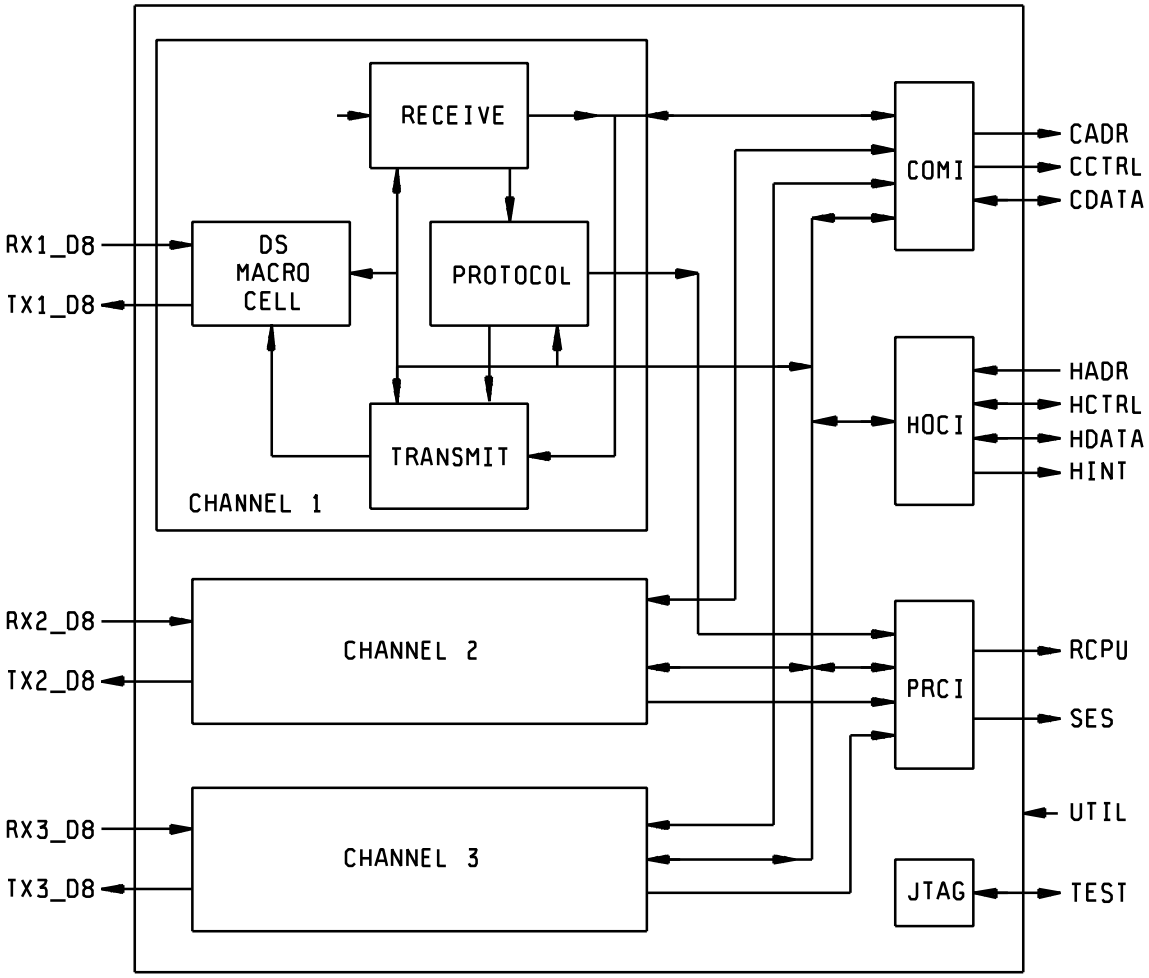


FIGURE 3. Block diagram.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535 appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical Parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical Parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9, 10,11 1/ 3/	1,2,3,7,8,9, 10,11 2/ 3/
Group A test Requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8, 9,10,11 3/	1,2,3,4,7,8, 9,10,11 3/
Group C end point electrical Parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end point electrical Parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end point electrical Parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits are as specified in table IIB herein and shall be required where specified in table I.

TABLE IIB. Delta limits

Parameter 1/	Symbol	Test Method	Test Conditions	Change limits	Unit
Low Level input current 2/	I_{IL}	As per Table I		± 0.1	µA
High level input current 2/	I_{IH}			± 0.1	µA
Output leakage low current 2/	I_{OZL}			± 0.1	µA
Output leakage high current 2/	I_{OZH}			± 0.1	µA
Supply current stand-by for array	I_{DDSBA}	As per Table I		10	µA
Low level output voltage BUF2	V_{OL1}			± 100	mV
Low level output voltage BUF4	V_{OL2}			± 100	mV
High level output voltage BUF2	V_{OH1}			± 100	mV
High level output voltage BUF4	V_{OH2}			± 100	mV

1/ The parameters shall be recorded before and after the required burn-in and life test to determine the delta limits.
2/ Only for inputs and I/O without pull up or pull down.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 01-08-08

Approved sources of supply for SMD 5962-01A17 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-01A1701QXC	F7400	TSS901EAMQ
5962-01A1701VXC	F7400	TSS901EASV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes S.A. Part of Atmel Wireless & Microcontrollers La Chantrerie BP 70602 44306 Nantes Cedex 3 France