REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device types 05 and 06. Change parameter t_{OW} for device types 03 and 04. Add a 20-terminal LCC package.	29 Apr. 1987	

REV																	
PAGE																	
REV STATUS OF PAGES	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
27 June 1986

AMSC N/A

PREPARED BY: Sandra Rooney

CHECKED BY: D. A. DiCenzo

APPROVED BY: Robert P. Evans

SIZE: A

CODE IDENT. NO.: 14933

REV: A

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, NMOS, 4096 X 4-BIT STATIC RAM, MONOLITHIC SILICON

DWG NO.: 5962-86081

PAGE 1 OF 16

5962-E383

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86081	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	2168-55	4096 X 4 static random access memory	(55 ns)
02	2168-70	4096 X 4 static random access memory	(70 ns)
03	2169-50	4096 X 4 static random access memory	(50 ns)
04	2169-70	4096 X 4 static random access memory	(70 ns)
05	2168-45	4096 X 4 static random access memory	(45 ns)
06	2169-40	4096 X 4 static random access memory	(40 ns)

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1/4" x 1-1/16") dual-in-line package
X	(See figure 1) (20-terminal, .430" x .295"), rectangular chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	1.2 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case R	See MIL-M-38510, appendix C
Case X	15°C/W
Junction temperature (T_J)	+175°C
DC output current	20 mA
All signal voltages with respect to GND	-3.5 V dc to +7.0 V dc

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.2 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum ratings are for system design reference only.

2/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Logic diagram. The logic diagram shall be as specified on figure 2.

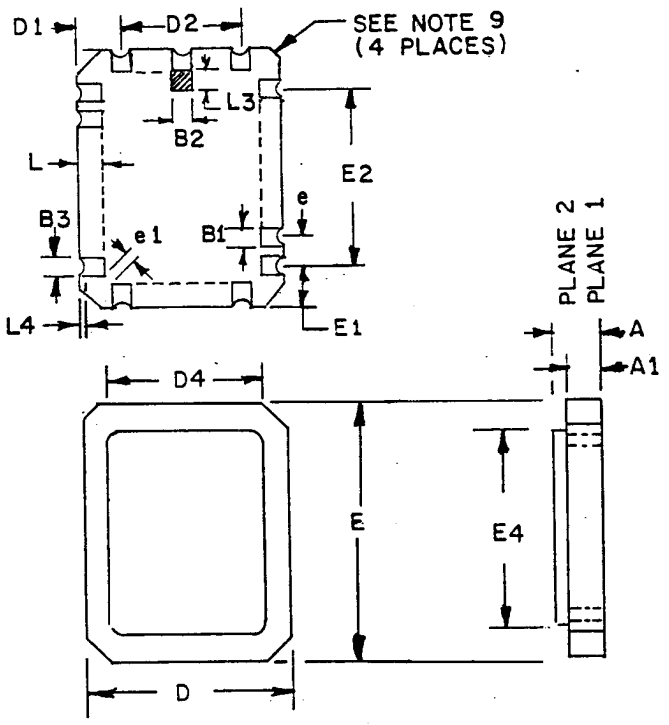
3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Truth table. The truth table shall be as specified on figure 4.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.



Parameter	Min	Max
A	.064 (1.63)	.08 (2.03)
A1	.054 (1.37)	.088 (2.24)
B1	.022 (.056)	.028 (0.71)
B2	.022 (0.56)	.041 (1.04)
D	.284 (7.21)	.296 (7.52)
D1	.065 (1.65)	.085 (2.16)
D2	.145 (3.68)	.155 (3.94)
D4	---	.270 (6.86)
E	.420 (10.67)	.435 (11.05)
E1	.083 (2.11)	.093 (2.36)
E2	.245 (6.22)	.255 (6.48)
E4	---	.410 (10.41)
e	.045 (1.14)	.055 (1.40)
e1	.015 (0.38)	---
L	.045 (1.14)	.055 (1.40)
L3	.032 (0.81)	.052 (1.32)
N	20 (508)	
ND	4 (102)	
NE	6 (152)	
B3	.006 (0.15)	.022 (0.56)
L4	.003 (0.08)	.015 (0.38)

FIGURE 1. Case outline X.

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Metric equivalents are in parentheses.
4. A minimum clearance of .015 inch (0.38 mm) shall be maintained between corner terminals, and refers to dimension e1.
5. N is the maximum quantity of terminal positions. ND and NE are the numbers of terminals along the sides of length D and E respectively.
6. Electrical, connection terminals are required on plane 1 and optional on plane 2. However, if plane 2 has such terminals they shall be electrically connected to opposing terminals on plane 1.
7. A minimum clearance of .020 (0.51 mm) shall be maintained between the lid and other features such as plane 2 terminals. The lid shall not extend beyond the edges of the body.
8. The index feature for number 1 terminal identification, optional orientation or handling purposes shall be within the shaded areas shown on plane 1; and is defined by dim. B2 and L3.
9. The chip carrier corner shape (square, notch, radius, etc.) may vary at the manufacturer's option from that shown in the chip carrier drawing.
10. Diameter B3 and L4 define the maximum castellation width and depth respectively, at any point of surface. Castellations are required on bottom two layers and optional in the top layer.
11. Package shall consist of a minimum of two ceramic layers.

FIGURE 1. Case outline X - Continued.

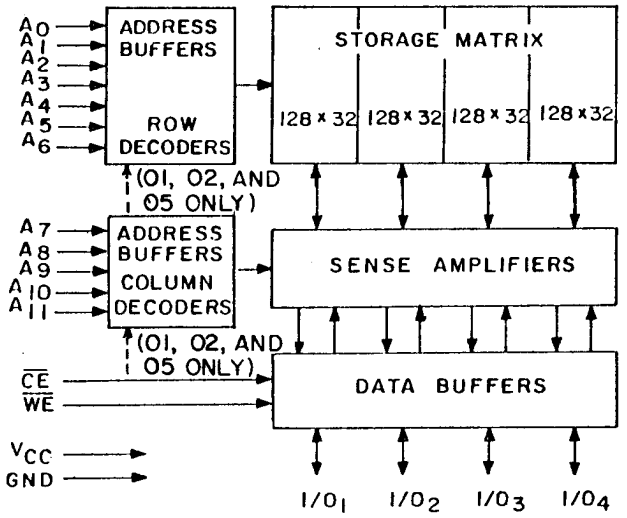
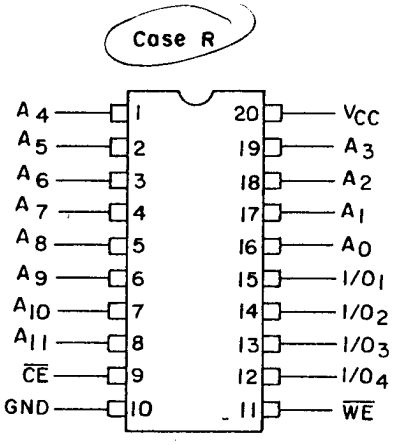


FIGURE 2. Logic diagram.



NOTE: Pin 1 is marked for orientation.

FIGURE 3. Terminal connections.

$\overline{CE}$	$\overline{WE}$	Mode	Power	I/O
H	X	Not selected	Stand by (01, 02) Active (03, 04)	High Z
L	L	Write	Active	D_{In}
L	H	Read	Active	D_{Out}

FIGURE 4. Truth table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Output high current	I_{OH}	V_{OH} = 2.4 V; V_{CC} = 4.5 V	1,2,3	All	-4		mA
Output low current	I_{OL}	V_{OL} = 0.4 V	1,2,3	All	8		mA
Input high voltage	V_{IH}		1,2,3	All	2.2	6.0	V
Input low voltage	V_{IL}	3/	1,2,3	All	-0.5	0.8	V
Input load current	I_{IX}	$GND \le V_I \le V_{CC}$	1,2,3	All	-10	10	µA
Output leakage current	I_{OZ}	$GND \le V_O \le V_{CC}$ Output disabled	1,2,3	All	-50	50	µA
V_{CC} operating supply current	I_{CC}	Maximum V_{CC}, $\overline{CE} \le V_{IL}$ Output open	1,2,3	All		160	mA
Automatic $\overline{CE}$ power down current	I_{SB}	Maximum V_{CC}, $\overline{CE} \ge V_{IH}$	1,2,3	05 01,02 03,04 06		30 N/A	mA mA
Output short-circuit current	I_{OS}		1,2,3 4/	All	-400	+400	mA
Input capacitance	C_I	Test frequency = 1.0 MHz T_A = +25°C, All pins at 0 V V_{CC} = 5 V 4/	4	All		5	pF
Input/output capacitance	$C_{I/O}$	4/	4	All		7	pF
Address valid to address do not care time (read cycle time)	t_{RC}	See figures 5 and 6	9,10,11	01,03 02,04 05,06	50 70 40		ns ns ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Address valid to data out valid delay (address access time)	t_{AA}	See figures 5 and 6	9,10,11	01,03		50	ns
				02,04		70	ns
				05,06		40	ns
Chip enable low to data valid (chip enable access time)	t_{ACS}	See figures 5 and 6	9,10,11	01		55	ns
				02		70	ns
				03		25	ns
				04		30	ns
				05		45	ns
				06		20	ns
Chip enable low to data out on	t_{LZ} 5/	See figures 5 and 7	4/	01			
				02,05	5		ns
				03,04 06	2		ns
Chip enable high to data out off	t_{HZ} 5/	See figures 5 and 7	4/	01,03	0	25	ns
				02,04,	0	30	ns
				05,06	0	20	ns
Address unknown to data out unknown time	t_{OH}	See figures 5 and 6	4/	All	1		ns
Chip enable high to power down delay	t_{PD}	See figures 5 and 6	4/	01		55	ns
				02		70	ns
				05		45	ns
Chip enable low to power up delay	t_{PU}	See figures 5 and 6	4/	01,02 05	0		ns
Address valid to address do not care (write cycle time)	t_{WC}	See figures 5 and 6	9,10,11	01,03	50		ns
				02,04	70		ns
				05,06	40		ns
Write enable low to write enable high	t_{WP} 6/	See figures 5 and 6	9,10,11	01,03	45		ns
				02,04	65		ns
				05,06	35		ns
Write enable high to address do not care	t_{WR}	See figures 5 and 6	9,10,11	All	0		ns
Write enable low to output in high Z	t_{WZ} 5/	See figures 5 and 7	4/	01,03	0	20	ns
				02,04	0	25	ns
				05,06	0	15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Data in valid to write enable high	t_{DW}	See figures 5 and 6	9,10,11	01,03	25		ns
				02,04	35		ns
				05,06	20		ns
Data hold time	t_{DH}	See figures 5 and 6	9,10,11	All	5		ns
Address valid to write enable low	t_{AS}	See figures 5 and 6	9,10,11	All	0		ns
Chip enable low to write enable high	t_{CW} 6/	See figures 5 and 6	9,10,11	01,03	50		ns
				02,04	70		ns
				05,06	40		ns
Write enable high to output in low Z	t_{OW} 5/	See figures 5 and 7	4/	01, 02,05	5		ns
				03,04, 06	0		ns
Address valid to end of write	t_{AW}	See figures 5 and 6	9,10,11	01,03	50		ns
				02,04	70		ns
				05,06	40		ns

1/ Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance. Output timing reference is 1.5 V.

2/ The operating case temperature range is guaranteed with transverse air flow of 400 linear feet per minute.

3/ V_{IL} voltages of less than -0.5 V on the I/O pins will cause the output current to exceed the maximum rating and thus should not exceed 30 seconds in duration.

4/ Tested initially and after any design changes.

5/ Transition is measured at 1.5 V on the input to V_{OH} -500 mV and V_{OL} +500 mV on the outputs using the load shown on figure 7. C_L = 5 pF.

6/ The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

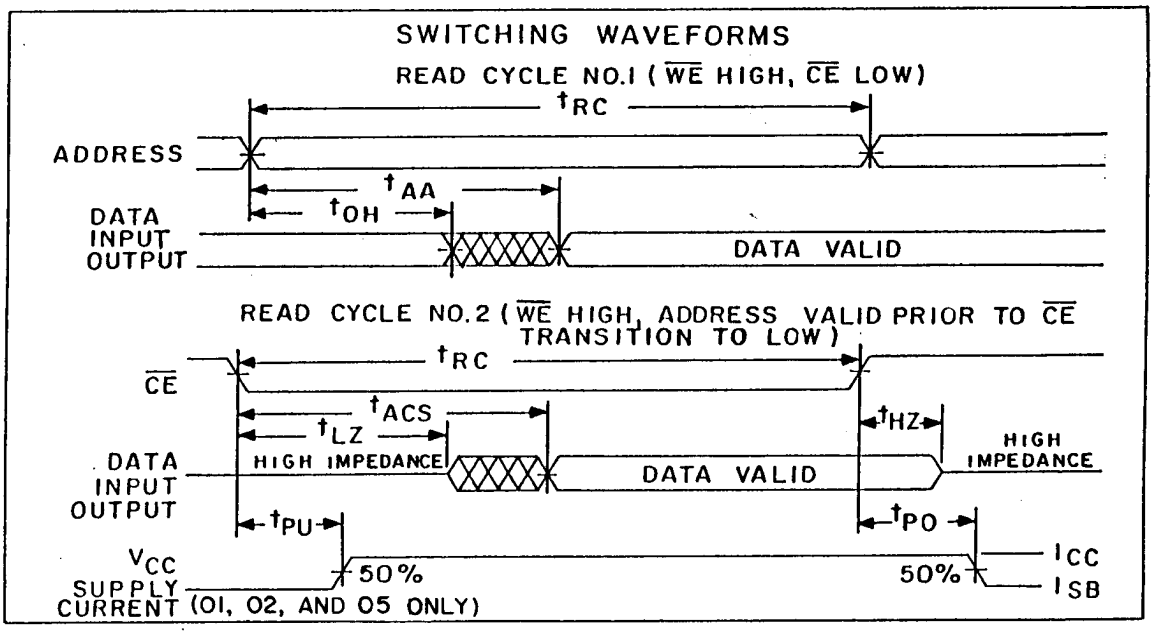
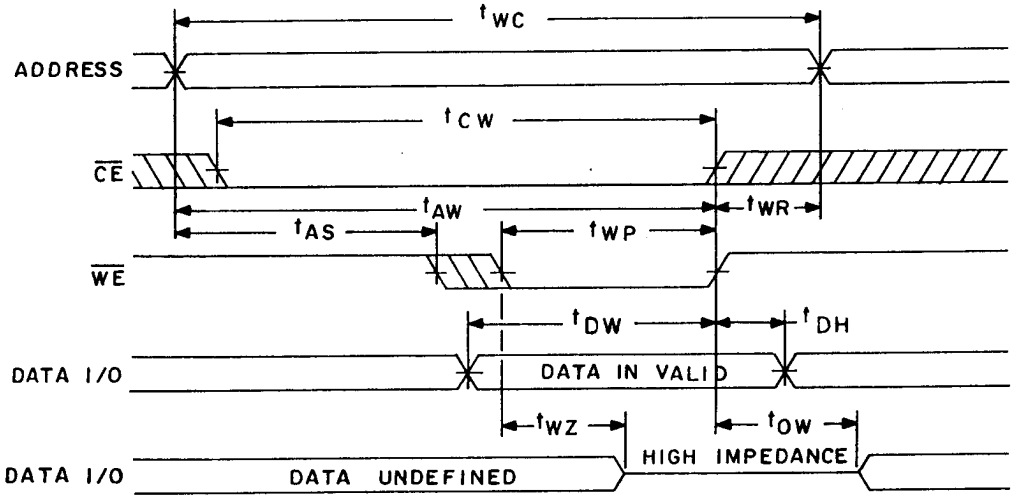
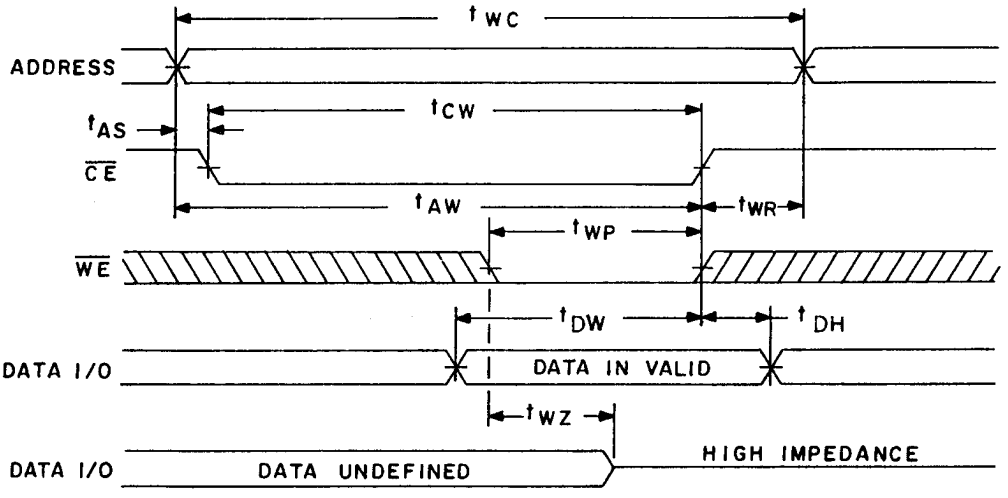


FIGURE 5. Switching waveforms.

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)



NOTE: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

FIGURE 5. Switching waveforms - Continued.

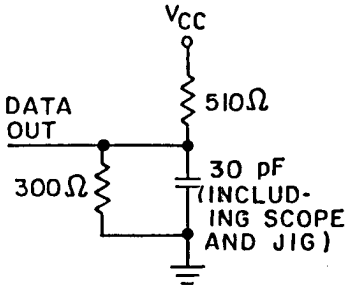


FIGURE 6. Output load.

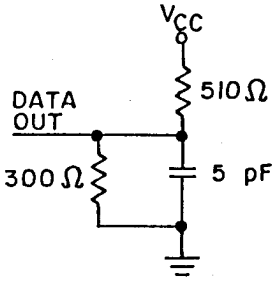


FIGURE 7. Output load for t_{HZ}, t_{LZ}, t_{OW}, and t_{WZ}.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 ($C_I/C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall consist of verifying the truth table specified on figure 4.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9
Group A test requirements (method 5005)	1,2,3,4,7,8,9, 10,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroups 1 and 7.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8608101RX	34335	AM2168-55/BRA	---
5962-8608101XX		AM2168-55/BUA	
5962-8608102RX	34335	AM2168-70/BRA	---
5962-8608102XX		AM2168-70/BUA	
5962-8608103RX	34335	AM2169-50/BRA	---
5962-8608103XX		AM2169-50/BUA	
5962-8608104RX	34335	AM2169-70/BRA	---
5962-8608104XX		AM2169-70/BUA	
5962-8608105RX	34335	AM2168-45/BRA	---
5962-8608105XX		AM2168-45/BUA	---
5962-8608106RX	34335	AM2169-40/BRA	---
5962-8608106XX		AM2169-40/BUA	---

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088