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Defense Electronics Supply Center Dayton, Ohio	PREPARED BY Ray Monnin	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY DA DiCenzo	
Original date of drawing: 1 May 1987	APPROVED BY MA Frank	TITLE: MICROCIRCUIT, UNIVERSAL INTERRUPT CONTROLLER, N-CHANNEL MOS, MONOLITHIC SILICON
	SIZE A / CODE IDENT. NO. 14933	DWG NO. 5962-87597
AMSC N/A	REV	PAGE 1 OF 14

5962-E403

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DESC FORM 193

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87597	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	9519A	Universal interrupt controller

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	D-10 (28-lead, 1/2" X 1-3/8") dual-in-line package Dip28.6
Y	C-5 (44-terminal, .650" X .650") square chip carrier package Lcc type C44

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation P_D (1/)	+1.5 W
Lead temperature (soldering, 5 seconds)	270°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case X 2/	30°C/W
Case Y 2/	15°C/W
Junction temperature (T_J)	150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Minimum low-level input voltage (V_{IL})	-0.5 V dc
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum high-level input voltage (V_{IH})	V_{CC}
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

2/ When a thermal resistance value for this case is included in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC}=4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input low voltage	V_{IL}		1,2,3		.8	V
Input high voltage	V_{IH}		1,2,3	2.0		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 3.2 mA	1,2,3		.40	V
Output low voltage (EO only)	V_{OL}	V_{CC} = 4.5 V I_{OL} = 1.0 mA	1,2,3		.40	V
Output high voltage 1/	V_{OH}	V_{CC} = 4.5 V I_{OH} = -200 µA	1,2,3	2.4		V
Output high voltage (EO only)	V_{OH}	V_{CC} = 4.5 V I_{OH} = -100 µA	1,2,3	2.4		V
Output float leakage	I_{OZ}	V_{CC} = 5.5 V V_{OUT} = 5.5 V and 0.0 V Output off	1,2,3	-150	+150	µA
Input leakage	I_{IX}	V_{CC} = 5.5 V V_{IN} = 5.5 V and 0.0 V	1,2,3	-10	+10	µA
Input leakage (EI only)	I_{IX}	V_{CC} = 5.5 V V_{IN} = 5.5 V and 0.0 V	1,2,3	-60	+10	µA
Power supply current	I_{CC}	V_{CC} = 5.5 V 2/	1,2,3		200	mA
Input capacitance	C_{IN}	F_C = 1 MHz T_A = 25°C See 4.3.1d	4		10	pF
Output capacitance	C_O		4		15	pF
I/O capacitance	$C_{I/O}$		4		20	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, $V_{CC}=4.5$ V to 5.5 V unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
C/$\overline{D}$ valid and $\overline{CS}$ low to READ low	t_{AVRL}	3/, 4/	9,10,11	0		ns
C/$\overline{D}$ valid and $\overline{CS}$ low to WRITE low	t_{AVWL}		9,10,11	0		ns
$\overline{RIP}$ low to $\overline{PAUSE}$ high 5/	t_{CLPH}		9,10,11	75	375	ns
$\overline{RIP}$ low to data out valid 6/	t_{CLQV}		9,10,11		50	ns
Data in valid to write high	t_{DVWH}		9,10,11	250		ns
EI high to $\overline{RIP}$ low 7/	t_{EHCL}		9,10,11	30	300	ns
Interrupt request valid to GINT valid	t_{IVGV}		9,10,11	100	800	ns
Interrupt request valid to interrupt request don't care. (IREQ pulse duration)	t_{IVIX}		9,10,11	250		ns
$\overline{IACK}$ high to $\overline{RIP}$ high	t_{KHCH}		9,10,11		450	ns
$\overline{IACK}$ high to GINT invalid	t_{KHIH}		9,10,11		1000	ns
$\overline{IACK}$ high to $\overline{IACK}$ low ($\overline{IACK}$ recovery)	t_{KHKL}		9,10,11	140		ns
$\overline{IACK}$ high to EO high 8/, 9/	t_{KHNH}		9,10,11		975	ns

See footnotes at end of table.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-87597
		REV	PAGE 5

DESC FORM 193A
FEB 86

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, V_{CC}=4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{IACK}$ high to data out invalid	t_{KHQX}	3/, 4/	9,10,11	20	200	ns
$\overline{IACK}$ low to $\overline{RIP}$ low 7/, 10/	t_{KLCL}		9,10,11	75	650	ns
$\overline{IACK}$ low to $\overline{IACK}$ high (1st $\overline{IACK}$) 10/	t_{KLKH}		9,10,11	975		ns
$\overline{IACK}$ low to $\overline{EO}$ low 8/,9/,10/	t_{KLNL}		9,10,11		125	ns
$\overline{IACK}$ low to $\overline{PAUSE}$ low 10/	t_{KLPL}		9,10,11	25	175	ns
$\overline{IACK}$ low to data out valid 6/,10/	t_{KLQV}		9,10,11	25	300	ns
1st $\overline{IACK}$ low to data out valid 10/	t_{KLQV1}		9,10,11	75	650	ns
$\overline{PAUSE}$ high to $\overline{IACK}$ low	t_{PHKH}		9,10,11	0		ns
Read high to C/$\overline{D}$ and $\overline{CS}$ don't care	t_{RHAX}		9,10,11	0		ns
Read low to data out valid	t_{RLQV}		9,10,11		300	ns
Read high to data out invalid	t_{RHQX}		9,10,11	20	200	ns
Read low to data out unknown	t_{RLQX}			35		ns
Read low to read high ($\overline{RD}$ pulse duration)	t_{RLRH}		9,10,11	300		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC}=4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Write high to C/$\overline{D}$ and $\overline{CS}$ don't care	t_{WHAX}	3/, 4/	9,10,11	25		ns
Write high to data in don't care	t_{WHDX}		9,10,11	25		ns
Write high to read or write low ($\overline{WR}$ recovery	t_{WHRW}		9,10,11	600		ns
Write low to write high ($\overline{WR}$ pulse duration)	t_{WLWH}		9,10,11	300		ns

1/ V_{OH} specifications do not apply to $\overline{RIP}$, $\overline{PAUSE}$ or GINT when active low. These outputs are open-drain and V_{OH} levels will be determined by external circuitry.
2/ I_{CC} is measured in a static condition with outputs in the worst condition with all outputs unloaded.
3/ Test conditions V_{IL}=0.45 V V_{IH}=2.4 V
V_{OL}=0.8 V V_{OH}=2.0 V
I_{OL}=3.2 mA I_{OH}=-200 µA
I_{OL}=1.0 mA I_{OH}=-100 µA (EO only)
C_L=100 pF
4/ See figure 4.
5/ During the first $\overline{IACK}$ pulse, $\overline{PAUSE}$ will be low long enough to allow for priority resolution and will not go high until after $\overline{RIP}$ goes low (t_{CLPH}).
6/ t_{KLQV} applies only to second, third, and fourth $\overline{IACK}$ pulses while $\overline{RIP}$ is low. During the first $\overline{IACK}$ pulse, data out will be valid following the falling edge of $\overline{RIP}$ (t_{CLQV}).
7/ $\overline{RIP}$ is pulled low to indicate that an interrupt request has been selected. $\overline{RIP}$ cannot be pulled low until EI is high following an internal delay. t_{KLCL} will govern the falling edge of $\overline{RIP}$ when EI is always high or is high early in the acknowledge cycle. t_{EHCL} will govern when EI goes high later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. $\overline{RIP}$ remains low until after the rising edge of $\overline{IACK}$ pulse that transfers the last response byte for selected IREQ.
8/ Test conditions for EO assume an output loading of I_{OL}=1.0mA and I_{OH}=-100µA
9/ The arrival of $\overline{IACK}$ will cause EO to go low, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return high when EI is high. If a pending request is selected, EO will stay low until after the last $\overline{IACK}$ pulse for that interrupt is complete and $\overline{RIP}$ goes high.
10/ $\overline{CS}$ must be high for at least 100 ns prior to $\overline{IACK}$ going low.

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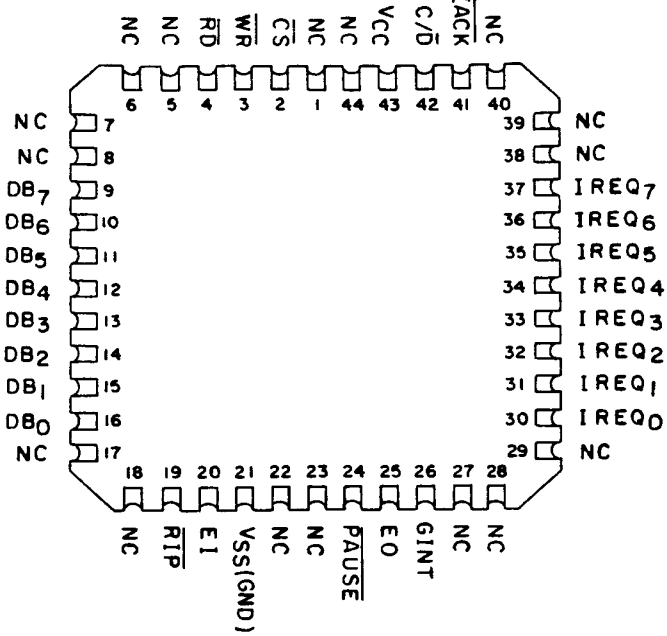
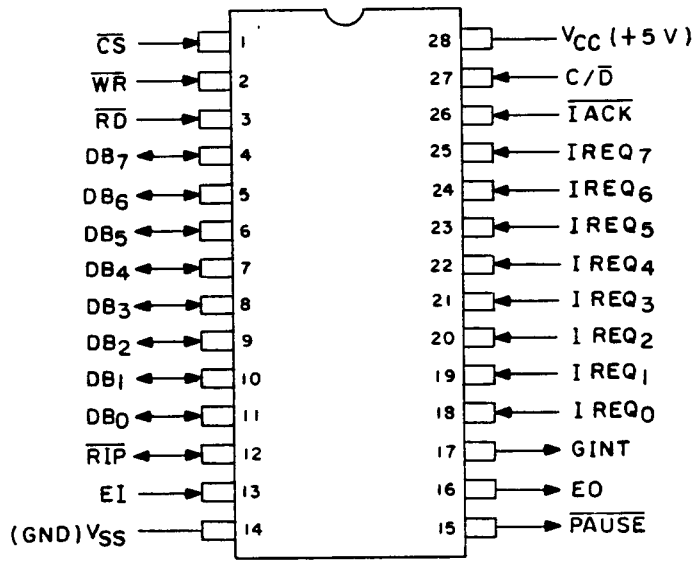
Top view



Case outline Y

Top view



Case outline X

FIGURE 1. Terminal connections.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-87597
		REV	PAGE 8

DESC FORM 193A
FEB 86

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Control input					Data bus operation
$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{IACK}$	
0	0	0	1	1	Transfer contents of preselected data register to data bus
0	0	1	0	1	Transfer contents of data bus to preselected data register
0	1	1	0	1	Transfer contents of status register to data bus
0	1	1	0	1	Transfer contents of data bus to command register
1	X	X	X	0	Transfer contents of selected response memory location to data bus
1	X	X	X	1	No information transferred

Command code								Command description
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	Reset
0	0	0	1	0	X	X	X	Clear all IRR and all IMR bits
0	0	0	1	1	B2	B1	B0	Clear all IRR and IMR bits specified by B2, B1, B0
0	0	1	0	0	X	X	X	Clear all IMR
0	0	1	0	1	B2	B1	B0	Clear IMR bits specified by B2, B1, B0
0	0	1	1	0	X	X	X	Set all IMR bits
0	0	1	1	1	B2	B1	B0	Set IMR bits specified by B2, B1, B0
0	1	0	0	0	X	X	X	Clear all IRR bits
0	1	0	0	1	B2	B1	B0	Clear IRR bit specified by B2, B1, B0
0	1	0	1	0	X	X	X	Set all IRR bits
0	1	0	1	1	B2	B1	B0	Set IRR bit specified by B2, B1, B0
0	1	1	0	X	X	X	X	Clear highest priority ISR bit
0	1	1	1	0	X	X	X	Clear all ISR bits
0	1	1	1	1	B2	B1	B0	Clear ISR bit specified by B2, B1, B0
1	0	0	M4	M3	M2	M1	M0	Load mode register bits 0-4 with specified pattern
1	0	1	0	M6	M5	0	0	Load mode register bits 5, 6 with specified pattern
1	0	1	0	M6	M5	0	1	Load mode register bits 5, 6 and set mode bit 7
1	0	1	0	M6	M5	1	0	Load mode register bits 5, 6 and clear mode bit 7
1	0	1	1	X	X	X	X	Preselected IMR for subsequent loading from data bus
1	1	0	0	X	X	X	X	Preselected auto clear register for subsequent loading from data bus
1	1	1	BY1	BY0	L2	L1	L0	Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus

FIGURE 2. Truth table.

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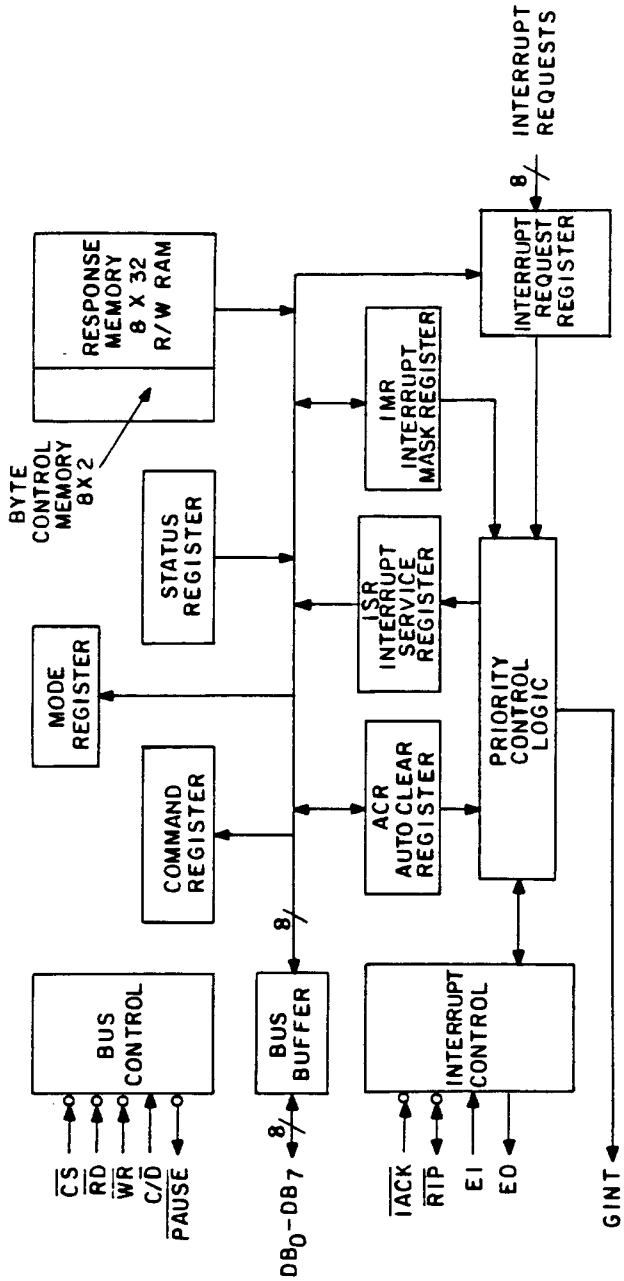

FIGURE 3. Block diagram.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 14933	DWG NO. 5962-87597
		REV	PAGE 10

DESC FORM 193A
FEB 86

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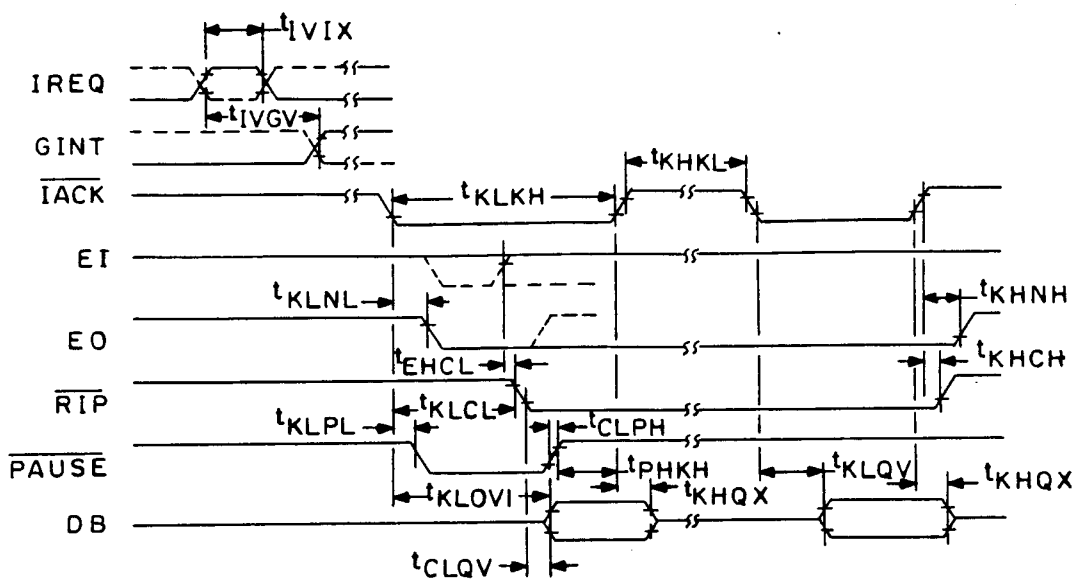
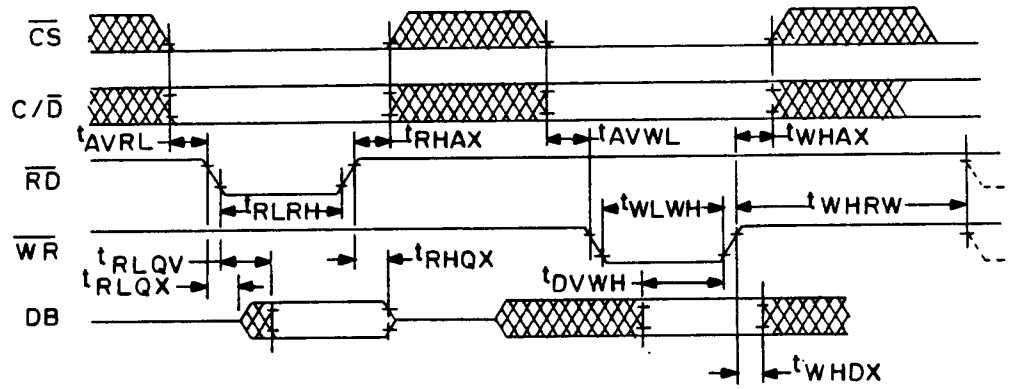


INTERRUPT OPERATIONS



DATA BUS TRANSFERS

FIGURE 4. Switching waveforms.

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3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition C using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 sufficient to verify the function table.

d. Subgroup 4 (C_{IN}, C_O, $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect input and output capacitances.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8, 9,10,11
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8759701XX	34335	AM9519A/BXA
5962-8759701YX	34335	AM9519A/BUA

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088

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