REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add CAGE number 50364 as a supplier for 02 and 03 device types. Add 04 device type. Add CAGE number 1FN41 as a supplier of the K package. Editorial changes throughout entire document. Remove C as a test condition option.	1989 AUG 23	M. A. Frye
B	Change C_I and C_O values in Table I. Incorporate power reset feature. Add 05 device. Add CAGE number 65786 for 04K, 04L and 043 devices. Add footnote 7/ to Table I. Editorial changes throughout entire document.	1991 NOV 06	M. A. Frye

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REV STATUS OF SHEETS	REV	B	B	B	B	B	B		A	B	B	B	B											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12											

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE: 27 JULY 1988

REVISION LEVEL: B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ONE-TIME PROGRAMMABLE, PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-88670

SHEET 1 OF 12

DESC FORM 193
SEP 87

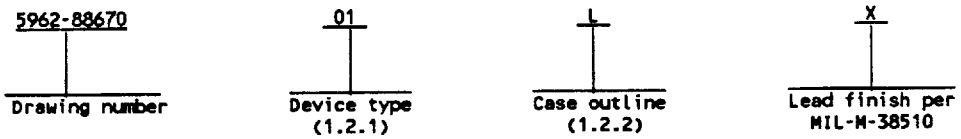
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E353

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or identifying number. The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	C22V10	22-input 10-output and-or-logic array	25 ns
02	C22V10	22-input 10-output and-or-logic array	30 ns
03	C22V10	22-input 10-output and-or-logic array	40 ns
04	C22V10	22-input 10-output and-or-logic array	20 ns
05	C22V10	22-input 10-output and-or-logic array	15 ns

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24-lead, .640" x .420" x .090"), flat package
L	D-9 (24-lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-2.0 V dc to +7.0 V dc 2/
Output voltage applied range	-0.5 V dc to +7.0 V dc 2/
Output sink current	16 mA
Thermal resistance, junction-to-case (O_{JC}):	See MIL-M-38510, appendix C
Maximum power dissipation (P_D) 3/	1.2 W
Maximum junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds maximum)	+260°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc minimum
Low level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ All voltages referenced to V_{SS}.
2/ Minimum voltage is -0.6 V dc which may undershoot to -2.0 V dc for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} +0.75 V dc which may overshoot to +7.0 V dc for pulses of less than 20 ns.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test with a minimum of 50 percent of the total number of gates programmed or to any altered item drawing pattern which includes at least 25 percent of the total number of gates programmed.

3.2.3.2 Programmed devices. The truth tables for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 7/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	I_O = -2.0 mA V_{IL} = 0.8 V V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_O = 12.0 mA V_{IL} = 0.8 V V_{IH} = 2.0 V	1, 2, 3	All		0.5	V
High impedance output leakage current 2/	I_{OZ}	V_{CC} = 5.5 V	1, 2, 3	All	-40	40	µA
High level input current	I_{IH}	V_{IH} = 5.5 V (excludes I/O pins)	1, 2, 3	All	0	10	µA
Low level input current	I_{IL}	V_{IL} = GND (excludes I/O pins)	1, 2, 3	All	-10	0	µA
Standby power supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = GND	1, 2, 3	01-03		100	mA
				04,05		120	mA
Output short circuit current 3/ 4/	I_{OS}	V_{CC} = 5.5 V, V_O = 0.5 V Outputs open for unprogrammed device	1, 2, 3	All	-30	-90	mA
Input capacitance 4/ 5/	C_I	V_I = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.3.1c)	4	All		10	pF
Output capacitance 4/ 5/	C_O	V_O = 0 V, V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz, (see 4.3.1c)	4	All		10	pF
Input to output enable	t_{EA}	V_{CC} = 4.5 V, C_L = 5 pF, See figure 3 (circuit A) and figure 4	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
Input to output disable	t_{ER}		9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, C_L = 50 pF, See figure 3 (circuit B) and figure 4	9, 10, 11	01		25	ns
				02		30	
				03		40	
				04		20	
				05		15	
Clock to output	t_{CO}		9, 10, 11	01, 04		15	ns
				02		20	
				03		25	
				05		10	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 7/ V_{SS} = 0 V, -55°C ≤ T_C ≤ +125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Clock period (t_{co} + t_s)	t_P	V_{CC} = 4.5 V, C_L = 50 pF, See figure 3 (circuit B) and figure 4	9, 10, 11	01	33		ns
				02	40		
				03	55		
				04	32		
				05	22		
Clock pulse width 4/ 6/	t_W		9, 10, 11	01,04	15		ns
				02	20		
				03	27		
				05	6		
Setup time 4/ 6/	t_S		9, 10, 11	01	18		ns
				02	20		
				03	30		
				04	17		
				05	12		
Hold time 4/ 6/	t_H		9, 10, 11	All	0		ns
Maximum clock frequency 4/ 6/	f_{MAX}		9, 10, 11	01	30		MHz
				02	25		
				03	18		
				04	31		
				05	45		
Asynchronous reset pulse width	t_{AW}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
Asynchronous reset recovery time	t_{AR}		9, 10, 11	01	25		ns
				02	30		
				03	40		
				04	20		
				05	15		
Asynchronous reset to registered output reset	t_{AP}		9, 10, 11	01,04		25	ns
				02		30	
				03		40	
				05		20	
Power-up reset time 4/	t_{PR}	See figure 5	9, 10, 11	All		1	µs

1/ All voltages are referenced to ground.
2/ I/O terminal leakage is the worst case of I_{IX} or I_{OZ}.
3/ Only one output shorted at a time.
4/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
5/ All pins not being tested are to be open.
6/ Test applies only to register outputs.
7/ AC testing. Input pulse levels are 0 to 3.0 V with transition times of 5ns or less. Timing reference levels are 1.5 V unless otherwise specified.

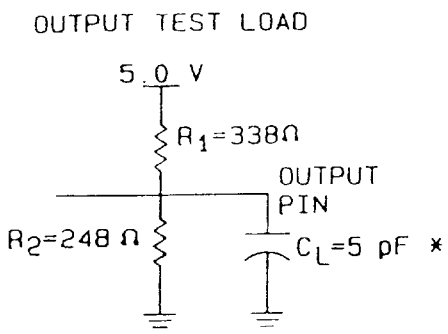
Device types	01, 02, 03, 04, 05	
Case outlines	K, L	3
Terminal number	Terminal symbol	
1	CP/I	NC
2	I	CP/I
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O	GND
15	I/O	NC
16	I/O	I
17	I/O	I/O
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	NC
23	I/O	I/O
24	V_{CC}	I/O
25	---	I/O
26	---	I/O
27	---	I/O
28	---	V_{CC}

FIGURE 1. Terminal connections.

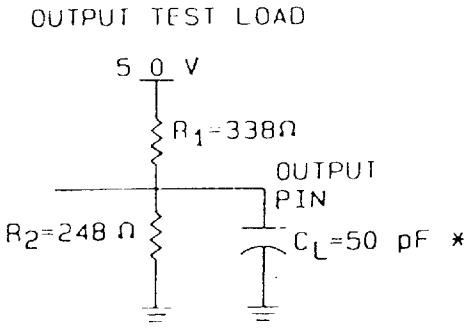
Truth table																					
Input pins												Output pins									
CP/I	I	I	I	I	I	I	I	I	I	I	I	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
X	X	X	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

NOTES:
1. Z = 3-state
2. X = don't care

FIGURE 2. Truth table (unprogrammed).



Circuit A or equivalent (t_{EA} and t_{ER})



Circuit B or equivalent

*Including jig and scope
(minimum value)

NOTES:
1. AC testing. Inputs pulse levels are 0 to 3.0 V with transition times of 5 ns or less. Timing reference levels are 1.5 V unless otherwise specified.
2. t_{EA} and t_{ER} transition are measured ±500 mV from steady state voltage.

FIGURE 3. Output test circuits.

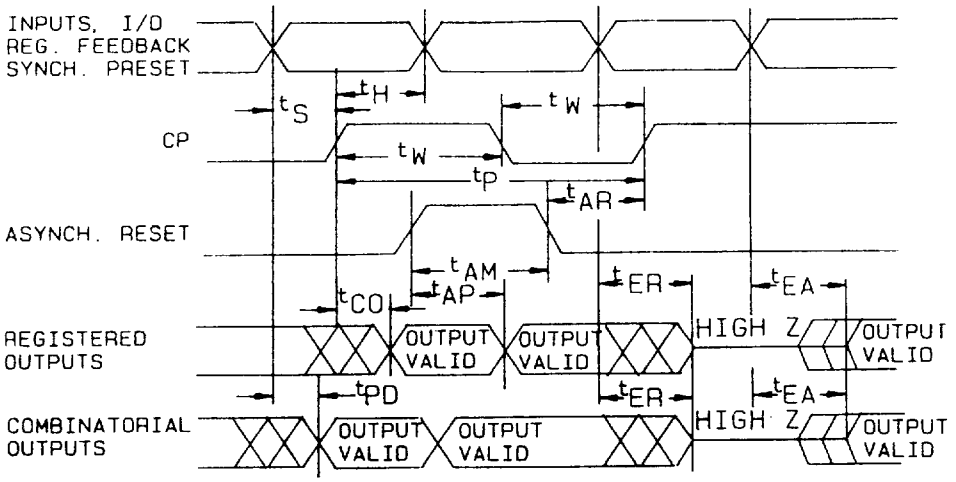
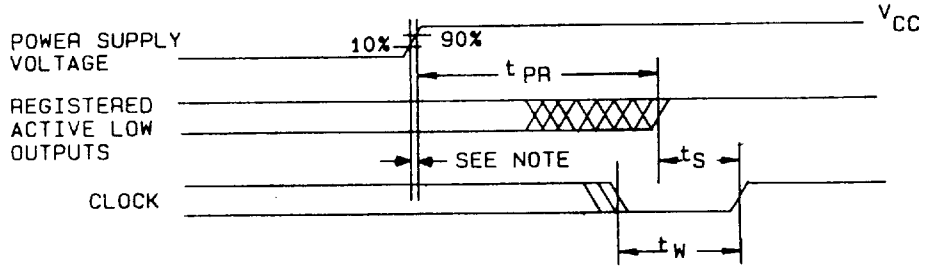


FIGURE 4. Switching waveforms.



NOTE: The power-up reset feature ensures that all flip-flops will be reset to low after the device has been powered up. The following conditions are required:

a) The V_{CC} rise must be monotonic.
b) After reset occurs, all applicable input and feedback setup times must be met before driving the clock pin high.
c) The clock signal must remain stable beginning prior to the occurrence of the 10% level and continuing until the end of t_{PR}.

FIGURE 5. POWER-UP RESET WAVEFORM.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.10.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table II. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for the initial characterization and after any process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. Unprogrammed devices shall be tested for programmability and ac performance compliance to the requirements of group A, subgroups 9, 10, and 11.

(1) A sample shall be selected to satisfy programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.3.1). If more than two devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable.

(2) Ten devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9, 10, and 11. If more than two devices fail, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004) for unprogrammed devices	1*,2,3,7*, 8a,8b
Final electrical test parameters (method 5004) for programmed devices	1*,2,3,7*,8a, 8b,9
Group A test requirements (method 5005)	1,2,3,4**,7, 8a,8b,9,10,11
Groups C and D end-point electrical parameters (method 5005)	2,3,7,8a,8b

1/ * indicates PDA applies to subgroups 1 and 7.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ ** see 4.3.1c.
4/ Subgroups 7 and 8 functional tests shall also verify that no cells are programmed for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

c. For quality conformance inspection, the programmability sample (see 4.3.1d) shall be included in subgroup 1 test.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6021.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.