

Octal transceiver (3-State)

74ALS645A/74ALS645A-1

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 24mA and source 15mA
- Outputs are placed in high impedance state during power-off conditions
- The -1 version sinks 48mA I_{OL} within the +5% V_{CC} range

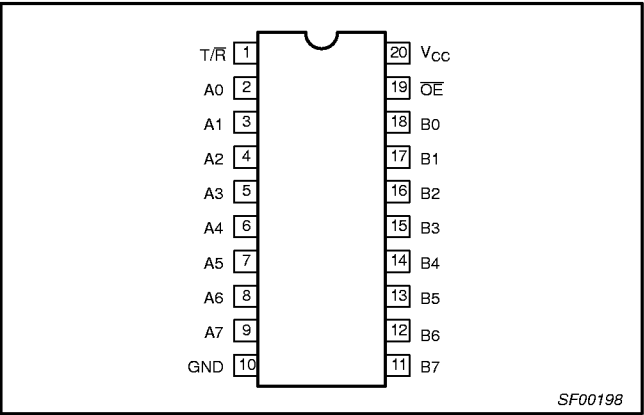
DESCRIPTION

The 74ALS645A is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both transmit and receive directions. The device features an output enable ($\overline{OE}$) input for easy cascading and transmit/receive ($\overline{R/T}$) input for direction control.

The 74ALS645A-1 is the same as the 74ALS645A except that both ports sink 48mA within the $\pm 5\%$ V_{CC} range.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74ALS645A	7.0ns	34mA
74ALS645A-1	7.0ns	34mA

PIN CONFIGURATION



ORDERING INFORMATION

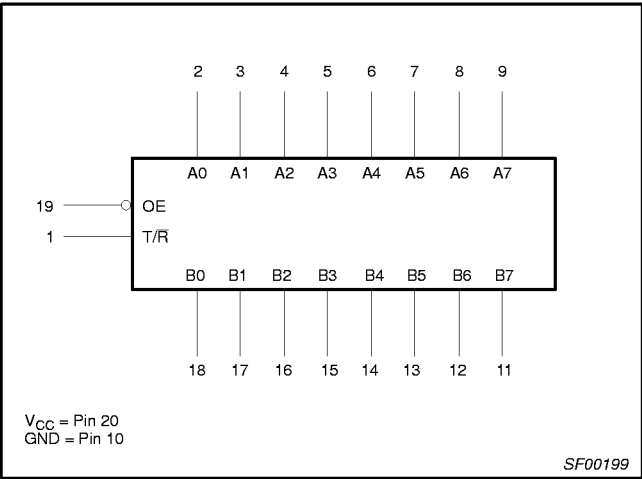
DESCRIPTION	ORDER CODE	DRAWING NUMBER
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$	
20-pin plastic DIP	74ALS645AN, 74ALS645A-1N	SOT146-1
20-pin plastic SOL	74ALS645AD, 74ALS645A-1D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

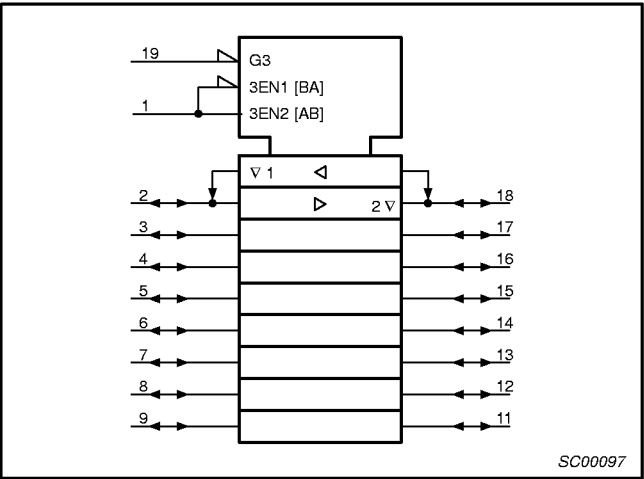
PINS	DESCRIPTION	74ALS (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A0 – A7, B0 – B7	Data inputs	1.0/1.0	20 μ A/0.1mA
$\overline{OE}$	Output Enable input (active-Low)	1.0/1.0	20 μ A/0.1mA
$\overline{T/R}$	Transmit/receive input	1.0/1.0	20 μ A/0.1mA
A0 – A7	A port outputs	750/240	15mA/24mA
B0 – B7	B port outputs	750/240	15mA/24mA
A0 – A7	A port outputs (-1 version)	750/480	15mA/48mA
B0 – B7	B port outputs (-1 version)	750/480	15mA/48mA

NOTE: One (1.0) ALS unit load is defined as: 20 μ A in the High state and 0.1mA in the Low state.

LOGIC SYMBOL



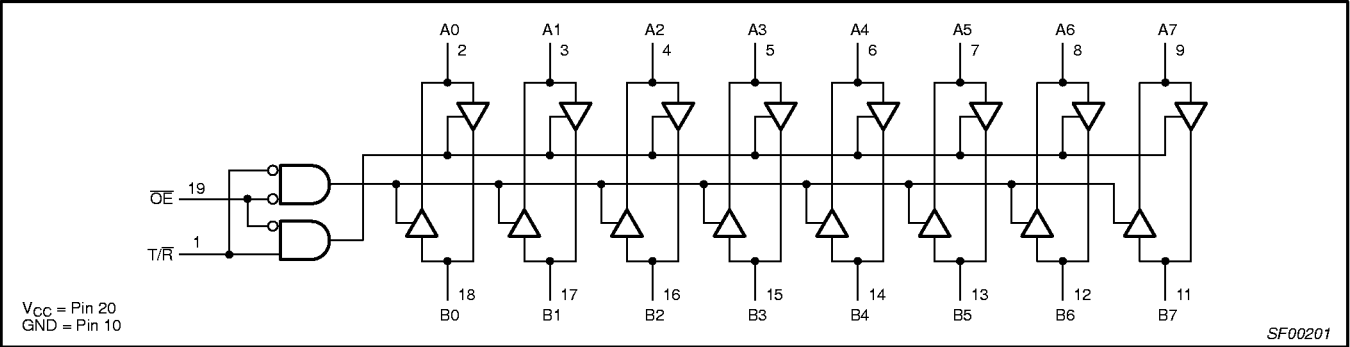
IEC/IEEE SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/R	
L	L	Bus B data to Bus A
L	H	Bus A data to Bus B
H	X	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	All versions	48	mA
		-1 version	96	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current	All versions		24	mA
		-1 version		48 ¹	mA
T_{amb}	Operating free-air temperature range	0		+70	°C

NOTES:

1. The 48mA limit applies only under the condition of $V_{CC} = 5.0V \pm 5\%$.

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DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT
					MIN	TYP ²	MAX	
V_{OH}	High-level output voltage		$V_{CC} \pm 10\%$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OH} = -0.4\text{mA}$	$V_{CC} - 2$			V
				$I_{OH} = -3\text{mA}$	2.4	3.2		V
			$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OH} = -15\text{mA}$	2.0			V
V_{OL}	Low-level output voltage	All versions	$V_{CC} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OL} = 12\text{mA}$		0.25	0.40	V
				$I_{OL} = 24\text{mA}$		0.35	0.50	V
		-1 version	$V_{CC} = 4.75\text{V}$, $V_{IL} = \text{MAX}$, $V_{IH} = \text{MIN}$	$I_{OL} = 48\text{mA}$		0.35	0.50	V
V_{IK}	Input clamp voltage		$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-0.73	-1.5	V
I_I	Input current at maximum input voltage	$\overline{OE}$ or $T/\overline{R}$	$V_{CC} = \text{MAX}$, $V_I = 7.0\text{V}$				0.1	mA
		A or B ports	$V_{CC} = \text{MAX}$, $V_I = 5.5\text{V}$				0.1	mA
I_{IH}	High-level input current ³		$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$				20	μA
I_{IL}	Low-level input current ³		$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$				-0.1	mA
I_O	Output current ⁴		$V_{CC} = \text{MAX}$, $V_O = 2.25\text{V}$		-30		-112	mA
I_{CC}	Supply current (total)	I_{CCH}	$V_{CC} = \text{MAX}$			28	45	mA
		I_{CCL}				40	55	mA
		I_{CCZ}				44	58	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{\text{amb}} = 25^\circ\text{C}$.
- For I/O ports, the parameter I_{IH} and I_{IL} include the off-state current.
- The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

AC ELECTRICAL CHARACTERISTICS

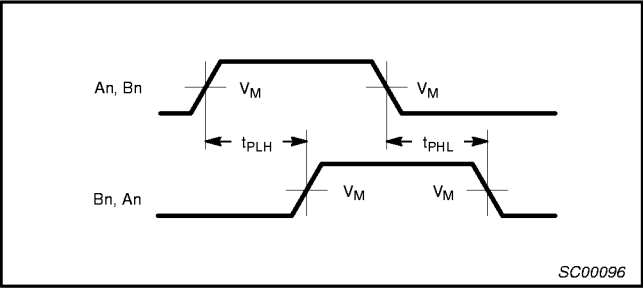
SYMBOL	PARAMETER	TEST CONDITION	LIMITS		UNIT
			$T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = +5.0V \pm 10\%$ $C_L = 50pF, R_L = 500\Omega$		
			MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay An to Bn, Bn to An	Waveform 1	2.0 2.0	10.0 10.0	ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	3.0 3.0	20.0 20.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 4.0	10.0 15.0	ns

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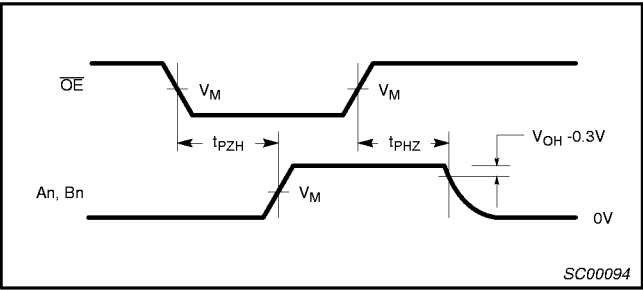
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AC WAVEFORMS

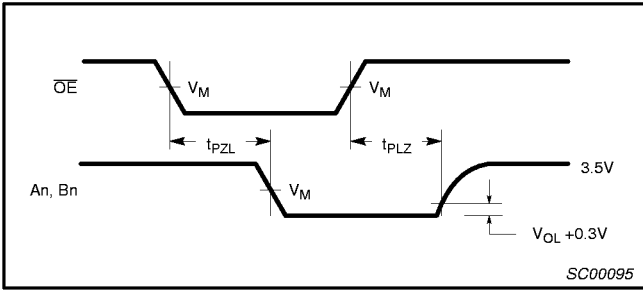
For all waveforms, $V_M = 1.3V$.



Waveform 1. Propagation Delay for Non-inverting Outputs

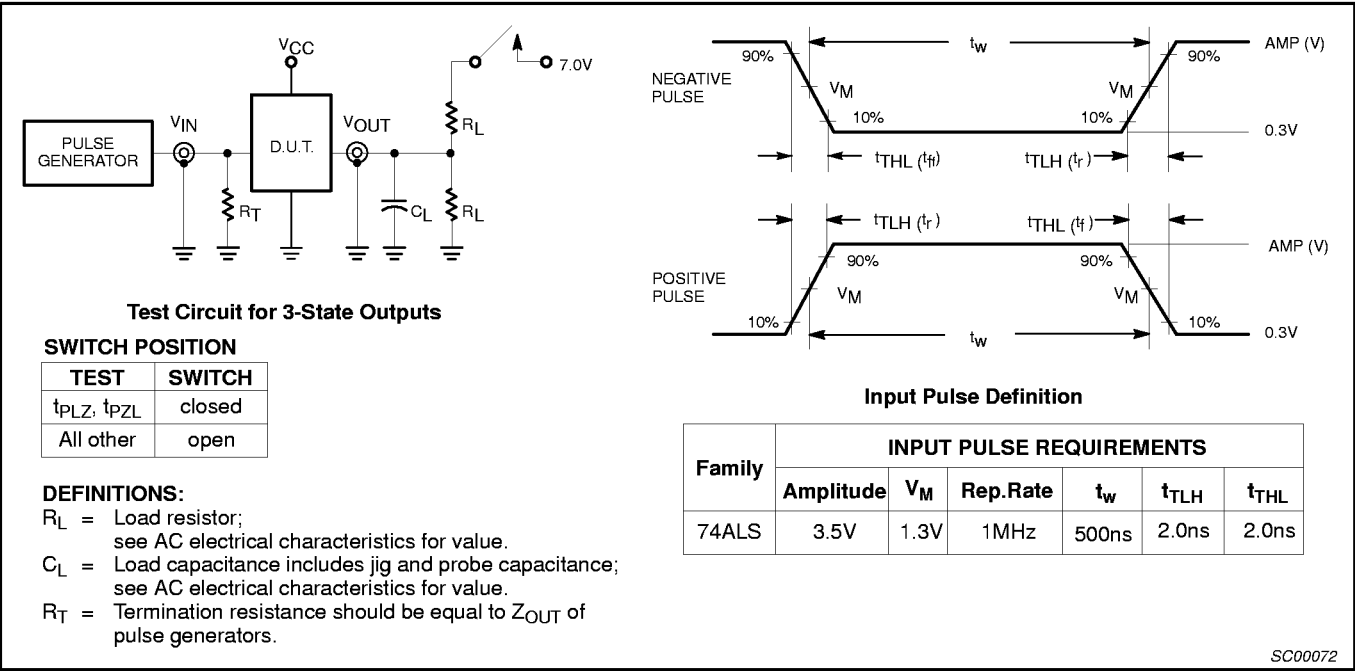


Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

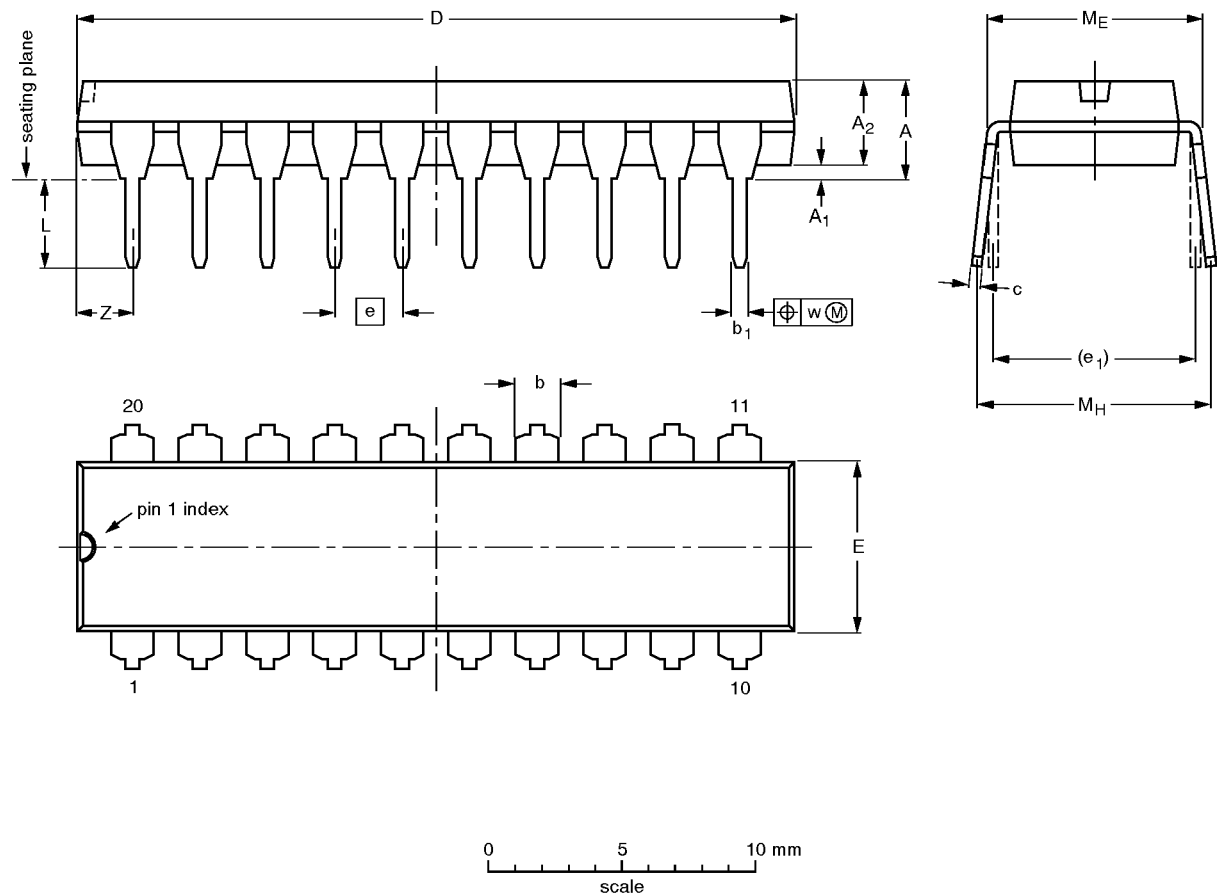


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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

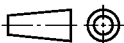


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

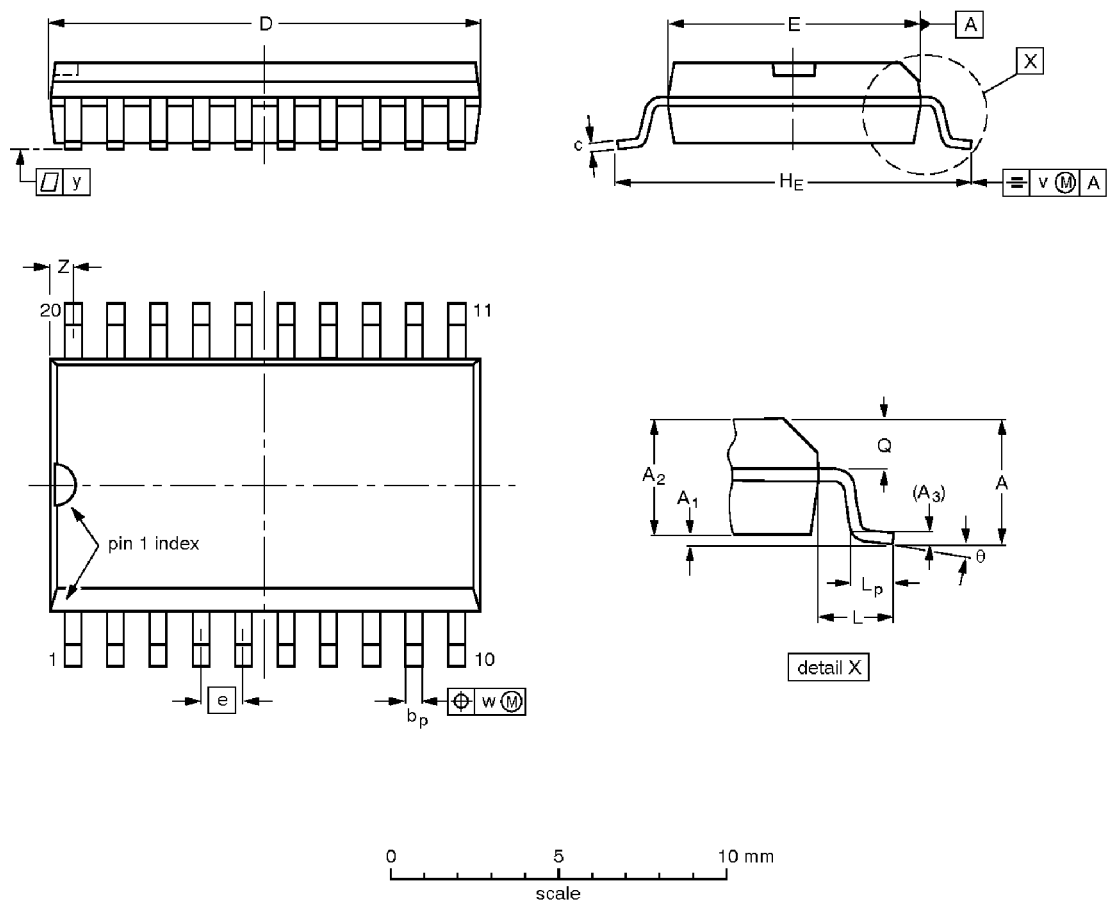
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

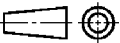


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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