

1.1 Scope.

This specification covers the detail requirements for a complete 12-bit, voltage output, D/A converter (DACPORT®) with output amplifier and Zener voltage reference on a monolithic chip.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7245AT(X)/883B
-2	AD7248AT(Y)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	(Y)	Package	Description
Q		Q-24	24-Pin Cerdip
E		E-28A	28-Pin LCC
	Q	Q-20	20-Pin Cerdip

1.3 Absolute Maximum Ratings.

Positive Supply Voltage (V_{DD}) to AGND	-0.3 V to +17.0 V
Positive Supply Voltage (V_{DD}) to DGND	-0.3 V to +17.0 V
V_{DD} to V_{SS}	+0.3 V to +34 V
AGND to DGND	0.3 V to V_{DD}
Digital Input Voltage to DGND	-0.3 V to $V_{DD} + 0.3$ V
V_{OUT} to AGND	V_{SS} to V_{DD}
V_{OUT} to V_{SS}	0 V to +24 V
V_{OUT} to V_{DD}	-32 V to 0 V
Voltage Reference Output (REF OUT) to AGND	0 V to V_{DD}
Power Dissipation to +75°C	450 mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

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AD7245A/AD7248A—SPECIFICATIONS

Table 1. Electrical Performance Characteristics (Dual Supply)

Test	Symbol	Device	Limits		Sub Groups	Test Condition ¹ ($-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$ unless otherwise noted)	Unit
			Min	Max			
Resolution	RES	-1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	-1, 2	-0.75	+0.75	1, 2, 3	$V_{DD} = +11.4\text{ V to }+15.75\text{ V}$ $V_{SS} = -11.4\text{ V to }-15.75\text{ V}$	LSB
Differential Nonlinearity	DNL	-1, 2	-1	+1	1, 2, 3	Guaranteed Monotonic	LSB
Bipolar Offset Error		-1, 2	2	2	1		LSB
			4	4	2, 3		
DAC Gain Error ²	GE	-1, 2	-2	+2	1, 2, 3		LSB
Full-Scale Output Voltage Error ³	V_{OUTE}	-1, 2	-0.2	+0.2	1	$V_{DD} = +12\text{ V and }+15\text{ V}$ $V_{SS} = -12\text{ V and }-15\text{ V}$	% FSR
			-0.6	+0.6	2, 3		
Δ Full Scale/ ΔV_{DD}		-1, 2	-0.06	+0.06	1	$V_{DD} \approx \pm 5\%$	% FSR/V
Δ Full Scale/ ΔV_{SS}		-1, 2	-0.01	+0.01	1		% FSR/V
Δ Offset/ ΔV_{DD}		-1, 2	-2	+2	1, 2, 3	$V_{DD} = \pm 5\%$	mV
Δ Offset/ ΔV_{SS}		-1, 2	-1	+1	1, 2, 3	$V_{SS} = \pm 5\%$	mV
Reference Output		-1, 2	4.99	5.01	1	$V_{DD} = +12\text{ V and }+15\text{ V}$ $V_{SS} = -12\text{ V and }-15\text{ V}$	V
Δ Reference/ ΔV_{DD}		-1, 2		6	1	$V_{DD} = \pm 5\%$	mV/V
Reference Load Sensitivity		-1, 2	-1.5	+1.5	1, 2, 3	Reference Load Current Change (0 μA –100 μA). Not Including R_{OFS} Current	mV
Digital Input High Voltage	V_{INH}	-1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V_{INL}	-1, 2		0.8	1, 2, 3		V
Digital Input Current for Data Inputs	I_{IN}	-1, 2	-10	+10	1, 2, 3	$V_{IN} = 0$ or V_{DD}	μA
Digital Input High for Control Inputs ⁴	I_{INH}	-1, 2	-1	+1	1	$V_{IN} = V_{DD}$	μA
			-10	+10	2, 3		
Digital Input Low for Control Inputs	I_{INL}	-1, 2		150	1	$V_{IN} = 0\text{ V}$	μA
				200	2, 3		
Digital Input Capacitance	C_{IN}	-1, 2		8	4		pF
Output Range Resistor	R_{OUT}	-1, 2	15	30	1, 2, 3		k Ω
Output Ranges ⁵		-1, 2	0	+5	1, 2, 3	Pin Strappable Minimum Load Resistance Is 2 k Ω to GND	V
			0	+10			
			-5	+5			
Power Supply Current	I_{DD}	-1, 2		12	1, 2, 3	Output Unloaded	mA
	I_{SS}			5			
Output Voltage Settling Positive and Negative Full-Scale Change ⁶	t_{SL}	-1, 2		10	13 ⁷	$T_0 \pm 0.5\text{ LSB}$, $R_L = 2\text{ k}\Omega$	μs

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Test	Symbol	Device	Limits		Sub Groups	Test Condition ¹ (-55°C ≤ T _C ≤ +125°C unless otherwise noted)	Unit
			Min	Max			
Output Voltage Slew Rate	SR	-1, 2	1.5		13, 14, 15 ⁷		V/μs
Chip Select Pulse Width	t ₁	-1, 2	100		9, 10, 11		ns
Write Pulse Width	t ₂	-1, 2	80		9, 10, 11		ns
			100				
Chip Select to Write Setup	t ₃	-1, 2	0		9, 10, 11		ns
Chip Select to Write Hold	t ₄	-1, 2	0		9, 10, 11		ns
Data Valid to Write Setup Time	t ₅	-1, 2	80		9, 10, 11		ns
Data Valid to Write Hold Time	t ₆	-1, 2	10		9, 10, 11		ns
Load DAC Pulse Width	t ₇	-1, 2	100		9, 10, 11		ns
Clear Pulse Width	t ₈	-1, 2	100		9, 10, 11		ns

NOTES

¹Dual Supply: V_{DD} = +11.4 V to +15.75 V; V_{SS} = -11.4 V to -15.75 V; AGND = DGND = 0 V; R_L = 2 kΩ to GND; C_L = 100 pF to GND. REF unloaded unless otherwise noted.

²This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

³This error is calculated with respect to an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full-scale temperature coefficient is ±30 ppm of FSSR/°C.

⁴Control Inputs are CS, WR, LDAC and CLR for Device 1 and CSMB, CSLOSB, WR and LDAC for Device 2.

⁵0 V to +10 V applies to V_{DD} = +15 V ± 5% only, and V_{SS} = -15 V ± 5%.

⁶For positive full-scale change, DAC register loaded all 0s to all 1s. For negative full-scale change, DAC register loaded all 1s to all 0s.

⁷Special Subgroups 13, 14, 15 (as referenced) shall be measured only for the initial test, or after process or design changes which may affect the parameter in those subgroups. Subgroup 13 is +25°C tests, Subgroup 14 is +125°C tests and Subgroup 15 is -25°C tests.

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AD7245A/AD7248A—SPECIFICATIONS

Table 2. Electrical Performance Characteristics (Single Supply)

Test	Symbol	Device	Limits		Sub Groups	Test Condition ¹ (-55°C ≤ T _C ≤ +125°C unless otherwise noted)	Unit
			Min	Max			
Resolution	RES	-1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	-1, 2	-0.75	+0.75	1, 2, 3	V _{DD} = +11.4 V to +15.75 V	LSB
Differential Nonlinearity	DNL	-1, 2	-1	+1	1, 2, 3	Guaranteed Monotonic	LSB
Unipolar Offset Error		-1, 2	2	2	1		LSB
			4	4	2, 3		
DAC Gain Error ²	GE	-1, 2	-2	+2	1, 2, 3		LSB
Full-Scale Output Voltage Error ³	V _{OUT} E	-1, 2	-0.2	+0.2	1	V _{DD} = +12 V and +15 V	% FSR
			-0.6	+0.6	2, 3		
ΔFull Scale/ΔV _{DD}		-1, 2	-0.06	+0.06	1	V _{DD} = +5%	% FSR/V
ΔOffset/ΔV _{DD}		-1, 2	-2	+2	1, 2, 3	V _{DD} = ±5%	mW
Reference Output		-1, 2	4.99	5.01	1	V _{DD} = +12 V and +15 V	V
ΔReference/ΔV _{DD}		-1, 2		6	1	V _{DD} = ±5%	mV/V
Reference Load Sensitivity		-1, 2	-1.5	+1.5	1, 2, 3	Reference Load Current Change (0 μA-100 μA). Not Including R _{OP} S Current	mV
Digital Input High Voltage	V _{INH}	-1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V _{INL}	-1, 2		0.8	1, 2, 3		V
Digital Input Current for Data Inputs	I _{IN}	-1, 2	-1	+1	1	V _{IN} = 0 or V _{DD}	μA
			-10	+10	2, 3		
Digital Input High for Control Inputs ⁴	I _{INH}	-1, 2	-1	+1	1	V _{IN} = V _{DD}	μA
			-10	+10	2, 3		
Digital Input Low for Control Inputs	I _{INL}	-1, 2		150	1	V _{IN} = 0 V	μA
				200	2, 3		
Digital Input Capacitance	C _{IN}	-1, 2		8	4		pF
					16		
Output Range Resistors	R _{OUT}	-1, 2	15	30	1, 2, 3		kΩ
Output Ranges ⁵		-1, 2	0	+5	1, 2, 3	Pin Strappable Minimum Load Resistance Is 2 kΩ to GND	V
			0	+10			
			-5	+5			
Power Supply Current	I _{DD}	-1, 2		12	1, 2, 3	Output Unloaded	mA
Output Voltage Settling Positive and Negative Full-Scale Change ⁶	t _{SL}	-1, 2		10	13 ⁷	T _O ±0.5 LSB, R _L = 5 kΩ	μs

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Test	Symbol	Device	Limits		Sub Groups	Test Condition ¹ (-55°C ≤ T _C ≤ +125°C unless otherwise noted)	Unit
			Min	Max			
Output Voltage Slew Rate	SR	-1, 2	2		13, 14, 15 ⁷		V/μs
Chip Select Pulse Width	t ₁	-1, 2	100		9, 10, 11		ns
Write Pulse Width	t ₂	-1, 2	100		9, 10, 11		ns
Chip Select to Write Setup	t ₃	-1, 2	0		9, 10, 11		ns
Chip Select to Write Hold	t ₄	-1, 2	0		9, 10, 11		ns
Data Valid to Write Setup Time	t ₅	-1, 2	80		9, 10, 11		ns
Data Valid to Write Hold Time	t ₆	-1, 2	10		9, 10, 11		ns
Load DAC Pulse Width	t ₇	-1, 2	100		9, 10, 11		ns
Clear Pulse Width	t ₈	-1, 2	100		9, 10, 11		ns

NOTES

¹Single Supply: V_{DD} = +15 V ± 5%; V_{SS} = AGND = DGND = 0 V.

²This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.

³This error is calculated with respect to an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full-scale temperature coefficient is ± 30 ppm of FSSR/°C.

⁴Control Inputs are CS, WR, LDAC and CLR for Device 1 and CSMB, CSLOSB, WR and LDAC for Device 2.

⁵0 V to +10 V Applies to V_{DD} = +15 V ± 5% only, and V_{SS} = -15 V ± 5%.

⁶For positive full-scale change, DAC register loaded all 0s to all 1s. For negative full-scale change, DAC register loaded all 1s to all 0s.

⁷Special Subgroups 13, 14, 15 (as referenced) shall be measured only for the initial test, or after process or design changes which may affect the parameter in those subgroups. Subgroup 13 is +25°C tests, Subgroup 14 is +125°C tests and Subgroup 15 is -25°C tests.

1.4 Recommended Operating Conditions.

Single Supply

Positive Supply Voltage Range (V_{DD}) +15 V ± 5%

Negative Supply Voltage Range (V_{SS}) 0 V

AGND = DGND 0 V

Dual Supply

Positive Supply Voltage Range (V_{DD}) +12 V to +15 V ± 5%

Negative Supply Voltage Range (V_{SS}) -12 V to -15 V ± 5%

AGND = DGND 0 V

R_L 2 kΩ to GND

C_L 100 pF to GND

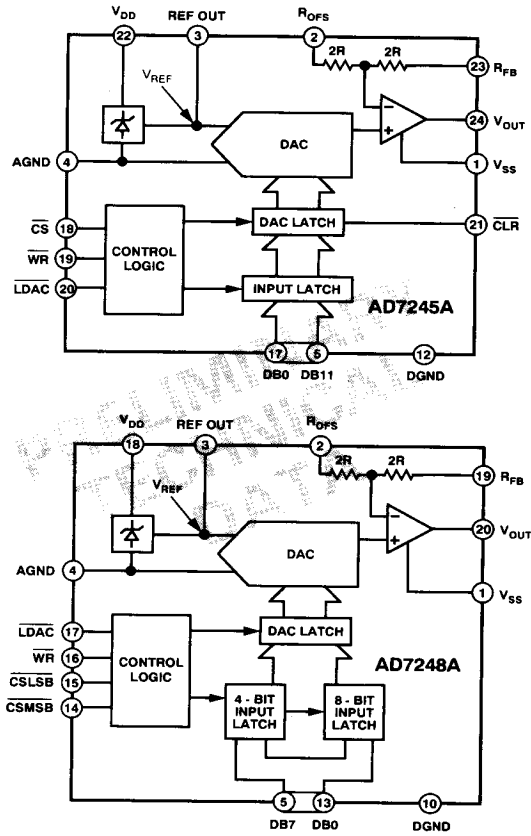
REF OUT Unloaded

Ambient Operating Temperature Range -55°C to +125°C

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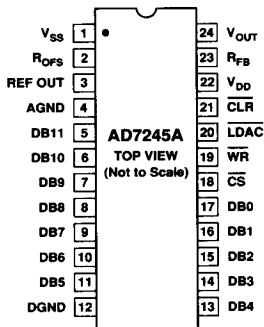
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3.2.1 Functional Block Diagram and Terminal Assignments.

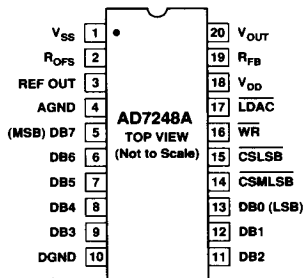


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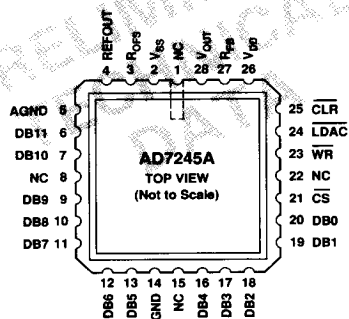
Q-24



Q-20



E-28A



NC = NO CONNECT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

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