Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 5.5 V)**
  - **2.5 V (V_{CC} = 2.5 V to 5.5 V)**
  - **2.0 V (V_{CC} = 1.8 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Three-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **Eight-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages**

3-Wire Serial CMOS E^2PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Description

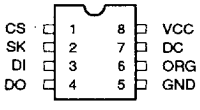
The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial E^2PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of eight bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/57/66 is available in space saving eight-pin PDIP and eight-pin JEDEC and EIAJ SOIC packages.

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

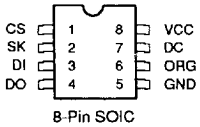
Atmel's E^2PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT93C46/56/57/66 is available in 5.0 V ± 10%, 2.7 V to 5.5 V, 2.5 V to 5.5 V, and 1.8 V to 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect

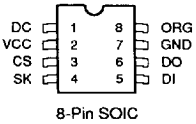


8-Pin PDIP



8-Pin SOIC

Rotated (R)
(1K JEDEC Only)



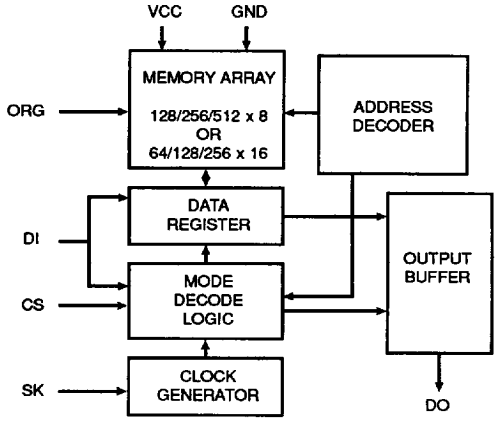
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0 V

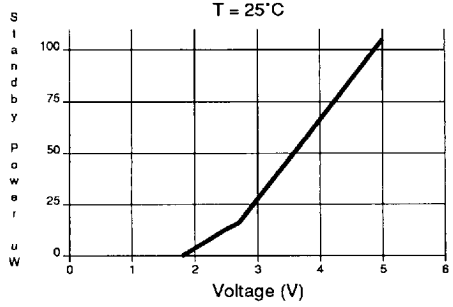
Note: 1. This parameter is characterized and is not 100% tested.

D.C. Characteristics

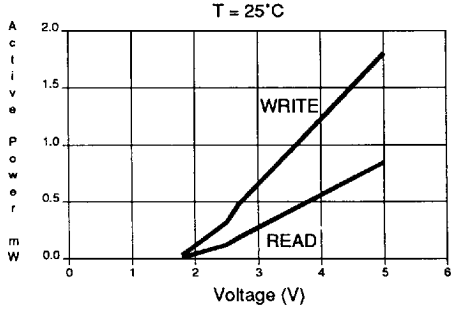
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +1.8 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1} (1)	Supply Voltage			1.8	5.0	5.5	V
V_{CC2}	Supply Voltage			2.5	5.0	5.5	V
V_{CC3}	Supply Voltage			2.7	5.0	5.5	V
V_{CC4}	Supply Voltage			4.5	5.0	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0 V	READ at 1.0 MHz		0.2	0.5	mA
			WRITE at 1.0 MHz		0.4	1.0	mA
I_{SB1} (1)	Standby Current	V_{CC} = 1.8 V	CS = 0 V		0.0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5 V	CS = 0 V		5.0	7.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7 V	CS = 0 V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0 V	CS = 0 V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
V_{IL1} (2) V_{IH1} (2)	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		-0.1 2.0		0.8 V_{CC}+1	V
V_{IL2} (2) V_{IH2} (2)	Input Low Voltage Input High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V		0.0 1.4		0.4 V_{CC}+1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V		 V_{CC}-0.2		0.2	V

Typical Standby Power vs. Voltage(3)



Typical Active Power vs. Voltage(3)



Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guarenteed by test.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency		4.5 V ≤ Vcc ≤ 5.5 V	0		1	MHz
			2.7 V ≤ Vcc ≤ 5.5 V	0		1	
			2.5 V ≤ Vcc ≤ 5.5 V	0		0.5	
			1.8 V ≤ Vcc ≤ 5.5 V	0		0.25	
t_{SKH}	SK High Time		4.5 V ≤ Vcc ≤ 5.5 V	250			ns
			2.7 V ≤ Vcc ≤ 5.5 V	250			
			2.5 V ≤ Vcc ≤ 5.5 V	500			
			1.8 V ≤ Vcc ≤ 5.5 V	1000			
t_{SKL}	SK Low Time		4.5 V ≤ Vcc ≤ 5.5 V	250			ns
			2.7 V ≤ Vcc ≤ 5.5 V	250			
			2.5 V ≤ Vcc ≤ 5.5 V	500			
			1.8 V ≤ Vcc ≤ 5.5 V	1000			
t_{CS}	Minimum CS Low Time		4.5 V ≤ Vcc ≤ 5.5 V	250			ns
			2.7 V ≤ Vcc ≤ 5.5 V	250			
			2.5 V ≤ Vcc ≤ 5.5 V	500			
			1.8 V ≤ Vcc ≤ 5.5 V	1000			
t_{CSS}	CS Setup Time	Relative to SK	4.5 V ≤ Vcc ≤ 5.5 V	50			ns
			2.7 V ≤ Vcc ≤ 5.5 V	50			
			2.5 V ≤ Vcc ≤ 5.5 V	100			
			1.8 V ≤ Vcc ≤ 5.5 V	200			
t_{DIS}	DI Setup Time	Relative to SK	4.5 V ≤ Vcc ≤ 5.5 V	100			ns
			2.7 V ≤ Vcc ≤ 5.5 V	100			
			2.5 V ≤ Vcc ≤ 5.5 V	200			
			1.8 V ≤ Vcc ≤ 5.5 V	400			
t_{CSH}	CS Hold Time	Relative to SK		0			ns
t_{DIH}	DI Hold Time	Relative to SK	4.5 V ≤ Vcc ≤ 5.5 V	100			ns
			2.7 V ≤ Vcc ≤ 5.5 V	100			
			2.5 V ≤ Vcc ≤ 5.5 V	200			
			1.8 V ≤ Vcc ≤ 5.5 V	400			
t_{PD1}	Output Delay to '1'	AC Test	4.5 V ≤ Vcc ≤ 5.5 V			250	ns
			2.7 V ≤ Vcc ≤ 5.5 V			250	
			2.5 V ≤ Vcc ≤ 5.5 V			500	
			1.8 V ≤ Vcc ≤ 5.5 V			1000	
t_{PD0}	Output Delay to '0'	AC Test	4.5 V ≤ Vcc ≤ 5.5 V			250	ns
			2.7 V ≤ Vcc ≤ 5.5 V			250	
			2.5 V ≤ Vcc ≤ 5.5 V			500	
			1.8 V ≤ Vcc ≤ 5.5 V			1000	
t_{SV}	CS to Status Valid	AC Test	4.5 V ≤ Vcc ≤ 5.5 V			250	ns
			2.7 V ≤ Vcc ≤ 5.5 V			250	
			2.5 V ≤ Vcc ≤ 5.5 V			500	
			1.8 V ≤ Vcc ≤ 5.5 V			1000	
t_{DF}	CS to DO in High Impedance	AC Test CS = V_{IL}	4.5 V ≤ Vcc ≤ 5.5 V			100	ns
			2.7 V ≤ Vcc ≤ 5.5 V			100	
			2.5 V ≤ Vcc ≤ 5.5 V			200	
			1.8 V ≤ Vcc ≤ 5.5 V			400	
t_{WP}	Write Cycle Time					10	ms
	Endurance	Number of Data Changes per Bit			100,000		Cycles

Instruction Set for the AT93C46

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A_6-A_0	A_5-A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXX	01XXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions.

Instruction Set for the AT93C57

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_7-A_0	A_6-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX	11XXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_7-A_0	A_6-A_0			Erase memory location A_n - A_0.
WRITE	1	01	A_7-A_0	A_6-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXX	10XXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXXX	01XXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	00	00XXXXXX	00XXXXX			Disables all programming instructions.

Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A_8-A_0	A_7-A_0			Erases memory location A_n - A_0.
WRITE	1	01	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	00	10XXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	00	01XXXXXXX	01XXXXXX	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXX	00XXXXXX			Disables all programming instructions.

Functional Description

The AT93C46/56/57/66 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY / BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '1' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

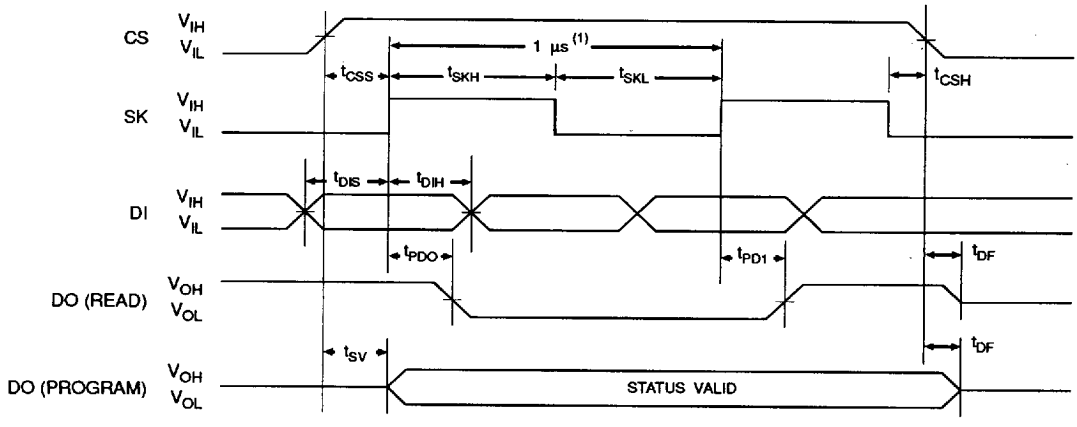
ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The ERAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (t_{CS}). The WRAL instruction is valid only at $V_{CC} = 5.0\ V \pm 10\%$.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Timing Diagrams

Synchronous Data Timing



Note: 1. This is the minimum SK period.

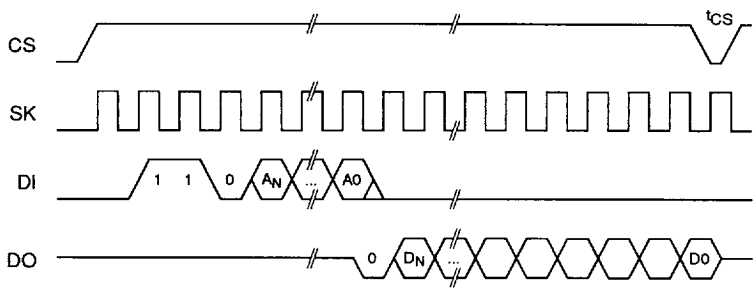
Organization Key for Timing Diagrams

I/O	Density 1K		Density 2K		Density 4K	
	x 8	x 16	x 8	x 16	x 8	x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

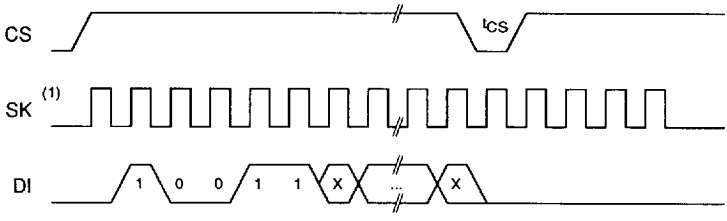
2

Timing Diagrams (Continued)

READ Timing

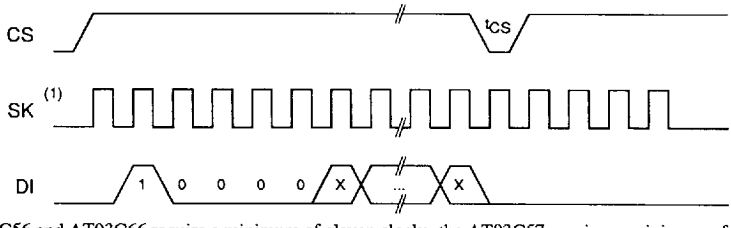


EWEN Timing



Note: 1. The AT93C56 and AT93C66 require a minimum of eleven clocks, the AT93C57 requires a minimum of ten clocks, and the AT93C46 requires a minimum of nine clock cycles.

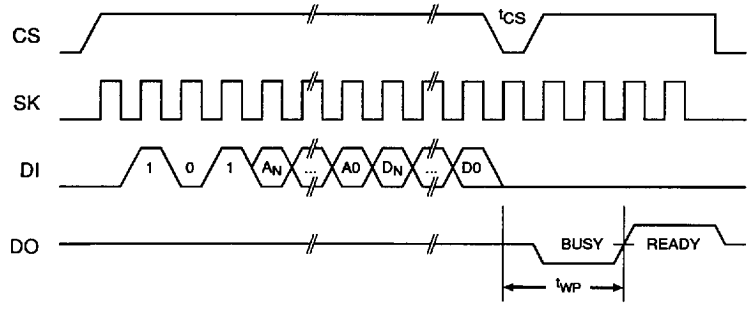
EWDS Timing



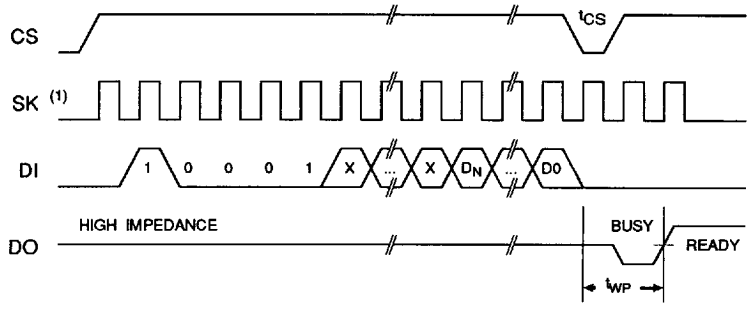
Note: 1. The AT93C56 and AT93C66 require a minimum of eleven clocks, the AT93C57 requires a minimum of ten clocks, and the AT93C46 requires a minimum of nine clock cycles.

Timing Diagrams (Continued)

WRITE Timing



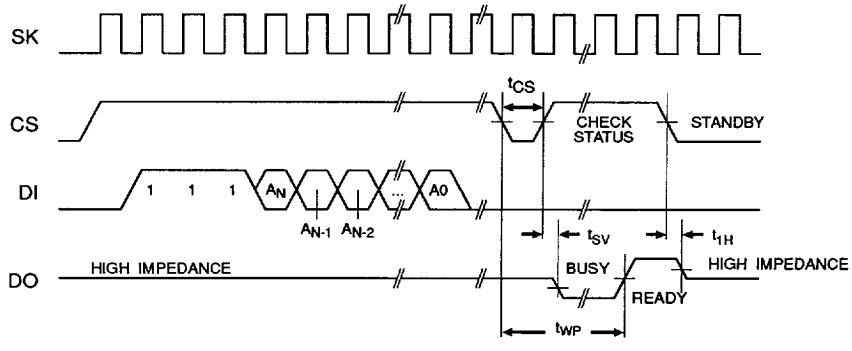
WRAL Timing [2]



Notes: 1. The AT93C56 and AT93C66 require a minimum of eleven clocks, the AT93C57 requires a minimum of ten clocks, and the AT93C46 requires a minimum of nine clock cycles.

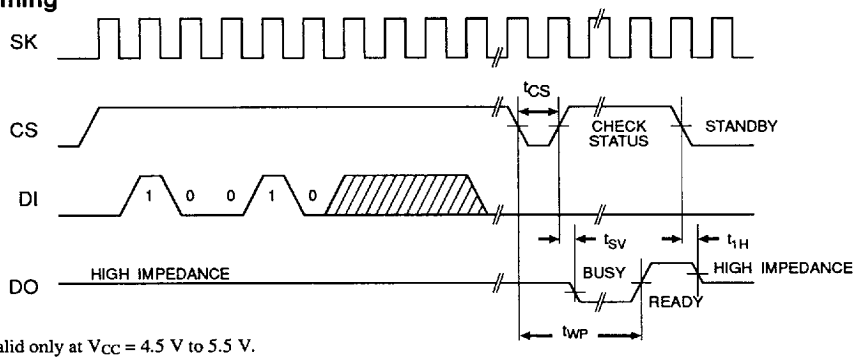
2. Valid only at V_{CC} = 4.5 V to 5.5 V.

ERASE Timing



Timing Diagrams (Continued)

TERAL Timing [1]



Note: 1. Valid only at V_{CC} = 4.5 V to 5.5 V.

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C46-10PC AT93C46-10SC AT93C46R-10SC AT93C46W-10SC	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C46-10PC-2.7 AT93C46-10SC-2.7 AT93C46R-10SC-2.7 AT93C46W-10SC-2.7	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C46-10PC-2.5 AT93C46-10SC-2.5 AT93C46R-10SC-2.5 AT93C46W-10SC-2.5	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C46-10PC-1.8 AT93C46-10SC-1.8 AT93C46R-10SC-1.8 AT93C46W-10SC-1.8	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C46-10PI AT93C46-10SI AT93C46R-10SI AT93C46W-10SI	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C46-10PI-2.7 AT93C46-10SI-2.7 AT93C46R-10SI-2.7 AT93C46W-10SI-2.7	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C46-10PI-2.5 AT93C46-10SI-2.5 AT93C46R-10SI-2.5 AT93C46W-10SI-2.5	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C46-10PI-1.8 AT93C46-10SI-1.8 AT93C46R-10SI-1.8 AT93C46W-10SI-1.8	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C46-10PM	8P3	Military (-55°C to 125°C)

Ordering Information

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)
R	Rotated Pinout

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C56-10PC AT93C56-10SC AT93C56W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C56-10PC-2.7 AT93C56-10SC-2.7 AT93C56W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C56-10PC-2.5 AT93C56-10SC-2.5 AT93C56W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C56-10PC-1.8 AT93C56-10SC-1.8 AT93C56W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C56-10PI AT93C56-10SI AT93C56W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C56-10PI-2.7 AT93C56-10SI-2.7 AT93C56W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C56-10PI-2.5 AT93C56-10SI-2.5 AT93C56W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C56-10PI-1.8 AT93C56-10SI-1.8 AT93C56W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C56-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8S2	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)
-2.5	Low Voltage (2.5 V to 5.5 V)
-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C57-10PC AT93C57-10SC AT93C57W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C57-10PC-2.7 AT93C57-10SC-2.7 AT93C57W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C57-10PC-2.5 AT93C57-10SC-2.5 AT93C57W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C57-10PC-1.8 AT93C57-10SC-1.8 AT93C57W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C57-10PI AT93C57-10SI AT93C57W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C57-10PI-2.7 AT93C57-10SI-2.7 AT93C57W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C57-10PI-2.5 AT93C57-10SI-2.5 AT93C57W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C57-10PI-1.8 AT93C57-10SI-1.8 AT93C57W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C57-10PM	8P3	Military (-55°C to 125°C)

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Blank	Standard Device (4.5 V to 5.5 V)
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-1.8	Low Voltage (1.8 V to 5.5 V)

Ordering Information

t_{WP} (ms)	I_{CC} (max) (µA)	I_{SB} (max) (µA)	f_{MAX} (kHz)	Ordering Code	Package	Operation Range
10	1000	30.0	1000	AT93C66-10PC AT93C66-10SC AT93C66W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	400	10.0	1000	AT93C66-10PC-2.7 AT93C66-10SC-2.7 AT93C66W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	300	7.0	500	AT93C66-10PC-2.5 AT93C66-10SC-2.5 AT93C66W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	40	0.1	250	AT93C66-10PC-1.8 AT93C66-10SC-1.8 AT93C66W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	1000	30.0	1000	AT93C66-10PI AT93C66-10SI AT93C66W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	400	10.0	1000	AT93C66-10PI-2.7 AT93C66-10SI-2.7 AT93C66W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	300	7.0	500	AT93C66-10PI-2.5 AT93C66-10SI-2.5 AT93C66W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	40	0.1	250	AT93C66-10PI-1.8 AT93C66-10SI-1.8 AT93C66W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	1000	30.0	1000	AT93C66-10PM	8P3	Military (-55°C to 125°C)

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