

PowerMOS transistor

BUK457-600B

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and AC/DC converters, and in general purpose switching applications.

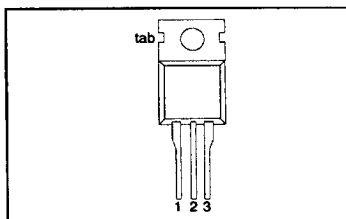
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (DC)	7.1	A
P_{tot}	Total power dissipation	150	W
$R_{DS(ON)}$	Drain-source on-state resistance	1.2	Ω

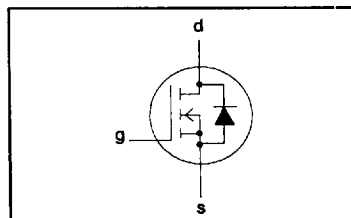
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	600	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	600	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	$T_{mb} = 25^\circ\text{C}$	-	7.1	A
I_D	Drain current (DC)	$T_{mb} = 100^\circ\text{C}$	-	4.5	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25^\circ\text{C}$	-	28	A
P_{tot}	Total power dissipation	$T_{mb} = 25^\circ\text{C}$	-	150	W
T_{stg}	Storage temperature	-	-55	150	$^\circ\text{C}$
T_j	Junction Temperature	-	-	150	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th j-mb}$	Thermal resistance junction to mounting base		-	-	0.83	K/W
$R_{th j-a}$	Thermal resistance junction to ambient		-	60	-	K/W

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STATIC CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}$	600	-	-	V
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 600\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	2	20	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 600\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 30\text{ V}; V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 6.5\text{ A}$	-	1.0	1.2	Ω

DYNAMIC CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 6.5\text{ A}$	5.0	8.0	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1500	1800	pF
C_{oss}	Output capacitance		-	170	270	pF
C_{rss}	Feedback capacitance		-	70	120	pF
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 2.8\text{ A};$ $V_{GS} = 10\text{ V}; R_{GS} = 50\text{ }\Omega;$ $R_{gen} = 50\text{ }\Omega$	-	20	40	ns
t_r	Turn-on rise time		-	60	90	ns
$t_{d\text{ off}}$	Turn-off delay time		-	200	250	ns
t_f	Turn-off fall time		-	75	90	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

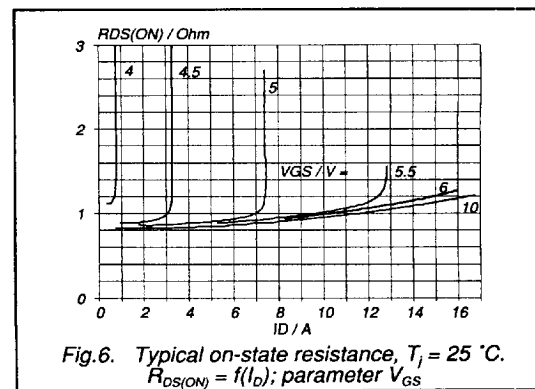
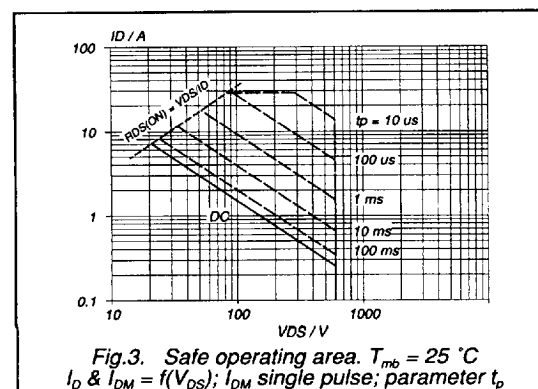
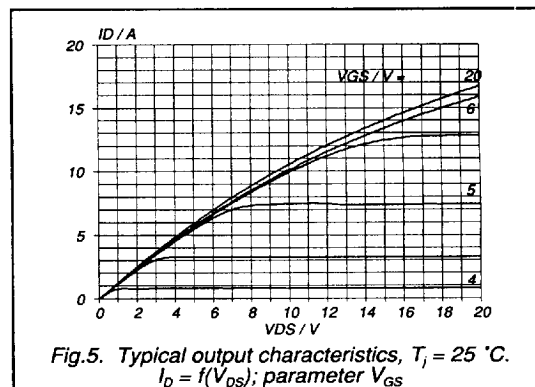
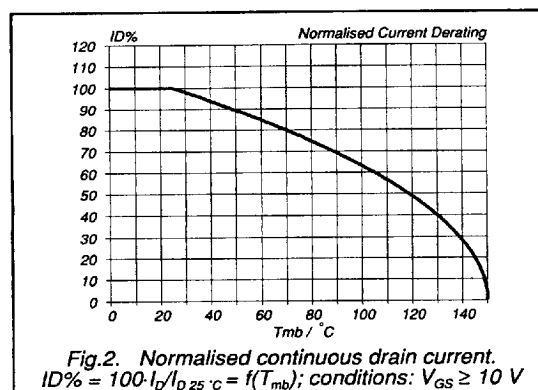
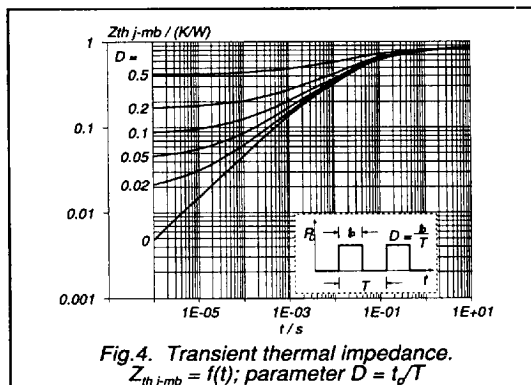
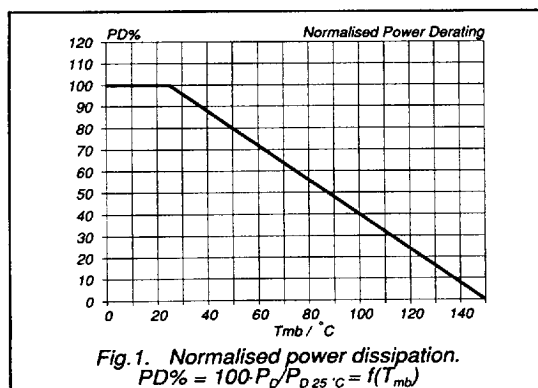
REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_{mb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	8	A
I_{DRM}	Pulsed reverse drain current	-	-	-	32	A
V_{SD}	Diode forward voltage	$I_F = 8\text{ A}; V_{GS} = 0\text{ V}$	-	1.1	1.4	V
t_r	Reverse recovery time	$I_F = 8\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s};$ $V_{GS} = 0\text{ V}; V_R = 100\text{ V}$	-	500	-	ns
Q_{rr}	Reverse recovery charge		-	6.0	-	μC

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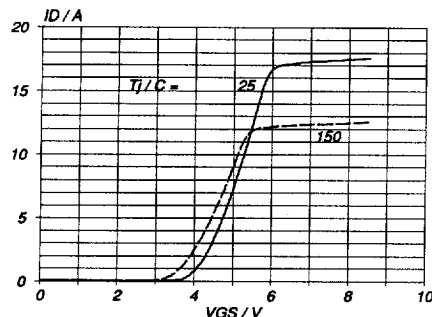


Fig. 7. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

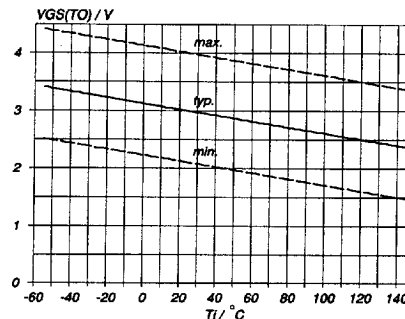


Fig. 10. Gate threshold voltage.
 $V_{GS(T0)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

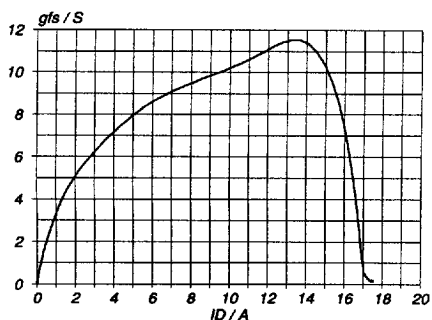


Fig. 8. Typical transconductance, $T_j = 25\text{ °C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

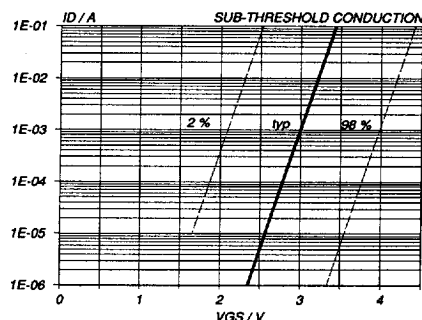


Fig. 11. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25\text{ °C}$; $V_{DS} = V_{GS}$

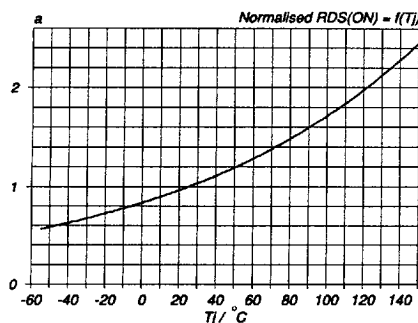


Fig. 9. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ °C}} = f(T_j)$; $I_D = 6.5\text{ A}$; $V_{GS} = 10\text{ V}$

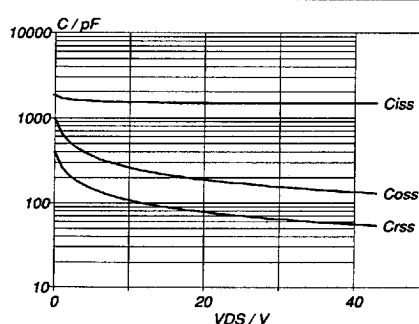


Fig. 12. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

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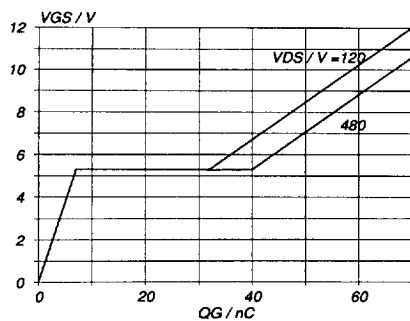


Fig. 13. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 8\text{ A}$; parameter V_{DS}

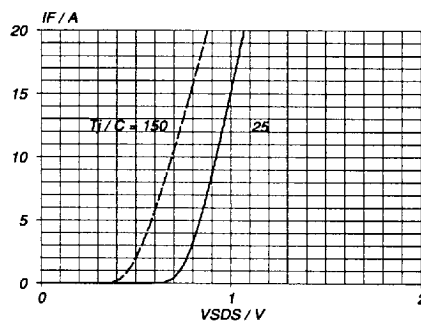


Fig. 14. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j