Marconi
Electronic Devices

3μm CELLSOS DESIGN SYSTEM

FEATURES

* **Silicon on sapphire oxide isolated CMOS technology**
* **3 micron design rules**
* **Typical gate delays 2nS — toggle rates of 65 MHz and greater achieved**
* **Radiation hard**
* **Latch-up free**
* **2μW/MHz power dissipation per active gate**
* **Comprehensive CAD design and support system**

SYSTEM DESCRIPTION

Marconi's SILICON ON SAPPHIRE process provides significant advantages over other CMOS technologies. The absence of the bulk silicon substrate reduces parasitic capacitances, giving an improvement in speed and a reduction in power consumption. The use of a self-aligning silicon gate process gives further improvements in both of the above parameters and achieves higher packing densities. The sapphire substrate also removes the risk of 'latch-up' allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation tolerance.

The cells in the core area are designed to have a common cell height, the cell width being dependent on the complexity of the cell. The cell width is the minimum possible, though this is, in some cases, increased to achieve adequate drive capability. The cells and the interconnect between cells are placed on a regular grid in such a way that design rule infringement is impossible.

A range of standard input and output buffers are available for use in the peripheral areas. These, and the interconnect from them to the core area, are placed on the same grid as the core area for the same reason.

The cell layout method eliminates design faults, giving a much better chance of first time success than with other design methodologies which involve significant human judgement. However, the normal constraints of logic design apply. Circuits must be designed with due attention to race hazards, timing considerations, and testability. Good digital design technique combined with the use of our simulation software and cell libraries gives the highest probability of first time design success.

Special cells may be configured by Marconi for non-standard functions. For Example, higher output current buffers and special input cells can be designed on request. These are not part of the current characterised cell library and naturally would require both additional funding and longer prototype and preproduction scheduling

Marconi's 'CELLSOS' system runs on Silvar Lisco's CAL-MP layout software with CASS or Mentor Graphic's IDEA series for schematic capture. Simulation is performed using Genrads's HILO-2. This powerful software suite together with Marconi cell libraries can be supplied through Marconi for customers who wish to design their own circuits.

CAL-MP and CASS are trademarks of Silvar Lisco Inc.
IDEA series is a trademark of Mentor Graphics Corporation
HILO is a trademark of GenRad Ltd.

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Integrated Circuits

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ABSOLUTE MAXIMUM RATINGS

Supply voltage	Vdd	12	volts
Positive voltage on any pin		Vdd + 0.3	volts
Negative voltage on any pin		Vss − 0.3	volts
Current through any I/O pin		±10	mA
Power dissipation		Package dependent	

Note: Exceeding the 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only and functional performance under these conditions for extended periods may adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Operating supply voltage	3V − 8V	
Storage temperature*	−65°C to 150°C	
Operating ambient temperature*		
Military	−55°C to +125°C	*Package dependent
Industrial	−40°C to +85°C	
Commercial	0°C to +70°C	

D.C. ELECTRICAL CHARACTERISTICS at 5V and 25°C

Symbol	Parameter	Limit	
Iin	Input leakage	1.0μA/gate	Typically <100nA
Idd	Static supply current		Typically <100nA/gate
STANDARD CMOS INPUTS			
Vih	Input high volts	3.5V min	
Vil	Input low volts	1.5V max	
STANDARD TTL INPUTS			
Vih	Input high volts	2.0V min	
Vil	Input low volts	0.8V max	
STANDARD CMOS OUTPUTS			
Voh	Output high volts	4.5V min	R_L = 50 Kohms C_L = 50 pF
Vol	Output low volts	0.5V max	R_L = 50 Kohms C_L = 50 pF
STANDARD TTL OUTPUTS			
Voh	Output high volts	2.4V min	at Ioh = −1mA
Vol	Output low volts	0.4V max	at Iol = 2mA

Note: The above data is for Marconi standard input and output cells. For buffered inputs, Schmitt inputs and other 'special cells' please refer to our CELLSOS design manual.

A.C. ELECTRICAL CHARACTERISTICS at 5V and 25°C

Cell name	Function		O/P edge	Inherent delay	Per 1pF load
CIO2	CMOS input/output		rising	2.0nS	0.5nS
			falling	2.5nS	0.5nS
NOR2	2 input NOR		rising	2.0nS	15.0nS
			falling	2.0nS	10.0nS
RDT	Reset D type	CK - QB	rising	6.0nS	11.0nS
			falling	9.0nS	20.0nS
	Data set up time	5.0nS			
	Data hold time	5.0nS			

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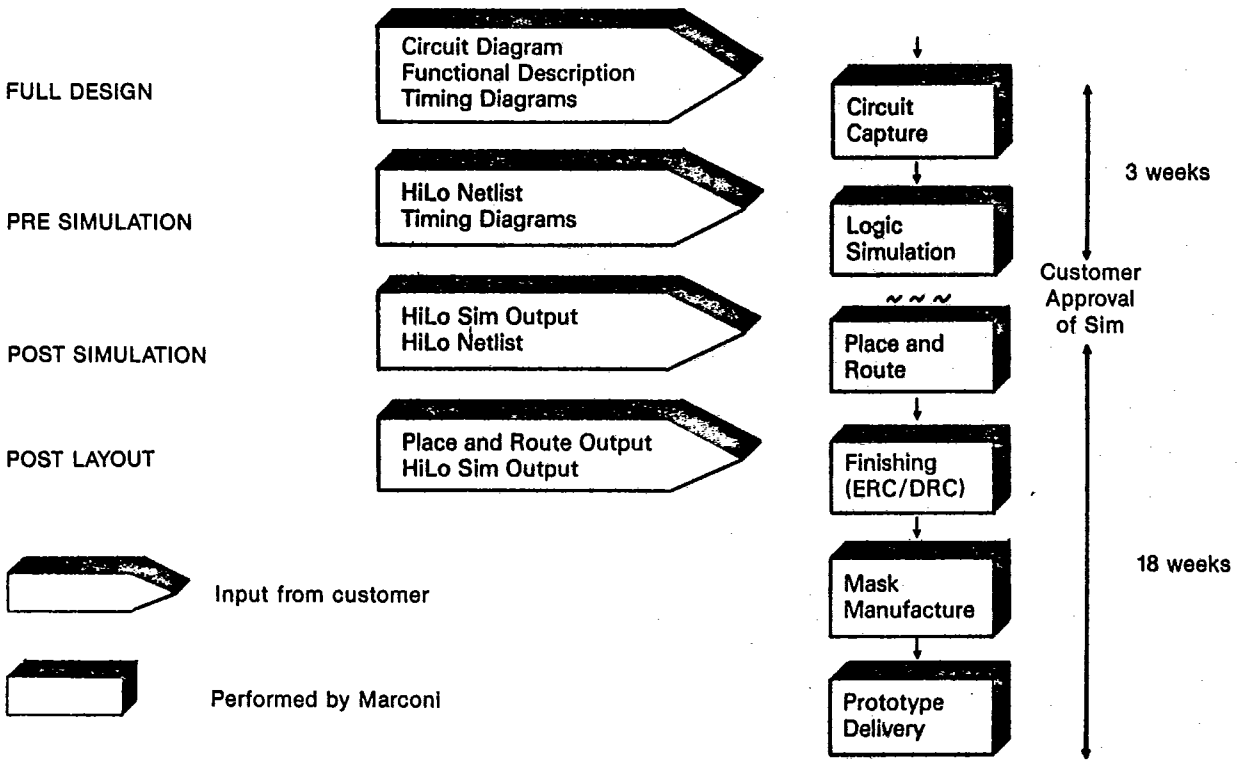
DEVELOPMENT INTERFACES



For further more detailed information on Marconi's design interfaces and CAD software please refer to our semi-custom CAD data sheet.

PACKAGE OPTIONS AVAILABLE AS STANDARD

CERAMIC DIL	14	16	18	20	24	28	40	48	
CERDIP	14	16	18	20	24	28	40	48	
PLASTIC DIL	14	16	18	20	24	28	40		
PLASTIC SO	16L								
PIN GRID ARRAY	68	84	120	144					
CERAMIC LCC	20	28	[40]	44	[48]	68	84		[ ] have 0.040" centers, others have 0.050"
PLASTIC LCC	28	44	68	84					
EPIC (PCB) LCC	40								
CERQUAD	44	68	84						

Marconi has a wide range of packages offered as standard as shown above. If, however, you have a packaging requirement not on this table a Marconi applications engineer will be happy to discuss your needs.

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CELL LIBRARY QUICK GUIDE

Name	Description	Cell width
COMBINATION GATES		
INVB	Fast inverter	6
INV	Inverter	3
BUFF	Non-inverting buffer	8
BUFFB	Double buffer	13
BUFFC	Triple buffer	18
BUFFD	Quad buffer	23
NAND2	2 input NAND	4
NAND3	3 input NAND	5
NAND4	4 input NAND	6
AND2	2 input AND	5
AND3	3 input AND	6
AND4	4 input AND	7
NOR2	2 input NOR	4
NOR3	3 input NOR	5
NOR4	4 input NOR	6
OR2	2 input OR	5
OR3	3 input OR	6
OR4	4 input OR	7
ANDNOR	2+2 input AND/NOR	7
ANDOR	2+2 input AND/OR	9
ORNAND	2+2 input OR/NAND	6
ORAND	2+2 input OR/AND	7
O2NA1	OR2/AND1 invert gate	8
O2A1	OR2/AND1 gate	7
O2NA2	OR2/AND2 invert gate	7
O2A2	OR2/AND2 gate	8
A2NO1	AND2/OR1 invert gate	6
A2O1	AND2/OR1 gate	7
A2NO2	AND2/OR2 invert gate	7
A2O2	AND2/OR2 gate	8
EXNOR	Exclusive NOR	6
EXOR	Exclusive OR	6
SEL2	Select 1 of 2	8
SEL2INV	Select 1 of 2 (inv)	7
ARITHMETIC		
FAD	Full adder	12
SIMPLE LATCHES		
NASR	NAND set-reset latch	5
NOSR	NOR set-reset latch	5
CLOCKED LATCHES		
DL	D-latch	7
DLH	Transparent high level latch	7
RDL	Reset D-latch	8
RDLH	Reset high level D-latch	8

CELL LIBRARY QUICK GUIDE

Name	Description	Cell width
EDGE TRIGGERED LATCHES		
RETS	Edge triggered latch with reset	11
RETSN	Negative edge triggered latch with reset	16
MASTER-SLAVE FLIP-FLOPS		
DT	D-Type	12
D2T	Dual input D-type	16
SDT	Set D-type	15
RDT	Reset D-type	15
SRDT	Set/reset D-type	17
RDTN	Negative edge triggered D-type with reset	16
TOGGLE FLIP-FLOPS		
RTT	Reset T-type	15
STT	Set T-type	15
RTTTOG	Reset T-type with low level toggle enable	18
RTTTOGH	Reset T-type with high level toggle enable	18
BUFFERS		
TTLIN	TTL input buffer	8
TRINVL	Tri-state inverter with low level enable	5
TRIOP	Tri-state I/O buffer	13

INPUT OUTPUT AND PERIPHERAL CELLS

COP2	CMOS output	
TOP2	TTL output	
STANDARD INPUT AND I/O DEVICES		
CIO2	CMOS input/output	
TIO2	TTL input/output	
DIP2	Direct input	
INPUT AND I/O DEVICES WITH EXTERNAL PULLUP		
CIO2U	CMOS input/output with external pullup	
TIO2U	TTL input/output with external pullup	
DIP2U	Direct input with external pullup	
INPUT AND I/O DEVICES WITH PULLDOWN		
CIO2D	CMOS input/output with pulldown	
TIO2D	TTL input/output with pulldown	
DIP2D	Direct input with pulldown	

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