

V853™

32-/16-BIT SINGLE-CHIP MICROCONTROLLERS

The μ PD703003A, 703004A, and 703025A are members of the V850 Family™ of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features including a 32-bit CPU core, ROM, RAM, an interrupt controller, a real-time pulse unit, a serial interface, an A/D converter, a D/A converter, and PWM.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V853 User's Manual Hardware: U10913E

V850 Family User's Manual Architecture: U10243E

FEATURES

- Number of instructions: 74
- Minimum instruction execution time: 30 ns (@ 33 MHz operation)
- General-purpose registers: 32 bits \times 32 registers
- Instruction set optimized for control applications
- On-chip memory

ROM:	256 KB (μ PD703025A)
	128 KB (μ PD703003A)
	96 KB (μ PD703004A)
RAM:	8 KB (μ PD703025A)
	4 KB (μ PD703003A, 703004A)
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- 8-bit resolution D/A converter: 2 channels
- 8-/9-/10-/12-bit resolution PWM: 2 channels
- Power saving functions

APPLICATIONS

- AV: Camcorders, VCRs, etc.
- Office equipment: PPCs, LBPs, printers, etc.
- Industrial equipment: Motor controllers, NC machine tools, etc.
- Communications equipment: Mobile telephones, etc.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

ORDERING INFORMATION

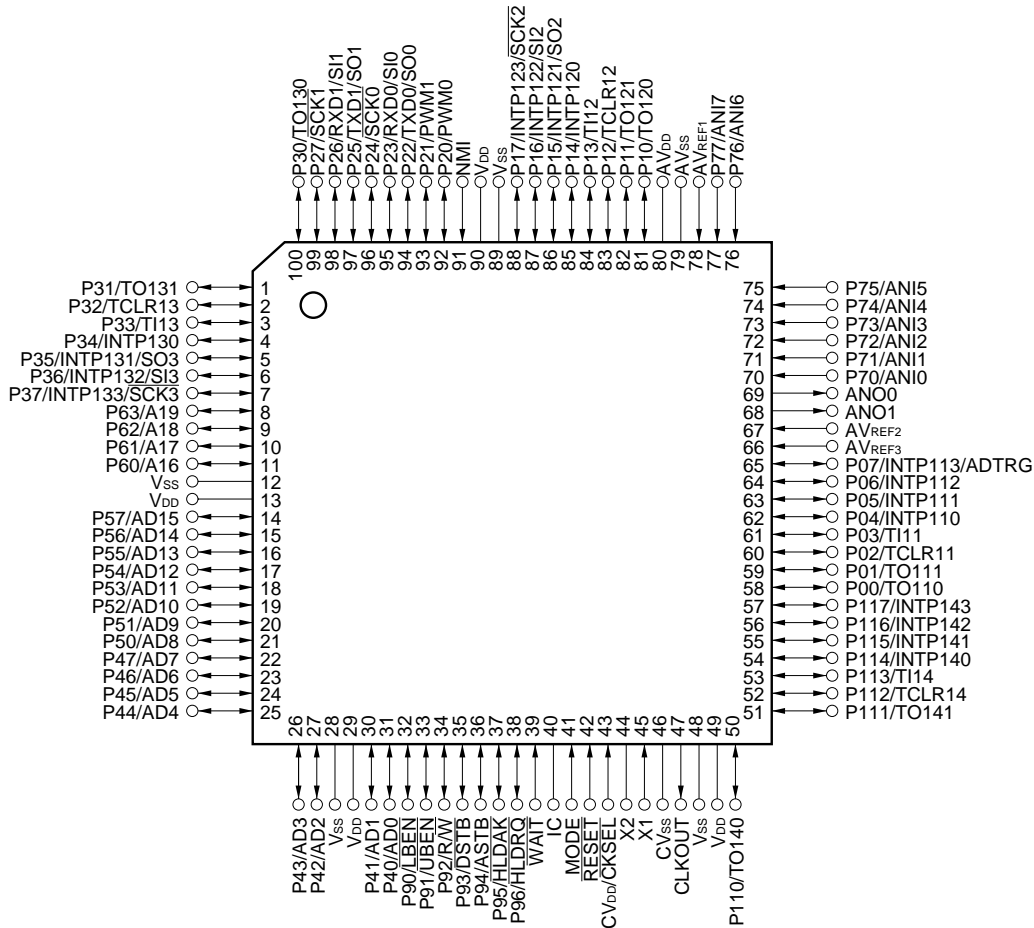
Part Number	Package	Maximum Operating Frequency (MHz)	Internal ROM (Bytes)	Internal RAM (Bytes)
μPD703003AGC-25-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	25	128 K	4 K
μPD703003AGC-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	33	128 K	4 K
μPD703004AGC-25-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	25	96 K	4 K
μPD703004AGC-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	33	96 K	4 K
μPD703025AGC-25-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	25	256 K	8 K
μPD703025AGC-33-xxx-8EU	100-pin plastic LQFP (fine pitch) (14 × 14 mm)	33	256 K	8 K

Remark xxx indicates ROM code suffix.

PIN CONFIGURATION

- 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

- μPD703003AGC-25-xxx-8EU μPD703004AGC-33-xxx-8EU
- μPD703003AGC-33-xxx-8EU μPD703025AGC-25-xxx-8EU
- μPD703004AGC-25-xxx-8EU μPD703025AGC-33-xxx-8EU

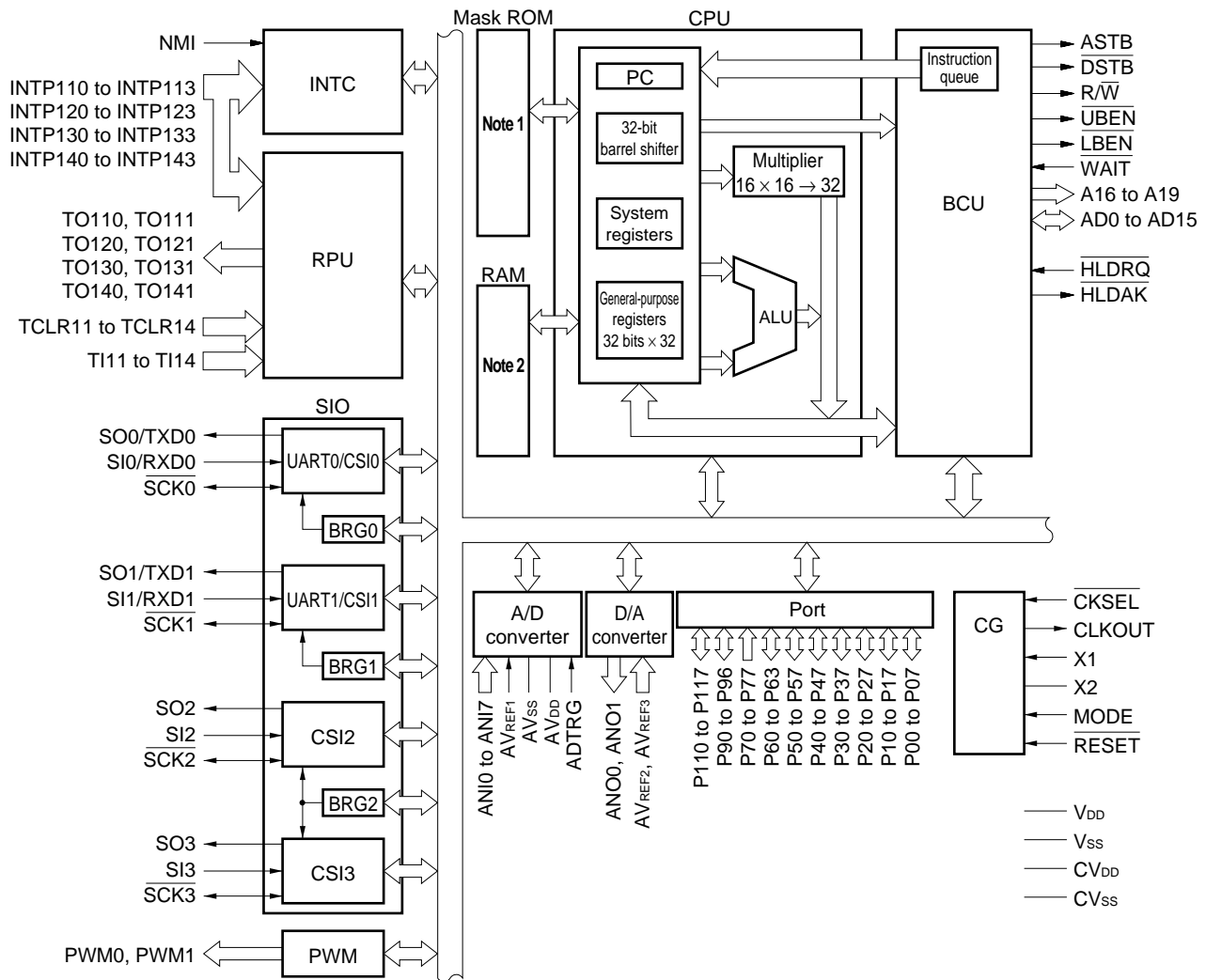


Caution Connect the IC (Internally Connected) pin directly to Vss.

PIN NAMES

A16 to A19:	Address Bus	P30 to P37:	Port 3
AD0 to AD15:	Address/Data Bus	P40 to P47:	Port 4
ADTRG:	AD Trigger Input	P50 to P57:	Port 5
ANI0 to ANI7:	Analog Input	P60 to P63:	Port 6
ANO0, ANO1:	Analog Output	P70 to P77:	Port 7
ASTB:	Address Strobe	P90 to P96:	Port 9
AVDD:	Analog Power Supply	P110 to P117:	Port 11
AVREF1 to AVREF3:	Analog Reference Voltage	PWM0, PWM1:	Pulse Width Modulation
AVSS:	Analog Ground	RESET:	Reset
CVDD:	Power Supply for Clock Generator	R/W:	Read/Write Status
CVSS:	Ground for Clock Generator	RXD0, RXD1:	Receive Data
CKSEL:	Clock Select	SCK0 to SCK3:	Serial Clock
CLKOUT:	Clock Output	SI0 to SI3:	Serial Input
DSTB:	Data Strobe	SO0 to SO3:	Serial Output
HLDAK:	Hold Acknowledge	TO110, TO111,:	Timer Output
HLDRQ:	Hold Request	TO120, TO121,	
IC:	Internally Connected	TO130, TO131,	
INTP110 to INTP113,:	Interrupt Request from Peripherals	TO140, TO141	
INTP120 to INTP123,		TCLR11 to TCLR14:	Timer Clear
INTP130 to INTP133,		TI11 to TI14:	Timer Input
INTP140 to INTP143		TXD0, TXD1:	Transmit Data
LBEN:	Lower Byte Enable	UBEN:	Upper Byte Enable
MODE:	Mode	WAIT:	Wait
NMI:	Non-maskable Interrupt Request	X1, X2:	Crystal
P00 to P07:	Port 0	VDD:	Power Supply
P10 to P17:	Port 1	VSS:	Ground
P20 to P27:	Port 2		

INTERNAL BLOCK DIAGRAM



- Notes**
1. μPD703003A: 128 KB
 μPD703004A: 96 KB
 μPD703025A: 256 KB
 2. μPD703003A, 703004A: 4 KB
 μPD703025A: 8 KB

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1. DIFFERENCES AMONG PRODUCTS

Item			μPD703003	μPD703003A	μPD703004A	μPD703025A	μPD70F3003	μPD70F3003A	μPD70F3025A	
Internal ROM			Mask ROM				Flash memory			
			128 KB		96 KB	256 KB	128 KB		256 KB	
Internal RAM			4 KB			8 KB	4 KB		8 KB	
Operation mode	Normal operation mode	Single-chip mode	Implemented							
		ROM-less mode	Implemented	Not implemented			Implemented	Not implemented		
	Flash memory programming mode		Not implemented				Implemented			
V _{PP} pin			Not implemented				Implemented			
Value of CKC register after reset			00H	MODE = 0: 03H MODE = 1: 00H			00H	MODE = 0: 03H MODE = 1: 00H		
Electrical specifications			Power consumption levels vary (see specific product's data sheet).							
Other			Depending on the products, noise tolerance and noise emission will vary due to the differences in circuit scale and mask layout.							

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units.	TO110
P01			TO111
P02			TCLR11
P03			TI11
P04			INTP110
P05			INTP111
P06			INTP112
P07			INTP113/ADTRG
P10	I/O	Port 1 8-bit I/O port Input/output can be specified in 1-bit units.	TO120
P11			TO121
P12			TCLR12
P13			TI12
P14			INTP120
P15			INTP121/SO2
P16			INTP122/SI2
P17			INTP123/SCK2
P20	I/O	Port 2 8-bit I/O port Input/output can be specified in 1-bit units.	PWM0
P21			PWM1
P22			TXD0/SO0
P23			RXD0/SI0
P24			SCK0
P25			TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P30	I/O	Port 3 8-bit I/O port Input/output can be specified in 1-bit units.	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO3
P36			INTP132/SI3
P37			INTP133/SCK3
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units.	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units.	AD8 to AD15

(2/2)

Pin Name	I/O	Function	Alternate Function
P60 to P63	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units.	A16 to A19
P70 to P77	Input	Port 7 8-bit input port	ANI0 to ANI7
P90	I/O	Port 9 7-bit I/O port Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/W
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			$\overline{\text{HLDK}}$
P96			$\overline{\text{HLDRQ}}$
P110	I/O	Port 11 8-bit I/O port Input/output can be specified in 1-bit units.	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143

2.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO110	Output	Pulse signal output from timers 11 to 14	P00
TO111			P01
TO120			P10
TO121			P11
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TCLR11	Input	External clear signal input for timers 11 to 14	P02
TCLR12			P12
TCLR13			P32
TCLR14			P112
TI11	Input	External count clock input for timers 11 to 14	P03
TI12			P13
TI13			P33
TI14			P113
INTP110	Input	External maskable interrupt request input, also used as external capture trigger input for timer 11	P04
INTP111			P05
INTP112			P06
INTP113			P07/ADTRG
INTP120	Input	External maskable interrupt request input, also used as external capture trigger input for timer 12	P14
INTP121			P15/SO2
INTP122			P16/SI2
INTP123			P17/SCK2
INTP130	Input	External maskable interrupt request input, also used as external capture trigger input for timer 13	P34
INTP131			P35/SO3
INTP132			P36/SI3
INTP133			P37/SCK3
INTP140	Input	External maskable interrupt request input, also used as external capture trigger input for timer 14	P114
INTP141			P115
INTP142			P116
INTP143			P117
SO0	Output	Serial transmit data output (3-wire) for CSI0 to CSI3	P22/TXD0
SO1			P25/TXD1
SO2			P15/INTP121
SO3			P35/INTP131
SI0	Input	Serial receive data input (3-wire) for CSI0 to CSI3	P23/RXD0
SI1			P26/RXD1
SI2			P16/INTP122
SI3			P36/INTP132

(2/2)

Pin Name	I/O	Function	Alternate Function
SCK0	I/O	Serial clock I/O (3-wire) for CSI0 to CSI3	P24
SCK1			P27
SCK2			P17/INTP123
SCK3			P37/INTP133
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
PWM0	Output	PWM pulse signal output	P20
PWM1			P21
AD0 to AD7	I/O	16-bit multiplexed address/data bus for external memory expansion	P40 to P47
AD8 to AD15			P50 to P57
A16 to A19	Output	Higher address bus used for external memory expansion	P60 to P63
LBEN	Output	External data bus's lower byte enable signal output	P90
UBEN		External data bus's higher byte enable signal output	P91
R/W	Output	External read/write status output	P92
DSTB		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
HLDAK	Output	Bus hold acknowledge output	P95
HLDRQ	Input	Bus hold request input	P96
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
ANO0, ANO1	Output	Analog output from D/A converter	—
NMI	Input	Non-maskable interrupt request input	—
CLKOUT	Output	System clock output	—
CKSEL	Input	Input for specifying clock generator's operation mode	CV _{DD}
WAIT	Input	Control signal input for inserting wait in bus cycle	—
MODE	Input	Operation mode specification	—
RESET	Input	System reset input	—
X1	Input	Resonator connection for system clock. Input is via X1 when using an external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P07/INTP113
AV _{REF1}	Input	Reference voltage input for A/D converter	—
AV _{REF2}	Input	Reference voltage input for D/A converter	—
AV _{REF3}			—
AV _{DD}	—	Positive power supply for A/D converter	—
AV _{SS}	—	Ground potential for A/D converter	—
CV _{DD}	—	Positive power supply for on-chip clock generator	CKSEL
CV _{SS}	—	Ground potential for on-chip clock generator	—
V _{DD}	—	Positive power supply	—
V _{SS}	—	Ground potential	—
IC	—	Internally connected pin (Connect directly to V _{SS})	—

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. Figure 2-1 illustrates the various circuit types using partially abridged diagrams.

When connecting to V_{DD} or V_{SS} via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

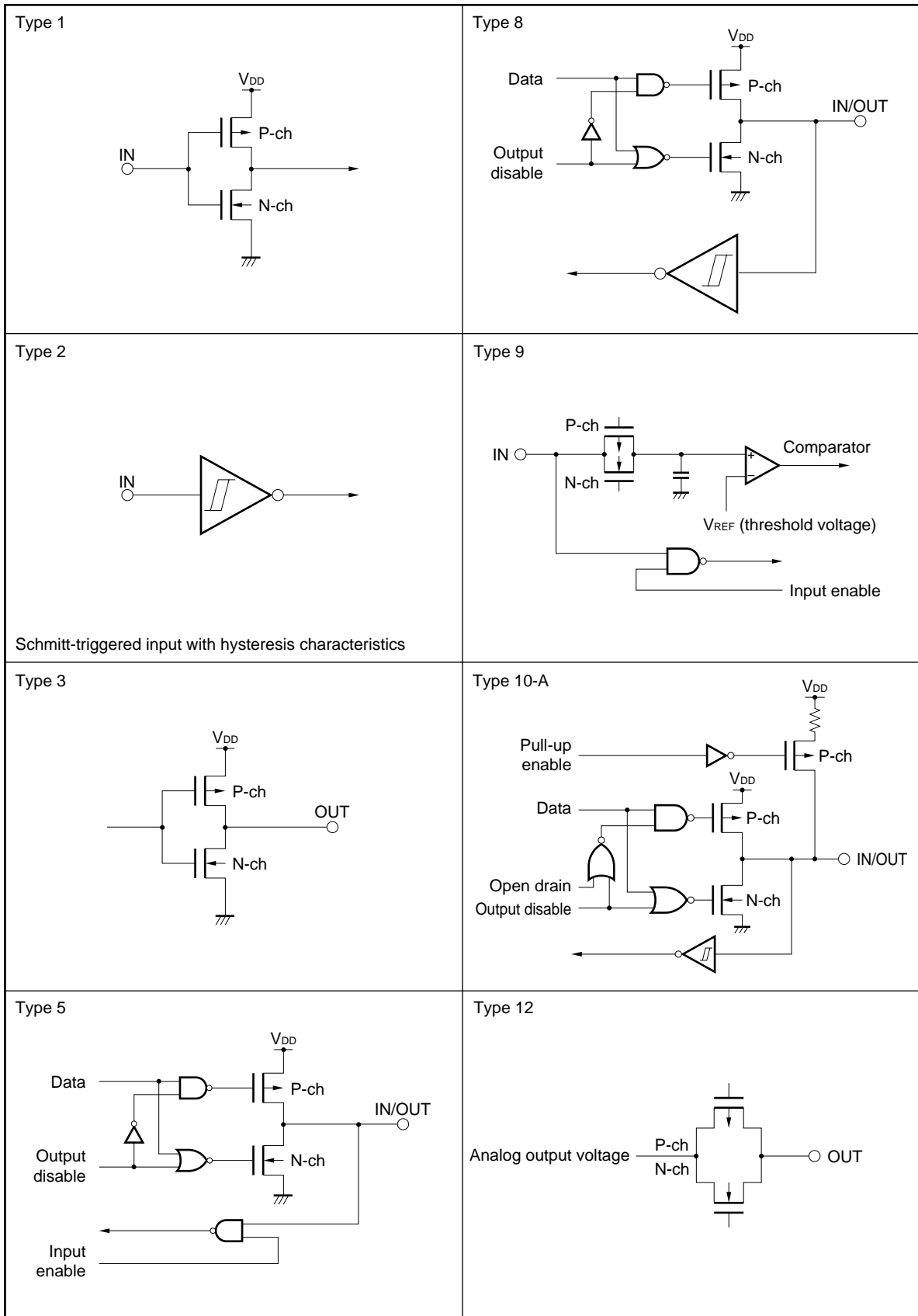
Table 2-1. Types of Pin Input/Output Circuits (1/2)

Pin Name	Input/Output Circuit Type	Recommended Connection of Unused Pins	
P00/TO110, P01/TO111	5	Input: Independently connect to V _{DD} or V _{SS} via a resistor. Output: Leave open.	
P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113/ADTRG	8		
P10/TO120, P11/TO121	5		
P12/TCLR12, P13/TI12 P14/INTP120 P15/INTP121/SO2 P16/INTP122/SI2 P17/INTP123/SCK2	8		
P20/PWM0, P21/PWM1 P22/TXD0/SO0	5		
P23/RXD0/SI0, P24/SCK0	8		
P25/TXD1/SO1	5		
P26/RXD1/SI1, P27/SCK1	8		
P30/TO130, P31/TO131	5		
P32/TCLR13, P33/TI13 P34/INTP130	8		
P35/INTP131/SO3 P36/INTP132/SI3 P37/INTP133/SCK3	10-A	Connect directly to V _{SS} .	
P40/AD0 to P47/AD7	5		
P50/AD8 to P57/AD15			
P60/A16 to P63/A19			
P70/ANI0 to P77/ANI7	9		
P90/LBEN	5		Input: Independently connect to V _{DD} or V _{SS} via a resistor. Output: Leave open.
P91/UBEN			
P92/R/W			
P93/DSTB			
P94/ASTB			
P95/HLDAK			
P96/HLDRQ			
P110/TO140, P111/TO141			
P112/TCLR14, P113/TI14 P114/INTP140 to P117/INTP143		8	
ANO0, ANO1	12	Leave open.	
NMI	2	Connect directly to V _{SS} .	

Table 2-1. Types of Pin Input/Output Circuits (2/2)

Pin Name	Input/Output Circuit Type	Recommended Connection of Unused Pins
CLKOUT	3	Leave open.
WAIT	1	Connect directly to V _{DD} .
MODE	2	—
RESET		
CV _{DD} /CKSEL		
AV _{REF1} to AV _{REF3} , AV _{SS}	—	Connect directly to V _{SS} .
AV _{DD}	—	Connect directly to V _{DD} .
IC	—	Connect directly to V _{SS} .

Figure 2-1. Pin Input/Output Circuits



3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit	
Power supply voltage	V _{DD}	V _{DD} pin	-0.5 to +7.0	V	
	CV _{DD}	CV _{DD} pin	-0.5 to V _{DD} + 0.3	V	
	CV _{SS}	CV _{SS} pin	-0.5 to +0.5	V	
	AV _{DD}	AV _{DD} pin	-0.5 to V _{DD} + 0.3	V	
	AV _{SS}	AV _{SS} pin	-0.5 to +0.5	V	
Input voltage	V _{I1}	Note , V _{DD} = 5.0 V ±10%	-0.5 to V _{DD} + 0.3	V	
Clock input voltage	V _K	X1 pin, V _{DD} = 5.0 V ±10%	-0.5 to V _{DD} + 1.0	V	
Output current, low	I _{OL}	Per pin	4.0	mA	
		Total for all pins	100	mA	
Output current, high	I _{OH}	Per pin	-4.0	mA	
		Total for all pins	-100	mA	
Output voltage	V _O	V _{DD} = 5.0 V ±10%	-0.5 to V _{DD} + 0.3	V	
Analog input voltage	V _{IAN}	P70/ANI0 to P77/ANI7	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.3	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.3	V
Analog reference input voltage	AV _{REF}	AV _{REF1} to AV _{REF3}	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.3	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.3	V
Operating ambient temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +150	°C	

Note X1, P70/ANI0 to P77/ANI7, and AV_{REF1} to AV_{REF3} are excluded.

- Cautions**
1. Be sure to avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND. However, open-drain pins and open collector pins can be directly connected. A direct connection to an external circuit can be made to avoid conflicting output from high-impedance pins if the external circuit is designed for the correct timing.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
- The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _I	f _c = 1 MHz Unmeasured pins returned to 0 V.			15	pF
I/O capacitance	C _{IO}				15	pF
Output capacitance	C _O				15	pF

★ **Operating Conditions**

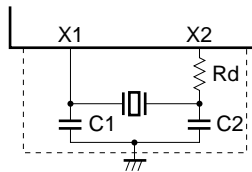
Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Ambient Temperature (T_A)	Power Supply Voltage (V_{DD})
Direct mode, PLL mode	2 to 33 MHz ^{Note 1}	-40 to +85°C	5.0 V \pm 10%
	5 to 33 MHz ^{Note 2}	-40 to +85°C	5.0 V \pm 10%

- Notes** 1. When not using A/D converter
 2. When using A/D converter

Recommended Oscillator

(1) Ceramic resonator connection ($T_A = -40$ to $+85^\circ\text{C}$)

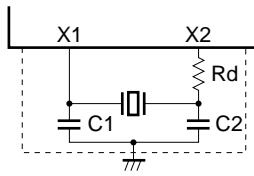
(a) μPD703003A, 703004A



Manufacturer	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)	
★ Kyocera Corporation	KBR-5.0MSA/MSB	5.0	33	33	680	4.5	5.5	0.14
	KBR-5.0MKC	5.0	On-chip	On-chip	680	4.5	5.5	0.14
	KBR-5.0MKD	5.0	On-chip	On-chip	680	4.5	5.5	0.14
	KBR-5.0MKS	5.0	On-chip	On-chip	680	4.5	5.5	0.14
	PBRC5.00A	5.0	33	33	680	4.5	5.5	0.14
	PBRC5.00B	5.0	On-chip	On-chip	680	4.5	5.5	0.14
	KBR-6.6MSA/MSB	6.6	33	33	—	4.5	5.5	0.10
	KBR-6.6MKC	6.6	On-chip	On-chip	—	4.5	5.5	0.10
	KBR-6.6MKD	6.6	On-chip	On-chip	—	4.5	5.5	0.10
	KBR-6.6MKS	6.6	On-chip	On-chip	—	4.5	5.5	0.10
	PBRC6.60A	6.6	33	33	—	4.5	5.5	0.10
PBRC6.60B	6.6	On-chip	On-chip	—	4.5	5.5	0.10	
TDK	CCR5.0MC3	5.0	On-chip	On-chip	—	4.5	5.5	0.18
	FCR5.0MC5	5.0	On-chip	On-chip	—	4.5	5.5	0.16
	CCR6.6MC3	6.6	On-chip	On-chip	—	4.5	5.5	0.17
★ Murata Mfg. Co., Ltd.	CSA5.00MG040	5.0	100	100	—	4.5	5.5	0.31
	CST5.00MGW040	5.0	On-chip	On-chip	—	4.5	5.5	0.31
	CSA6.60MTZ040	6.6	100	100	—	4.5	5.5	0.30
	CST6.60MTW040	6.6	On-chip	On-chip	—	4.5	5.5	0.30

- Cautions** 1. Put the oscillator as close to the X1 and X2 pins as possible.
 2. Do not cross the wiring with the other signal lines in the area enclosed by the broken lines.
 3. Sufficiently evaluate the matching between the μPD703003A or 703004A and the resonator.

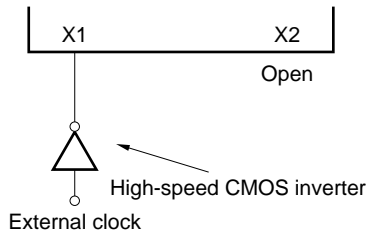
(b) μ PD703025A



Manufacturer	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)	
TDK	CCR4.0MC3	4.0	On-chip	On-chip	—	4.5	5.5	0.28
	CCR5.0MC3	5.0	On-chip	On-chip	—	4.5	5.5	0.20
★ Murata Mfg. Co., Ltd.	CSA4.00MG040	4.0	100	100	—	4.5	5.5	0.20
	CST4.00MGW040	4.0	On-chip	On-chip	—	4.5	5.5	0.20
	CSTS0400MG06	4.0	On-chip	On-chip	—	4.5	5.5	0.16
	CSA6.60MTZ040	6.6	100	100	—	4.5	5.5	0.20
	CST6.60MTW040	6.6	On-chip	On-chip	—	4.5	5.5	0.20
	CSTS0660MG06	6.6	On-chip	On-chip	—	4.5	5.5	0.09

- Cautions**
1. Put the oscillator as close to the X1 and X2 pins as possible.
 2. Do not cross the wiring with the other signal lines in the area enclosed by the broken lines.
 3. Sufficiently evaluate the matching between μ PD703025A and the resonator.

(2) External clock input



- Cautions**
1. Put the high-speed CMOS inverter as close to the X1 pin as possible.
 2. Sufficiently evaluate the matching between the μ PD703003A, 703004A, or 703025A and the high-speed CMOS inverter.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH}	Except for X1 and pins listed in Note	2.2		V _{DD} + 0.3	V
		Note	0.8V _{DD}		V _{DD} + 0.3	V
Input voltage, low	V _{IL}	Except for X1 and pins listed in Note	-0.5		+0.8	V
		Note	-0.5		0.2V _{DD}	V
Clock input voltage, high	V _{XH}	X1	0.8V _{DD}		V _{DD} + 0.5	V
Clock input voltage, low	V _{XL}	X1	-0.5		+0.6	V
Schmitt-triggered input Threshold voltage	V _T ⁺	Note , rising edge		3.0		V
	V _T ⁻	Note , falling edge		2.0		V
Schmitt-triggered input hysteresis width	V _T ⁺ - V _T ⁻	Note	0.5			V
Output voltage, high	V _{OH}	I _{OH} = -2.5 mA	0.7V _{DD}			V
		I _{OH} = -100 μA	V _{DD} - 0.4			V
Output voltage, low	V _{OL}	I _{OL} = 2.5 mA			0.45	V
Input leakage current, high	I _{LIH}	V _i = V _{DD}			10	μA
Input leakage current, low	I _{LIL}	V _i = 0 V			-10	μA
Output leakage current, high	I _{LOH}	V _o = V _{DD}			10	μA
Output leakage current, low	I _{LOL}	V _o = 0 V			-10	μA
Software pull-up resistor	R	P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3	15	40	90	kΩ

Note P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, RESET, NMI, MODE

Remarks 1. TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V.
2. φ = Internal system clock frequency

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

(2/2)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Power supply current	μPD703003A, 703004A	When operating	I _{DD1}	Direct mode ^{Note}		1.9 × φ + 5	2.1 × φ + 17	mA
				PLL mode ^{Note}		2.0 × φ + 7	2.2 × φ + 20	mA
		In HALT mode	I _{DD2}	Direct mode ^{Note}		1.2 × φ + 5	1.3 × φ + 13	mA
				PLL mode ^{Note}		1.3 × φ + 7	1.4 × φ + 15	mA
		In IDLE mode	I _{DD3}	Direct mode ^{Note}		8 × φ + 300	10 × φ + 500	μA
				PLL mode ^{Note}		0.1 × φ + 2	0.2 × φ + 3	mA
		In STOP mode	I _{DD4}			2	50	μA
			μPD703025A	When operating	I _{DD1}	Direct mode ^{Note}		2.5 × φ + 2
PLL mode ^{Note}						2.6 × φ + 4	2.9 × φ + 19.5	mA
In HALT mode	I _{DD2}			Direct mode ^{Note}		1.3 × φ + 5	1.4 × φ + 13	mA
				PLL mode ^{Note}		1.3 × φ + 10	1.4 × φ + 18	mA
In IDLE mode	I _{DD3}			Direct mode ^{Note}		8 × φ + 300	10 × φ + 500	μA
				PLL mode ^{Note}		0.1 × φ + 2	0.2 × φ + 3	mA
In STOP mode	I _{DD4}					2	50	μA

Note When using A/D converter: φ = 5 to 33 MHz

★ When not using A/D converter: φ = 2 to 33 MHz

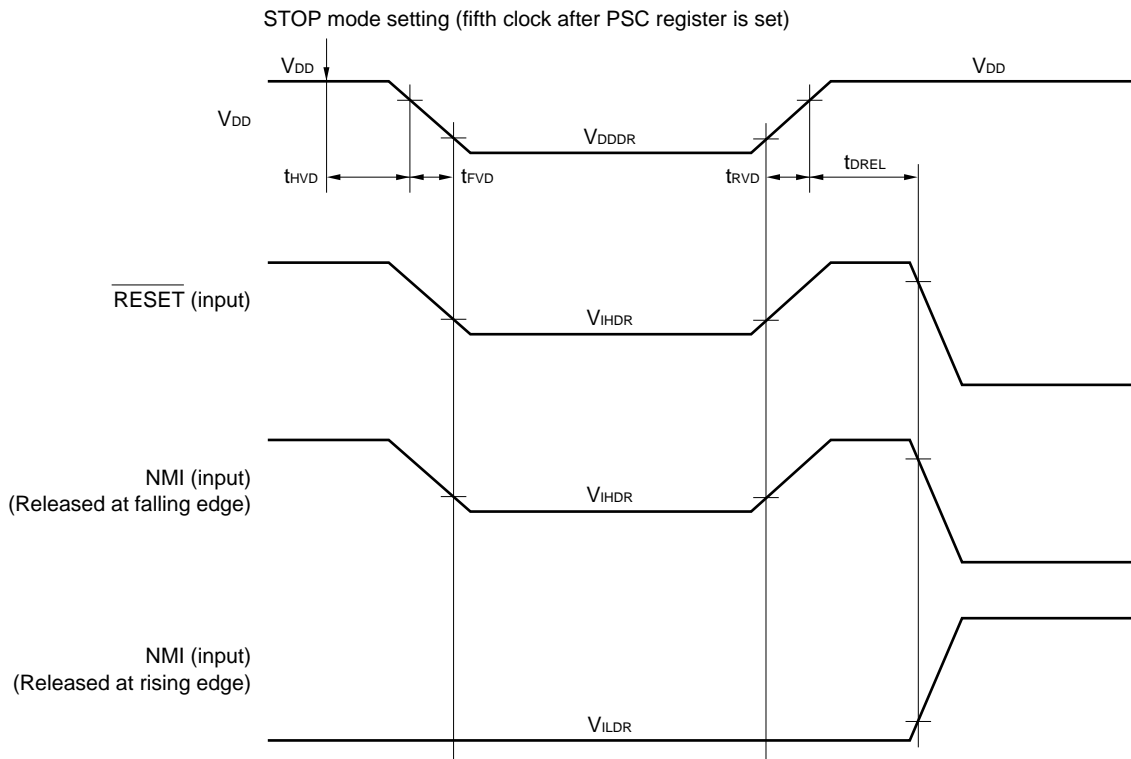
- Remarks**
1. TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V. The power supply current does not include AV_{REF1} to AV_{REF3} or the current that flows across a software pull-up resistor.
 2. φ = Internal system clock frequency

Data Retention Characteristics (T_A = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Data retention voltage	V _{DDDR}	STOP mode	1.5		5.5	V	
Data retention current	I _{DDDR}	V _{DD} = V _{DDDR}	-40°C ≤ T _A ≤ +50°C		0.2V _{DDDR}	50	μA
			50°C < T _A ≤ 85°C		0.2V _{DDDR}	200	μA
Power supply voltage rise time	t _{RV} D		200			μs	
Power supply voltage fall time	t _{FV} D		200			μs	
Power supply voltage hold time (vs. STOP mode setting)	t _{HV} D		0			ms	
STOP mode release signal input time	t _{DREL}	Note	0			ns	
Data retention high-level input voltage	V _{IHDR}	Note	0.9V _{DDDR}		V _{DDDR}	V	
Data retention low-level input voltage	V _{ILDR}		0		0.1V _{DDDR}	V	

Note P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, RESET, NMI, MODE, X1

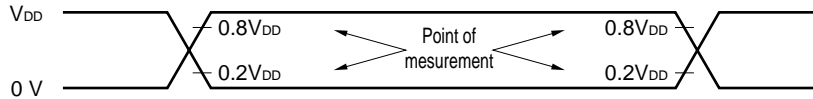
Remark TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V.



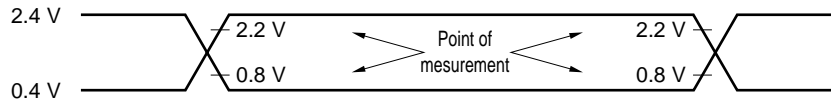
AC Characteristics (T_A = -40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

AC test input waveform

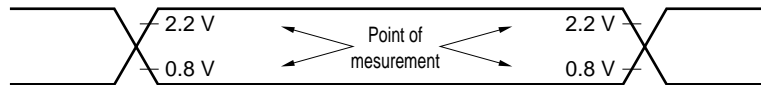
- (a) P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, RESET, NMI, MODE, X1



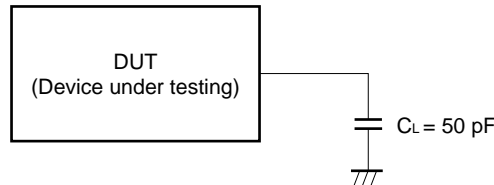
- (b) Pins other than those listed in (a) above



AC test output measurement points



Load condition



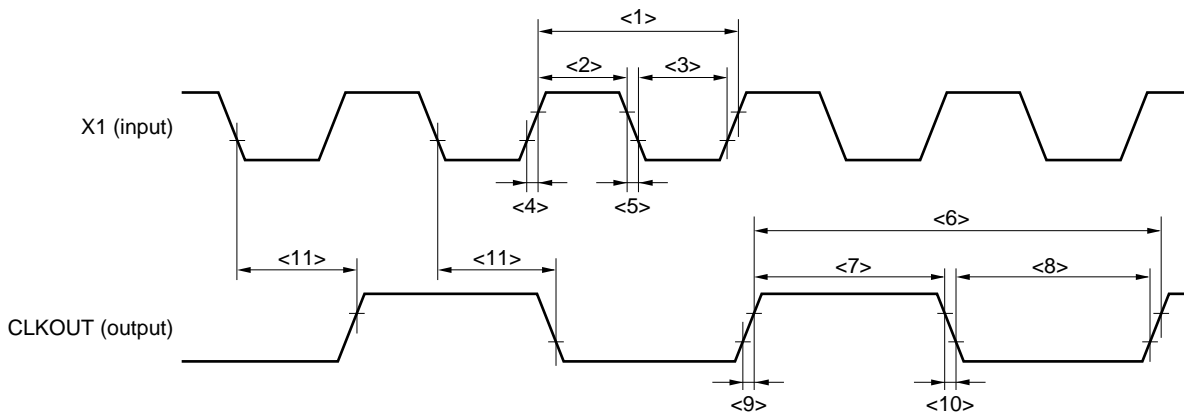
Caution In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance to below 50 pF.

(1) Clock timing

Parameter	Symbol		Conditions	25 MHz Version		33 MHz Version		Unit
				MIN.	MAX.	MIN.	MAX.	
★ X1 input cycle	<1>	t _{CYX}	Direct mode	20	Note 1	15	Note 1	ns
			PLL mode (PLL locked)	200	Note 1	151	Note 1	ns
X1 input high-level width	<2>	t _{WXH}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input low-level width	<3>	t _{WXL}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input rise time	<4>	t _{XR}	Direct mode		7		7	ns
			PLL mode		15		10	ns
X1 input fall time	<5>	t _{XF}	Direct mode		7		7	ns
			PLL mode		15		10	ns
★ CPU operating frequency	–	φ		Note 2	25	Note 2	33	MHz
CLKOUT output cycle	<6>	t _{CYK}		40	Note 3	30	Note 3	ns
CLKOUT input high-level width	<7>	t _{WKH}		0.5T – 5		0.5T – 5		ns
CLKOUT input low-level width	<8>	t _{WKL}		0.5T – 5		0.5T – 5		ns
CLKOUT input rise time	<9>	t _{KR}			5		5	ns
CLKOUT input fall time	<10>	t _{KF}			5		5	ns
Delay time from X1↓ to CLKOUT	<11>	t _{DXK}	Direct mode	3	17	3	17	ns

- ★ **Notes** 1. When using A/D converter: 100 ns
When not using A/D converter: 250 ns
- ★ 2. When using A/D converter: 5 MHz
When not using A/D converter: 2 MHz
- ★ 3. When using A/D converter: 200 ns
When not using A/D converter: 500 ns

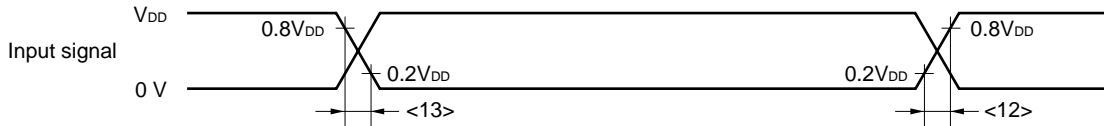
Remark T = t_{CYK}



(2) Input waveform

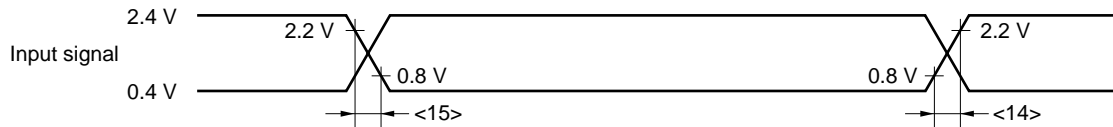
- (a) P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113, P12/TCLR12, P13/TI12, P14/INTP120, P15/INTP121/SO2, P16/INTP122/SI2, P17/INTP123/SCK2, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, P32/TCLR32, P33/TI13, P34/INTP130, P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3, P112/TCLR14, P113/TI14, P114/INTP140 to P117/INTP143, RESET, NMI, MODE

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
Input rise time	<12> t_{IR2}			20		20	ns
Input fall time	<13> t_{IF2}			20		20	ns



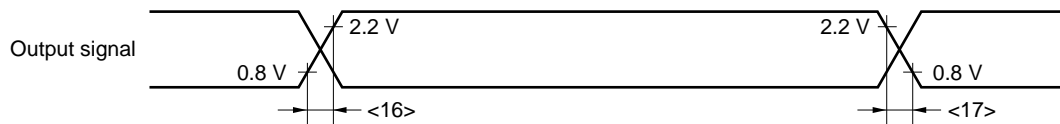
(b) Pins other than those listed in (a) above

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
Input rise time	<14> t_{IR1}			10		10	ns
Input fall time	<15> t_{IF1}			10		10	ns



(3) Output waveform (other than CLKOUT)

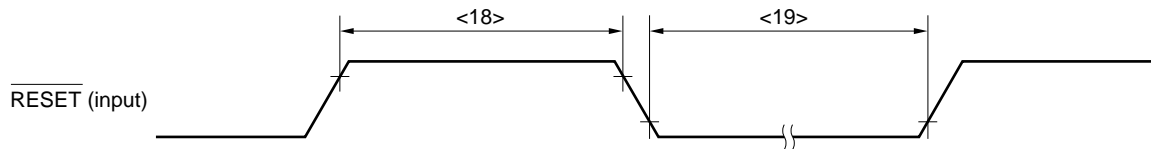
Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
Output rise time	<16> t_{OR}			10		10	ns
Output fall time	<17> t_{OF}			10		10	ns



(4) Reset timing

Parameter	Symbol		Conditions	25 MHz Version		33 MHz Version		Unit
				MIN.	MAX.	MIN.	MAX.	
RESET high-level width	<18>	t _{WRSH}		500		500		ns
RESET low-level width	<19>	t _{WRSL}	When power supply is ON and STOP mode has been released	500 + T _{OST}		500 + T _{OST}		ns
			Other than when power supply is ON and STOP mode has been released	500		500		ns

Remark T_{OST}: Oscillation stabilization time



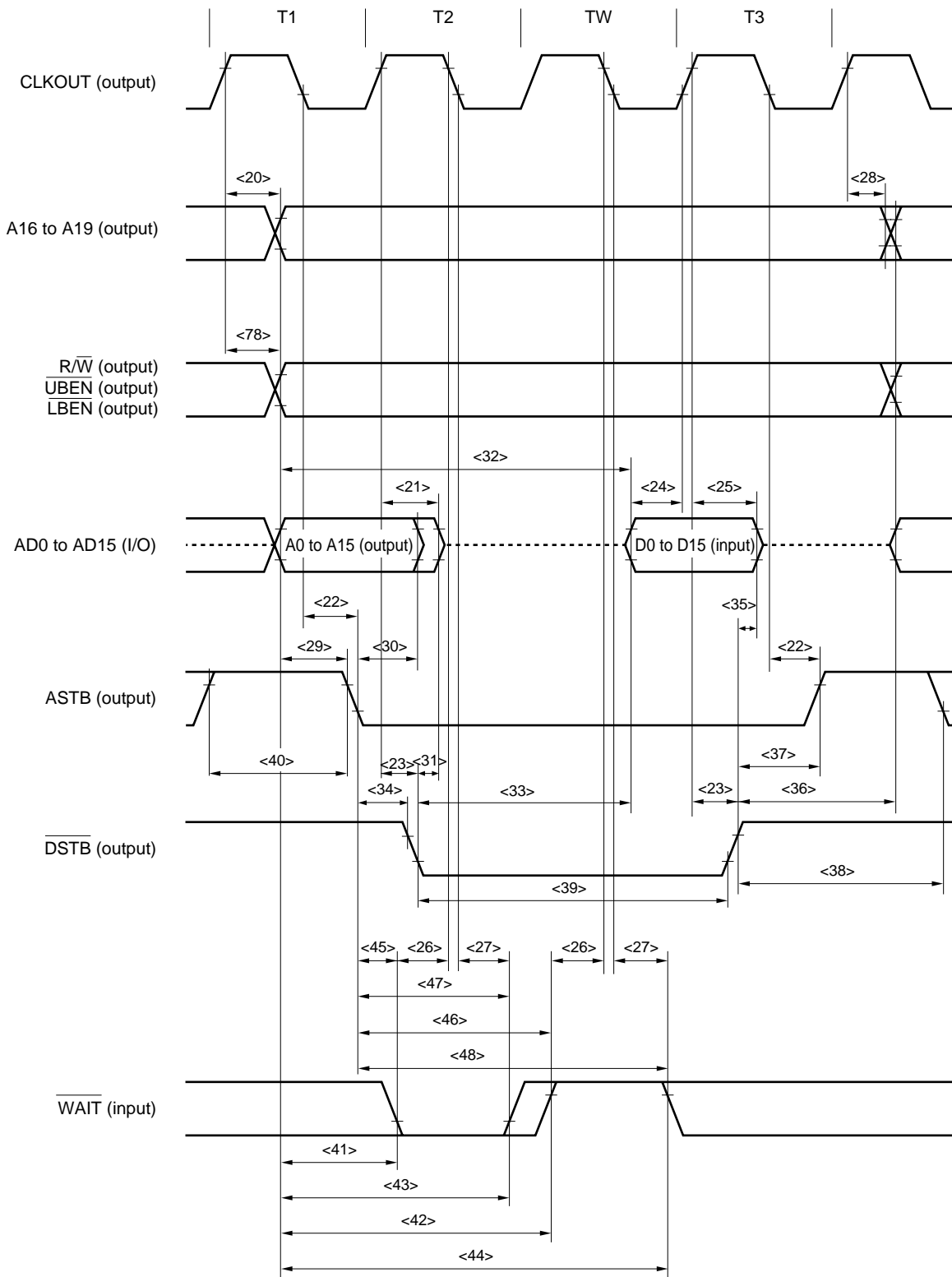
(5) Read timing (1/2)

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
Delay time from CLKOUT↑ to address	<20> t _{DKA}		3	20	3	20	ns
Delay time from CLKOUT↑ to R _W , UBEN, LBEN	<78> t _{DKA2}		-2	+13	-2	+13	ns
Delay time from CLKOUT↑ to address float	<21> t _{FKA}		3	15	3	15	ns
Delay time from CLKOUT↓ to ASTB	<22> t _{DKST}		3	15	3	15	ns
Delay time from CLKOUT↑ to $\overline{\text{DSTB}}$	<23> t _{DKD}		3	15	3	15	ns
Data input setup time (to CLKOUT↑)	<24> t _{SIDK}		5		5		ns
Data input hold time (from CLKOUT↑)	<25> t _{HKID}		5		5		ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<26> t _{SWTK}		5		5		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<27> t _{HKWT}		5		5		ns
Address hold time (from CLKOUT↑)	<28> t _{HKA}		0		0		ns
Address setup time (to ASTB↓)	<29> t _{SAST}	-40°C ≤ T _A ≤ +70°C	0.5T - 10		0.5T - 10		ns
		70°C < T _A ≤ 85°C	0.5T - 12		0.5T - 12		ns
Address hold time (from ASTB↓)	<30> t _{HSTA}		0.5T - 10		0.5T - 10		ns
Delay time from $\overline{\text{DSTB}}$ ↓ to address float	<31> t _{FDA}			0		0	ns
Data input setup time (to address)	<32> t _{SAID}	-40°C ≤ T _A ≤ +70°C		(2 + n)T - 22		(2 + n)T - 22	ns
		70°C < T _A ≤ 85°C		(2 + n)T - 25		(2 + n)T - 25	ns
Data input setup time (to $\overline{\text{DSTB}}$ ↓)	<33> t _{SDID}	-40°C ≤ T _A ≤ +70°C		(1 + n)T - 20		(1 + n)T - 20	ns
		70°C < T _A ≤ 85°C		(1 + n)T - 24		(1 + n)T - 24	ns
Delay time from ASTB↓ to $\overline{\text{DSTB}}$ ↓	<34> t _{DSTD}		0.5T - 10		0.5T - 10		ns
Data input hold time (from $\overline{\text{DSTB}}$ ↑)	<35> t _{HDID}		0		0		ns
Delay time from $\overline{\text{DSTB}}$ ↑ to address output	<36> t _{DDA}		(1 + i)T		(1 + i)T		ns
Delay time from $\overline{\text{DSTB}}$ ↑ to ASTB↑	<37> t _{DDSTH}		0.5T - 10		0.5T - 10		ns
Delay time from $\overline{\text{DSTB}}$ ↑ to ASTB↓	<38> t _{DDSTL}		(1.5 + i)T - 10		(1.5 + i)T - 10		ns
$\overline{\text{DSTB}}$ low-level width	<39> t _{WDL}	-40°C ≤ T _A ≤ +70°C	(1 + n)T - 10		(1 + n)T - 10		ns
		70°C < T _A ≤ 85°C	(1 + n)T - 13		(1 + n)T - 13		ns
ASTB high-level width	<40> t _{WSTH}		T - 10		T - 10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<41> t _{SAWT1}	n ≥ 1, -40°C ≤ T _A ≤ +70°C		1.5T - 20		1.5T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		1.5T - 24		1.5T - 24	ns
	<42> t _{SAWT2}	n ≥ 1, -40°C ≤ T _A ≤ +70°C		(1.5 + n)T - 20		(1.5 + n)T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		(1.5 + n)T - 24		(1.5 + n)T - 24	ns
$\overline{\text{WAIT}}$ hold time (from address)	<43> t _{HAWT1}	n ≥ 1	(0.5 + n)T		(0.5 + n)T		ns
	<44> t _{HAWT2}	n ≥ 1	(1.5 + n)T		(1.5 + n)T		ns
$\overline{\text{WAIT}}$ setup time (to ASTB↓)	<45> t _{SSTWT1}	n ≥ 1, -40°C ≤ T _A ≤ +70°C		T - 18		T - 18	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		T - 20		T - 20	ns
	<46> t _{SSTWT2}	n ≥ 1		(1 + n)T - 15		(1 + n)T - 15	ns
$\overline{\text{WAIT}}$ hold time (from ASTB↓)	<47> t _{HSTWT1}	n ≥ 1	nT		nT		ns
	<48> t _{HSTWT2}	n ≥ 1	(1 + n)T		(1 + n)T		ns

Remarks 1. T = t_{cyk}

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.
3. i indicates the number of idle states (0 or 1) that are inserted after a read cycle.
4. Maintain at least one of the two data input hold times, either t_{HKID} (<25>) or t_{HDID} (<35>).

(5) Read timing (2/2): 1 wait



★

Remark Broken lines indicate high impedance.

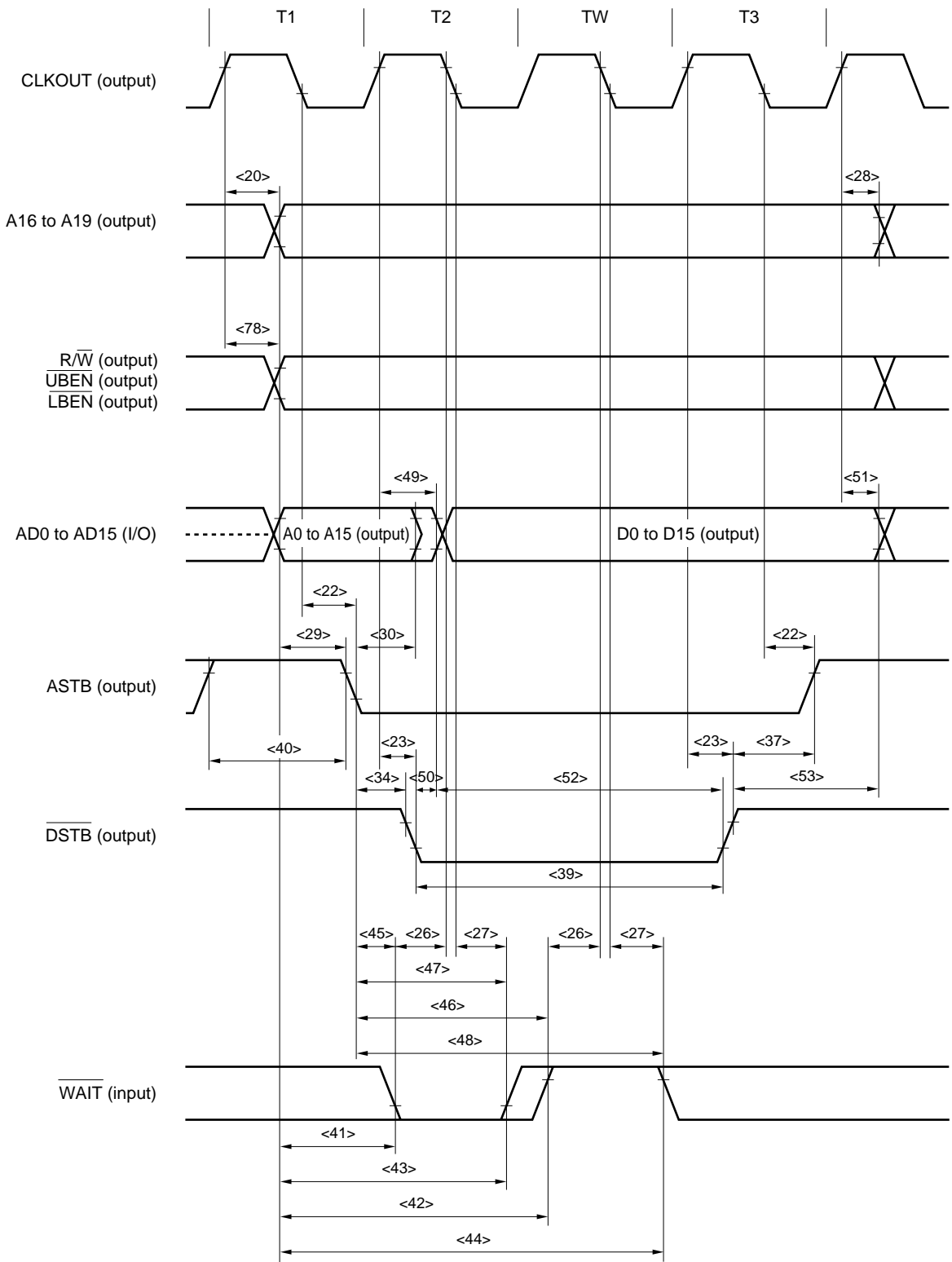
(6) Write timing (1/2)

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
Delay time from CLKOUT↑ to address	<20> t _{DKA}		3	20	3	20	ns
Delay time from CLKOUT↑ to R/W, UBEN, LBEN	<78> t _{DKA2}		-2	+13	-2	+13	ns
Delay time from CLKOUT↓ to ASTB	<22> t _{DKST}		3	15	3	15	ns
Delay time from CLKOUT↑ to $\overline{\text{DSTB}}$	<23> t _{DKD}		3	15	3	15	ns
WAIT setup time (to CLKOUT↓)	<26> t _{SWTK}		5		5		ns
WAIT hold time (from CLKOUT↓)	<27> t _{HKWT}		5		5		ns
Address hold time (from CLKOUT↑)	<28> t _{HKA}		0		0		ns
Address setup time (to ASTB↓)	<29> t _{SAST}	-40°C ≤ T _A ≤ +70°C	0.5T - 10		0.5T - 10		ns
		70°C < T _A ≤ 85°C	0.5T - 12		0.5T - 12		ns
Address hold time (from ASTB↓)	<30> t _{HSTA}		0.5T - 10		0.5T - 10		ns
Delay time from ASTB↓ to $\overline{\text{DSTB}}$ ↓	<34> t _{DDST}		0.5T - 10		0.5T - 10		ns
Delay time from DSTB↓ to $\overline{\text{ASTB}}$ ↓	<37> t _{DDSTH}		0.5T - 10		0.5T - 10		ns
$\overline{\text{DSTB}}$ low-level width	<39> t _{WDL}	-40°C ≤ T _A ≤ +70°C	(1 + n)T - 10		(1 + n)T - 10		ns
		70°C < T _A ≤ 85°C	(1 + n)T - 13		(1 + n)T - 13		ns
ASTB high-level width	<40> t _{WSTH}		T - 10		T - 10		ns
WAIT setup time (to address)	<41> t _{SAWT1}	n ≥ 1, -40°C ≤ T _A ≤ +70°C		1.5T - 20		1.5T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		1.5T - 24		1.5T - 24	ns
	<42> t _{SAWT2}	n ≥ 1, -40°C ≤ T _A ≤ +70°C		(1.5 + n)T - 20		(1.5 + n)T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		(1.5 + n)T - 24		(1.5 + n)T - 24	ns
WAIT hold time (from address)	<43> t _{HAWT1}	n ≥ 1	(0.5 + n)T		(0.5 + n)T		ns
	<44> t _{HAWT2}	n ≥ 1	(1.5 + n)T		(1.5 + n)T		ns
WAIT setup time (to ASTB↓)	<45> t _{SSTWT1}	n ≥ 1, -40°C ≤ T _A ≤ +70°C		T - 18		T - 18	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		T - 20		T - 20	ns
	<46> t _{SSTWT2}	n ≥ 1		(1 + n)T - 15		(1 + n)T - 15	ns
WAIT hold time (from ASTB↓)	<47> t _{HSTWT1}	n ≥ 1	nT		nT		ns
	<48> t _{HSTWT2}	n ≥ 1	(1 + n)T		(1 + n)T		ns
Delay time from CLKOUT↑ to data output	<49> t _{DKOD}	-40°C ≤ T _A ≤ +70°C		20		20	ns
		70°C < T _A ≤ 85°C		23		23	ns
Delay time from $\overline{\text{DSTB}}$ ↓ to data output	<50> t _{DDOD}			10		10	ns
Data output hold time (from CLKOUT↑)	<51> t _{HKOD}		0		0		ns
Data output setup time (to $\overline{\text{DSTB}}$ ↑)	<52> t _{SODD}		(1 + n)T - 15		(1 + n)T - 15		ns
Data output hold time (from $\overline{\text{DSTB}}$ ↑)	<53> t _{HDOD}		T - 10		T - 10		ns

Remarks 1. T = t_{cyk}

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

(6) Write timing (2/2): 1 wait



★ Remark Broken lines indicate high impedance.

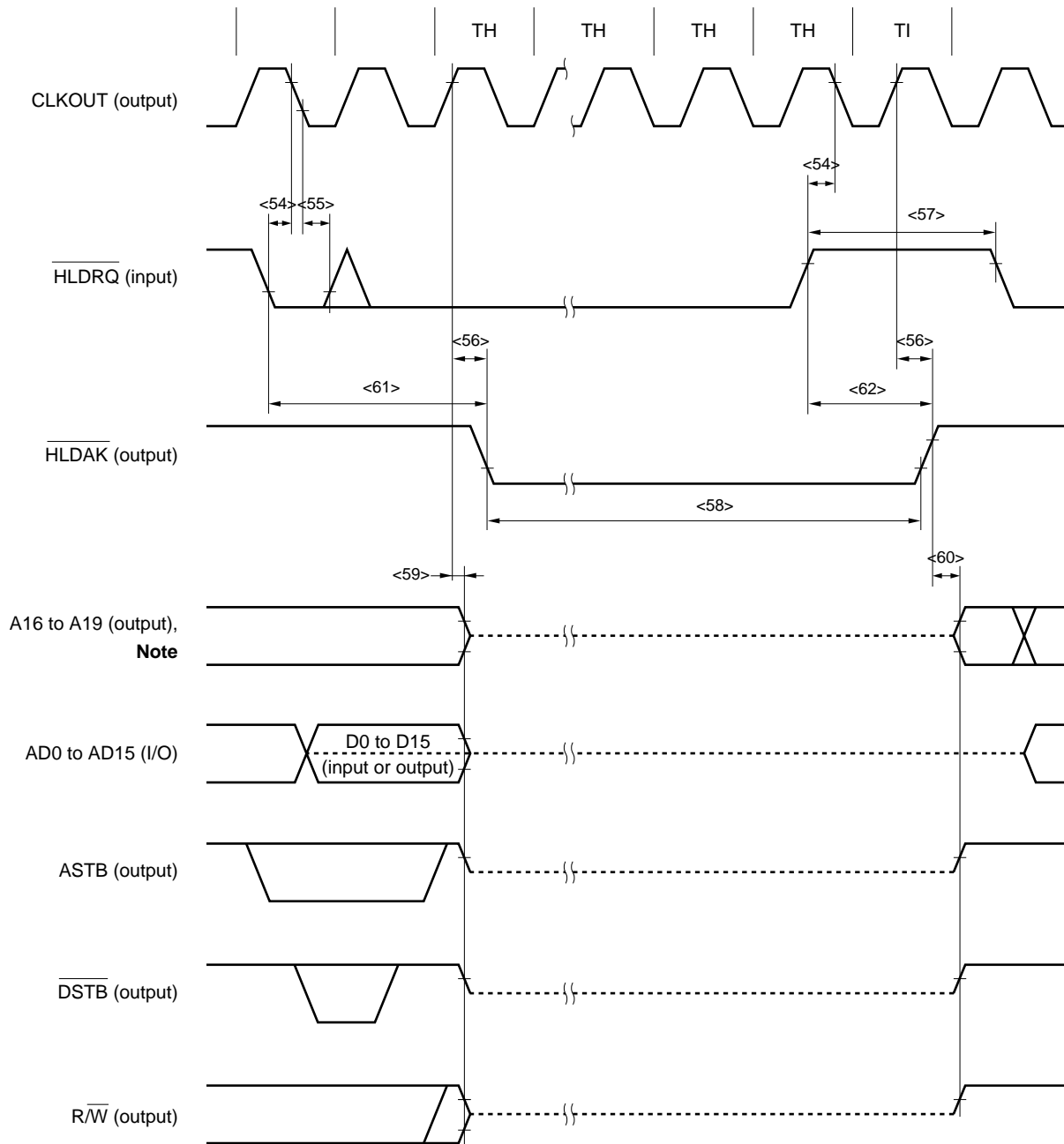
(7) Bus hold timing (1/2)

Parameter	Symbol		Conditions	25 MHz Version		33 MHz Version		Units
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT \downarrow)	<54>	t _{SHQK}		5		5		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT \downarrow)	<55>	t _{HKHQ}		5		5		ns
$\overline{\text{HLDAK}}$ delay time from CLKOUT \uparrow	<56>	t _{DKHA}			20		20	ns
$\overline{\text{HLDRQ}}$ high-level width	<57>	t _{WHQH}		T + 10		T + 10		ns
$\overline{\text{HLDAK}}$ low-level width	<58>	t _{WHAL}	-40°C ≤ T _A ≤ +70°C	T - 10		T - 10		ns
			70°C < T _A ≤ 85°C	T - 12		T - 12		ns
Delay time from CLKOUT \uparrow to bus float	<59>	t _{DKF}			20		20	ns
Delay time from $\overline{\text{HLDAK}}\uparrow$ to bus output	<60>	t _{DHAC}		-3		-3		ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	<61>	t _{DHQHA1}			(2n + 7.5)T + 20		(2n + 7.5)T + 20	ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	<62>	t _{DHQHA2}		0.5T	1.5T + 20	0.5T	1.5T + 20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks that are inserted during a bus cycle. The sampling timing may vary when using the programmable wait insertion function.

(7) Bus hold timing (2/2)



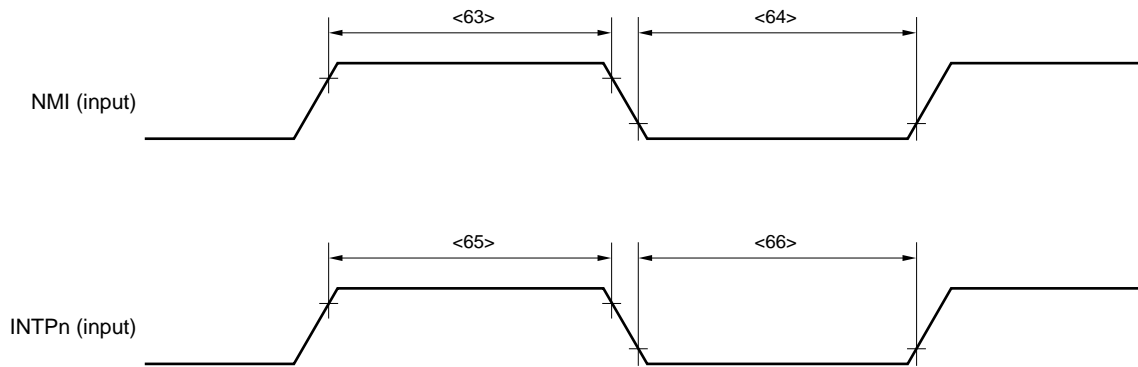
Note $\overline{\text{UBEN}}$ (output), $\overline{\text{LBEN}}$ (output)

Remark Broken lines indicate high impedance.

(8) Interrupt timing

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
NMI high-level width	<63> t_{WNIH}		500		500		ns
NMI low-level width	<64> t_{WNIL}		500		500		ns
INTPn high-level width	<65> t_{WITH}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3T + 10		3T + 10		ns
INTPn low-level width	<66> t_{WITL}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3T + 10		3T + 10		ns

Remark T = t_{CYK}



Remark n = 110 to 113, 120 to 123, 130 to 133, 140 to 143

(9) CSI timing (1/2)

(a) Master mode

(i) Timing of CSI0 to CSI2

Parameter	Symbol		Conditions	25 MHz Version		33 MHz Version		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SCKn}}$ cycle	<67>	t_{CYSK1}	Output	160		120		ns
$\overline{\text{SCKn}}$ high-level width	<68>	t_{WSKH1}	Output	$0.5t_{\text{CYSK1}} - 20$		$0.5t_{\text{CYSK1}} - 20$		ns
$\overline{\text{SCKn}}$ low-level width	<69>	t_{WSKL1}	Output	$0.5t_{\text{CYSK1}} - 20$		$0.5t_{\text{CYSK1}} - 20$		ns
SIn setup time (to $\overline{\text{SCKn}}\uparrow$)	<70>	t_{SSISK1}		30		30		ns
SIn hold time (from $\overline{\text{SCKn}}\uparrow$)	<71>	t_{HSKS11}		0		0		ns
SOn output delay time (from $\overline{\text{SCKn}}\downarrow$)	<72>	t_{DSKSO1}			18		18	ns
SOn output hold time (from $\overline{\text{SCKn}}\uparrow$)	<73>	t_{HSKSO1}		$0.5t_{\text{CYSK1}} - 5$		$0.5t_{\text{CYSK1}} - 5$		ns

Remark n = 0 to 2

(ii) Timing of CSI3

Parameter	Symbol		Conditions	25 MHz Version		33 MHz Version		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SCK3}}$ cycle	<67>	t_{CYSK3}	Output	$R_L = 1.5 \text{ k}\Omega$ $C_L = 50 \text{ pF}$	500		500	ns
$\overline{\text{SCK3}}$ high-level width	<68>	t_{WSKH3}	Output		$0.5t_{\text{CYSK3}} - 70$		$0.5t_{\text{CYSK3}} - 70$	ns
$\overline{\text{SCK3}}$ low-level width	<69>	t_{WSKL3}	Output		$0.5t_{\text{CYSK3}} - 70$		$0.5t_{\text{CYSK3}} - 70$	ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	<70>	t_{SSISK3}		100		100		ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	<71>	t_{HSKS13}		50		50		ns
SO3 output delay time (from $\overline{\text{SCK3}}\downarrow$)	<72>	t_{DSKSO3}	$R_L = 1.5 \text{ k}\Omega$ $C_L = 50 \text{ pF}$		150		150	ns
SO3 output hold time (from $\overline{\text{SCK3}}\uparrow$)	<73>	t_{HSKSO3}		$0.5t_{\text{CYSK3}} - 5$		$0.5t_{\text{CYSK3}} - 5$		ns

Remark R_L and C_L are the load resistance and load capacitance of the $\overline{\text{SCK3}}$ and SO3 output lines.

(b) Slave mode

(i) Timing of CSI0 to CSI2

Parameter	Symbol		Conditions	25 MHz Version		33 MHz Version		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SCKn}}$ cycle	<67>	t_{CYSK2}	Input	160		120		ns
$\overline{\text{SCKn}}$ high-level width	<68>	t_{WSKH2}	Input	50		30		ns
$\overline{\text{SCKn}}$ low-level width	<69>	t_{WSKL2}	Input	50		30		ns
SIn setup time (to $\overline{\text{SCKn}}\uparrow$)	<70>	t_{SSISK2}		10		10		ns
SIn hold time (from $\overline{\text{SCKn}}\uparrow$)	<71>	t_{HSKS12}		10		10		ns
SOn output delay time (from $\overline{\text{SCKn}}\downarrow$)	<72>	t_{DSKSO2}			30		30	ns
SOn output hold time (from $\overline{\text{SCKn}}\uparrow$)	<73>	t_{HSKSO2}		t_{WSKH2}		t_{WSKH2}		ns

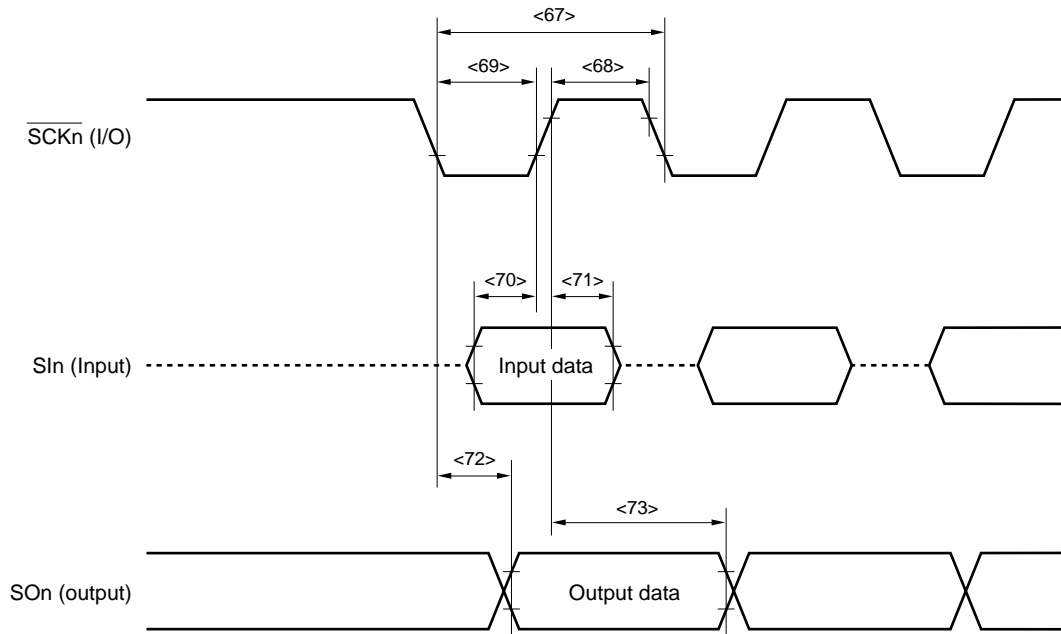
Remark n = 0 to 2

(9) CSI timing (2/2)

(ii) Timing of CSI3

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
SCK3 cycle	<67>	t _{CYSK4}	500		500		ns
SCK3 high-level width	<68>	t _{WSKH4}	180		180		ns
SCK3 low-level width	<69>	t _{WSKL4}	180		180		ns
SI3 setup time (to SCK3↑)	<70>	t _{SSISK4}	100		100		ns
SI3 hold time (from SCK3↑)	<71>	t _{HSKSI4}	50		50		ns
SO3 output delay time (from SCK3↓)	<72>	t _{DSKSO4}		150		150	ns
SO3 output hold time (from SCK3↑)	<73>	t _{HSKSO4}	t _{WSKH4}		t _{WSKH4}		ns

Remark R_L and C_L are the load resistance and load capacitance of the SCK3 and SO3 output lines.

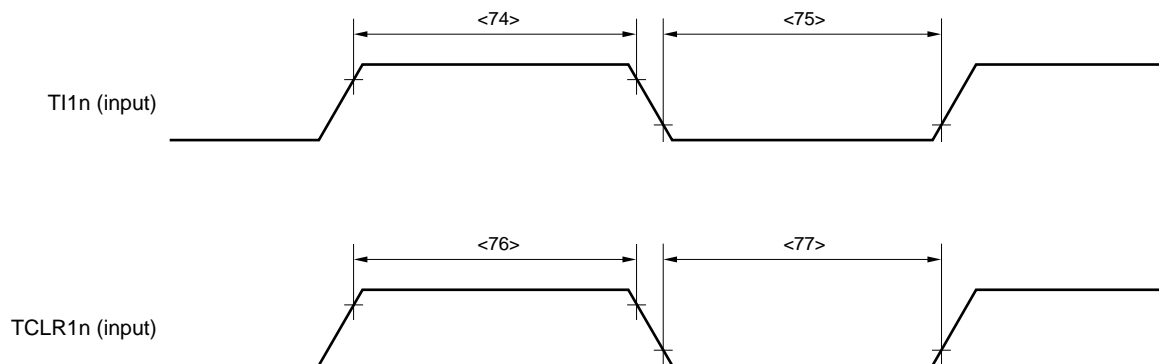


- Remarks**
1. Broken lines indicate high impedance.
 2. n = 0 to 3

(10) RPU timing

Parameter	Symbol	Conditions	25 MHz Version		33 MHz Version		Unit
			MIN.	MAX.	MIN.	MAX.	
T11n high-level width	<74> t_{WTH}		3T + 10		3T + 10		ns
T11n low-level width	<75> t_{WTL}		3T + 10		3T + 10		ns
TCLR1n high-level width	<76> t_{WTCH}		3T + 10		3T + 10		ns
TCLR1n low-level width	<77> t_{WTCL}		3T + 10		3T + 10		ns

Remark T = t_{cyk}



Remark n = 1 to 4

A/D Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	25 MHz Version			33 MHz Version			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Resolution	—		10	10	10	10	10	10	bit
Overall error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.4			±0.4	%FSR
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.7			±0.7	%FSR
Quantization error	—				±1/2			±1/2	LSB
Conversion time	t _{CONV}	4.5 V ≤ AV _{REF1} ≤ AV _{DD}	48			60			t _{CYK}
		3.5 V ≤ AV _{REF1} ≤ AV _{DD}	48			60			t _{CYK}
Sampling time	t _{SAMP}	4.5 V ≤ AV _{REF1} ≤ AV _{DD}	8			10			t _{CYK}
		3.5 V ≤ AV _{REF1} ≤ AV _{DD}	8			10			t _{CYK}
Zero-scale error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±3.5		±1.5	±3.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Full-scale error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5		±1.5	±2.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Non-linearity error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5		±1.5	±2.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5		±1.5	±4.5	LSB
Analog input voltage ^{Note 2}	V _{IAN}		-0.3		AV _{DD} + 0.3	-0.3		AV _{DD} + 0.3	V
Reference voltage	AV _{REF1}		3.5		AV _{DD}	3.5		AV _{DD}	V
AV _{REF1} current	AI _{REF1}			1.2	3.0		1.2	3.0	mA
AV _{DD} power supply current	AI _{DD}			2.3	6.0		2.3	6.0	mA

Notes 1. Excludes quantization error.

2. When V_{IAN} = 0, the conversion result becomes 000H.

When 0 < V_{IAN} < AV_{REF1}, conversion has 10-bit resolution.

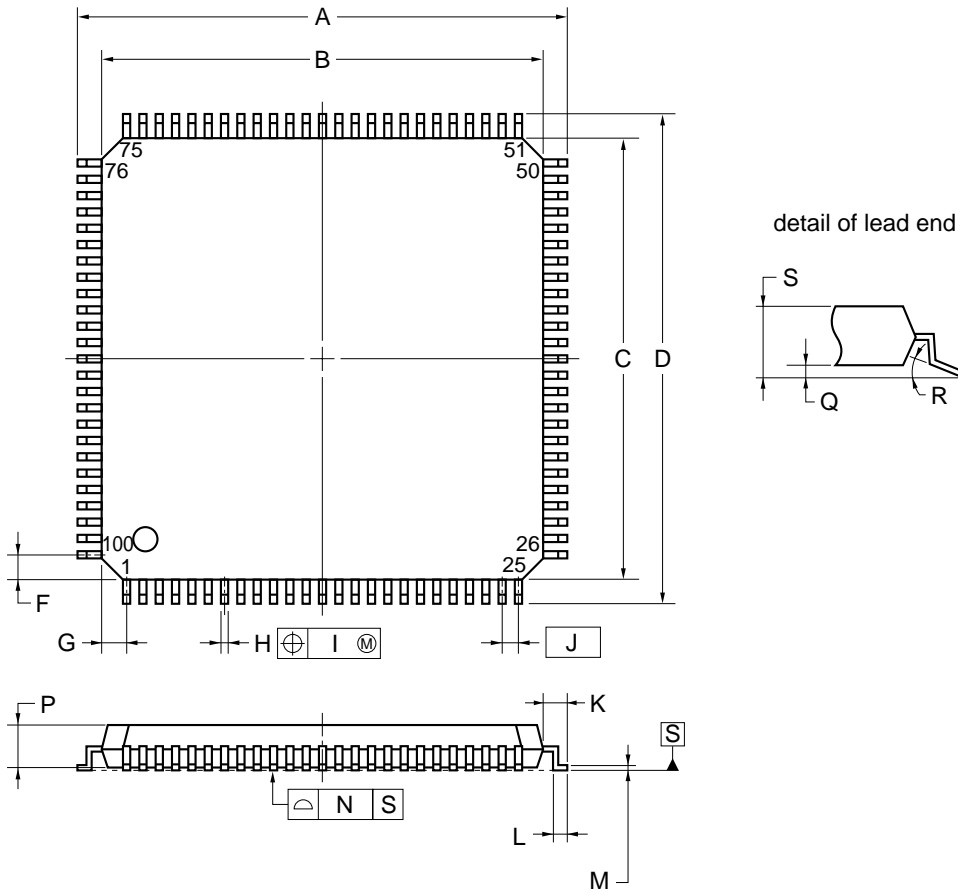
When AV_{REF1} ≤ V_{IAN} ≤ AV_{DD}, the conversion result becomes 3FFH.

D/A Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	25 MHz Version			33 MHz Version			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Resolution	—		8	8	8	8	8	8	bit
Overall error	—	Load condition: 2 MΩ, 30 pF AV _{REF2} = V _{DD} AV _{REF3} = 0			0.8			0.8	%
	—	Load condition: 2 MΩ, 30 pF AV _{REF2} = 0.75V _{DD} AV _{REF3} = 0.25V _{DD}			1.0			1.0	%
	—	Load condition: 4 MΩ, 30 pF AV _{REF2} = V _{DD} AV _{REF3} = 0			0.6			0.6	%
	—	Load condition: 4 MΩ, 30 pF AV _{REF2} = 0.75V _{DD} AV _{REF3} = 0.25V _{DD}			0.8			0.8	%
Settling time	—	Load condition: 2 MΩ, 30 pF			10			10	μs
Output resistance	RO			8		8			kΩ
AV _{REF2} input voltage	AV _{REF2}		0.75V _{DD}		V _{DD}	0.75V _{DD}		V _{DD}	V
AV _{REF3} input voltage	AV _{REF3}		0		0.25V _{DD}	0		0.25V _{DD}	V
Resistance between AV _{REF2} and AV _{REF3}	RA _{IREF}	DACS0, DACS1 = 55H	2	4		2	4		kΩ

★ 4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE
 Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 ^{+0.05} _{-0.04}
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° ^{+7°} _{-3°}
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

5. RECOMMENDED SOLDERING CONDITIONS

The μPD703003A, 703004A, and 703025A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representatives.

Table 5-1. Soldering Conditions

- μPD703003AGC-25-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
- μPD703003AGC-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
- μPD703004AGC-25-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
- μPD703004AGC-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
- μPD703025AGC-25-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)
- μPD703025AGC-33-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours)	VP15-107-2
Partial heating	Pin temperature: 300°C max., Time 3 seconds max. (per pin row)	—

Note After opening a dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

RELATED DOCUMENTS μ PD703003 Data Sheet (U12261E)
 μ PD70F3003 Data Sheet (U12036E)
 μ PD70F3003A, 70F3025A Data Sheet (U13189E)

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- Product release schedule
- Availability of related technical literature
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- Network requirements

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NEC Electronics Inc. (U.S.)

Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH

Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

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Fax: 01908-670-290

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Milano, Italy
Tel: 02-66 75 41
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Tel: 040-2445845
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Tel: 01-30-67 58 00
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Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.

Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.

Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.

United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.

Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.

Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

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