

54ACQ/74ACQ245 • 54ACTQ/74ACTQ245 Quiet Series Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

General Description

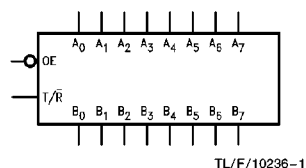
The 'ACQ/'ACTQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT245
- 4 kV minimum ESD immunity ('ACQ)
- Standard Military Drawing (SMD)
 - 'ACTQ245: 5962-8766303
 - 'ACQ245: 5962-92177

Logic Symbols



Pin Names	Description
OE	Output Enable Input
T/R	Transmit/Receive Input
A ₀ -A ₇	Side A TRI-STATE Inputs or TRI-STATE Outputs
B ₀ -B ₇	Side B TRI-STATE Inputs or TRI-STATE Outputs

Truth Table

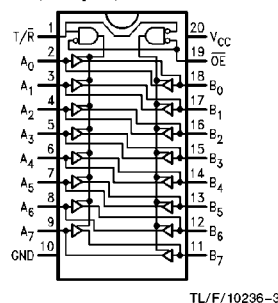
Inputs		Outputs
OE	T/R	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

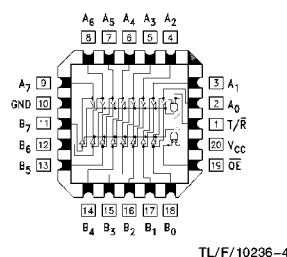
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Connection Diagrams

Pin Assignment for DIP, Flatpak, QSOP and SOIC



Pin Assignment for LCC



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	−20 mA
$V_I = -0.5V$	
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	−20 mA
$V_O = -0.5V$	
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to 6.0V
'ACQ	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACQ Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V _{CC} (V)	74ACQ		54ACQ		74ACQ		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		2.1		V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	3.15	3.15		3.15			
		5.5	2.75	3.85	3.85		3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		0.9		V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		4.5	2.25	1.35	1.35		1.35			
		5.5	2.75	1.65	1.65		1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		2.9		V	I _{OUT} = −50 μA
		4.5	4.49	4.4	4.4		4.4			
		5.5	5.49	5.4	5.4		5.4			
		3.0		2.56	2.4		2.46		V	*V _{IN} = V _{IL} or V _{IH} −12 mA I _{OH} −24 mA −24 mA
		4.5		3.86	3.7		3.76			
		5.5		4.86	4.7		4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1		0.1			
		5.5	0.001	0.1	0.1		0.1			
		3.0		0.36	0.50		0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5		0.36	0.50		0.44			
		5.5		0.36	0.50		0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		±1.0		μA	V _I = V _{CC} , GND (Note 1)

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACQ		54ACQ	74ACQ	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
I _{OLD}	† Minimum Dynamic Output Current	5.5			50	75	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5			−50	−75	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	V _{IN} = V _{CC} or GND (Note 1)
I _{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±5.5	±3.0	μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5			V	Figures 2-12, 13 (Notes 2, 3)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	−0.6	−1.2			V	Figures 2-12, 13 (Notes 2,3)
V _{IHD}	minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IH} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}. I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V _{CC} (V)	74ACTQ		54ACTQ	74ACTQ	Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C	T _A = −40°C to +85°C		
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	2.0	2.0	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	V _{OUT} = 0.1V or V _{CC} − 0.1V
		5.5	1.5	0.8	0.8	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	4.4	V	I _{OUT} = −50 μA
		5.5	5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	*V _{IN} = V _{IL} or V _{IH} −24 mA I _{OH} −24 mA
		5.5		4.86	4.70	4.76		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5		0.36	0.50	0.44		
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	V _I = V _{CC} , GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	74ACTQ		54ACTQ		74ACTQ		Units	Conditions
			T _A = +25°C		T _A = −55°C to +125°C		T _A = −40°C to +85°C			
			Typ	Guaranteed Limits						
I _{OZT}	Maximum TRI-STATE Leakage Current	5.5		±0.3	±5.5	±3.0		μA	V _I = V _{IL} , V _{IH} V _O = V _{CC} , GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.6	1.5		mA	V _I = V _{CC} − 2.1V	
I _{OLD}	†Minimum Dynamic Output Current	5.5			50	75		mA	V _{OLD} = 1.65V Max	
I _{OHD}		5.5			−50	−75		mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0		μA	V _{IN} = V _{CC} or GND (Note 1)	
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.1	1.5				V	Figures 2-12, 13 (Notes 2, 3)	
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	−0.6	−1.2				V	Figures 2-12, 13 (Notes 2, 3)	
V _{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2				V	(Notes 2, 4)	
V _{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8				V	(Notes 2, 4)	

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). n − 1 Data Inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 3V (ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACQ			54ACQ		74ACQ		Units
			T _A = +25°C C _L = 50 pF			T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	3.3 5.0	2.0 1.5	7.5 5.0	10.0 6.5	1.0 1.0	11.5 8.5	2.0 1.5	10.5 7.0	ns
t _{PZL} , t _{PZH}	Output Enable Time	3.3 5.0	3.0 2.0	8.5 6.0	13.0 8.5	1.0 1.0	13.0 10.0	3.0 2.0	13.5 9.0	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.5 7.5	14.5 9.5	1.0 1.0	13.0 10.0	1.0 1.0	15.0 10.0	ns
t _{OSHL} , t _{OSLH}	Output to Output Skew** Data to Output	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACTQ			54ACTQ		74ACTQ		Units
			T _A = +25°C C _L = 50 pF			T _A = −55°C to +125°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay Data to Output	5.0	1.5	5.5	7.0	1.5	9.0	1.5	7.5	ns
t _{PZL} , t _{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	1.5	12.0	2.0	9.5	ns
t _{PHZ} , t _{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.0	11.5	1.0	10.5	ns
t _{OSHL} , t _{OSLH}	Output to Output Skew** Data to Output	5.0		0.5	1.0				1.0	ns

*Voltage Range 5.0 is 5.0V ± 0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{I/O}	Input/Output Capacitance	15	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	80.0	pF	V _{CC} = 5.0V

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.

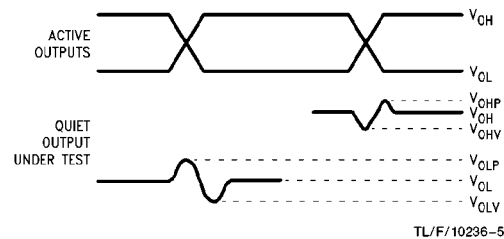


FIGURE 8. Quiet Output Noise Voltage Waveforms

Note A. V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B. Input pulses have the following characteristics: $f = 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

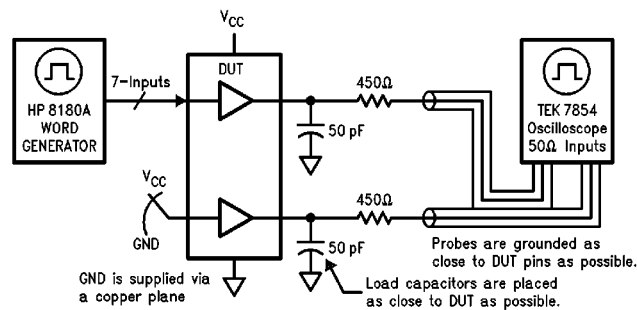


FIGURE 9. Simultaneous Switching Test Circuit

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

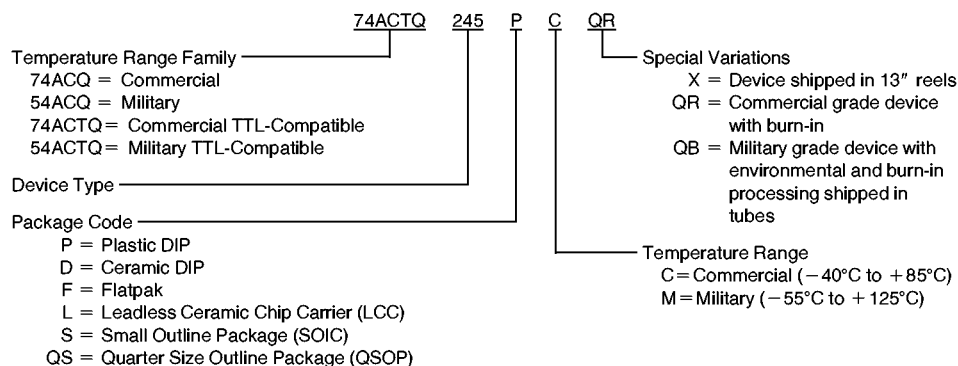
- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

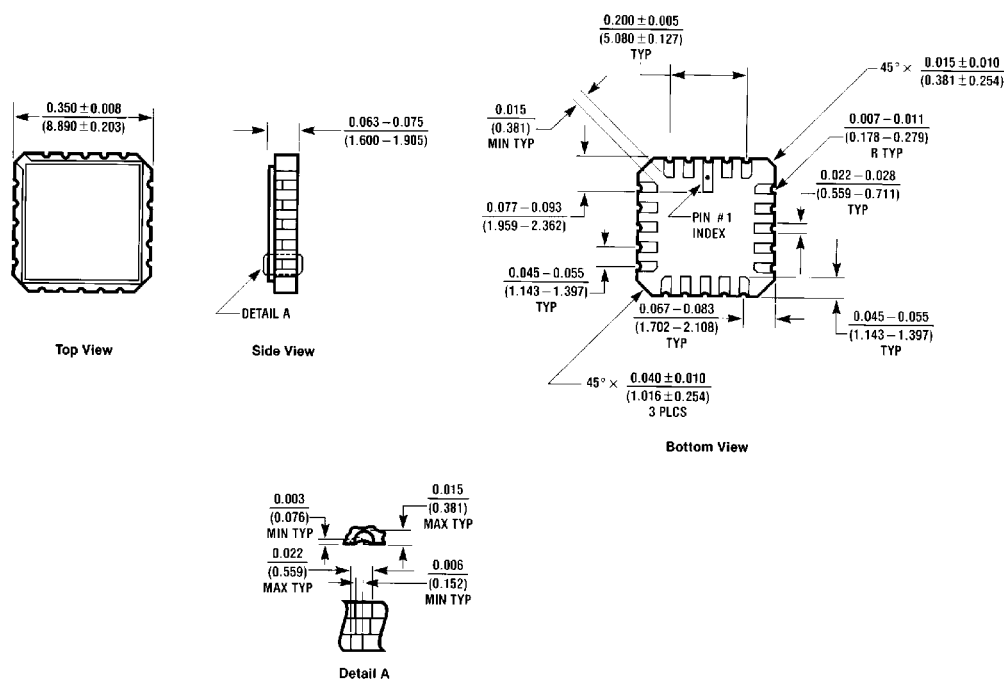
- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



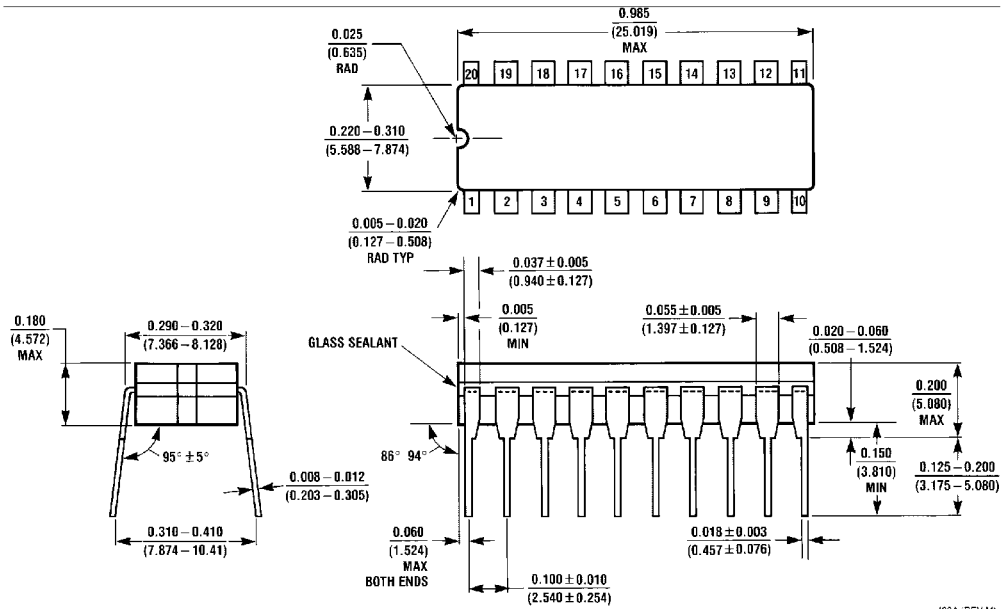
Physical Dimensions inches (millimeters)



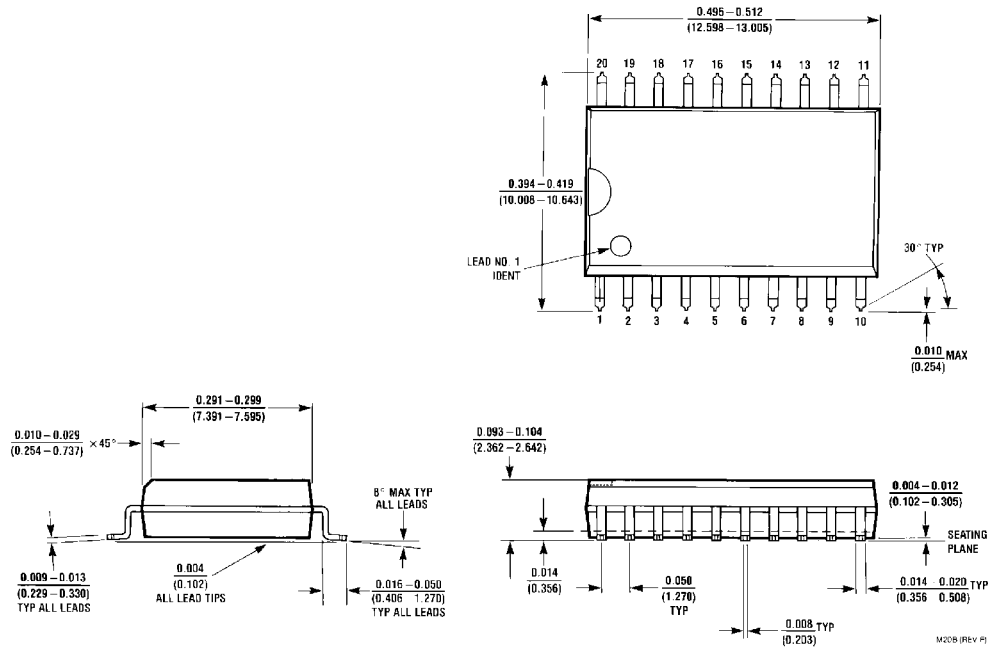
**20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

6204 (REV D)

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

The drawing illustrates the MQA20 package, a 20-lead quarter size outline package (QS). It includes three views: a top view, a side view, and a detail view of the lead profile.

Top View Dimensions:

- Overall width: 0.341 ± 0.003 [-A-]
- Lead pitch: 0.040 ± 0.005
- Lead width: 0.050 ± 0.005
- Lead diameter: $\varnothing 0.030 \pm 0.002$
- Body width: 0.152 ± 0.003 (TOP) and 0.154 ± 0.003 (BOT)
- Overall height: 0.236 ± 0.005

Side View Dimensions:

- Lead height: 0.057 ± 0.002
- Lead thickness: 0.026 ± 0.002
- Body thickness: 0.058 ± 0.002
- Lead thickness (bottom): 0.025 TYP
- Lead thickness (top): 0.063 ± 0.005 TYP
- Lead thickness (bottom): 0.006 ± 0.002 TYP
- Lead thickness (top): 0.010 ± 0.002 TYP
- Lead thickness (bottom): 0.007 (M)
- Lead thickness (top): 0.007 (C)
- Lead thickness (bottom): 0.007 (A)
- Lead thickness (top): 0.007 (S)

Detail View Dimensions:

- Lead profile: $45^\circ \times 0.015$
- Lead thickness: 0.010 TYP
- Lead thickness: 0.007 TYP
- Lead thickness: 0.026 ± 0.002 TYP
- Lead thickness: $5^\circ \pm 3^\circ$ TYP

Other Features:

- SEATING PLANE
- 0.004 (C)
- 0.004 (A)

Package Identification:

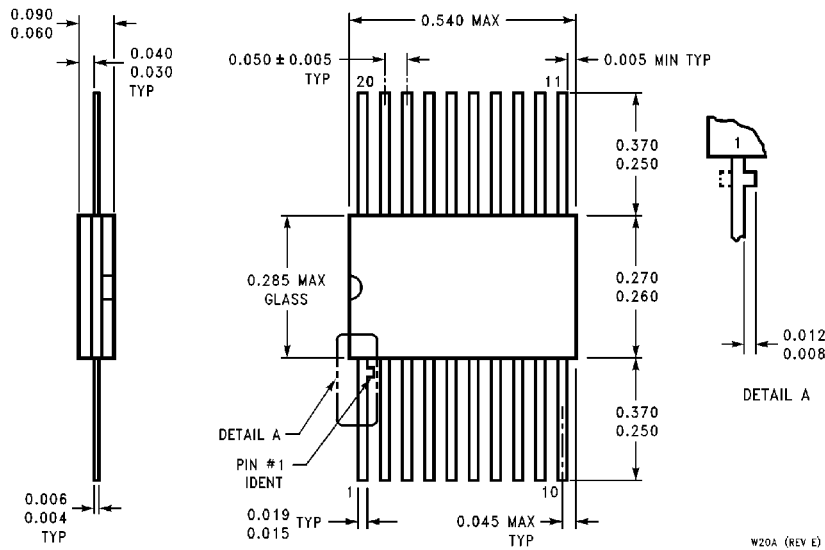
20-Lead Quarter Size Outline Package (QS)
NS Package Number MQA20

MQA20 (REV A)



Physical Dimensions inches (millimeters) (Continued)

Lit. # 114675



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livy-Gargan-Str. 10
D-82256 Fürstfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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