4-Mbit (256K x 16) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.20V–3.60V
- Pin compatible with CY62146DV30
- Ultra low standby power
  - Typical standby current: 1 μA
  - Maximum standby current: 7 μA
- Ultra low active power
  - Typical active current: 2 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in a Pb-free 48-ball VFBGA and 44-pin TSOP II packages

Functional Description [1]

The CY62146EV30 is a high performance CMOS static RAM organized as 256K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The input and output pins (IO_0 through IO_{15}) are placed in a high impedance state when:

- Deselected ($\overline{CE}$ HIGH)
- Outputs are disabled ($\overline{OE}$ HIGH)
- Both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH)
- Write operation is active ($\overline{CE}$ LOW and $\overline{WE}$ LOW)

Write to the device by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

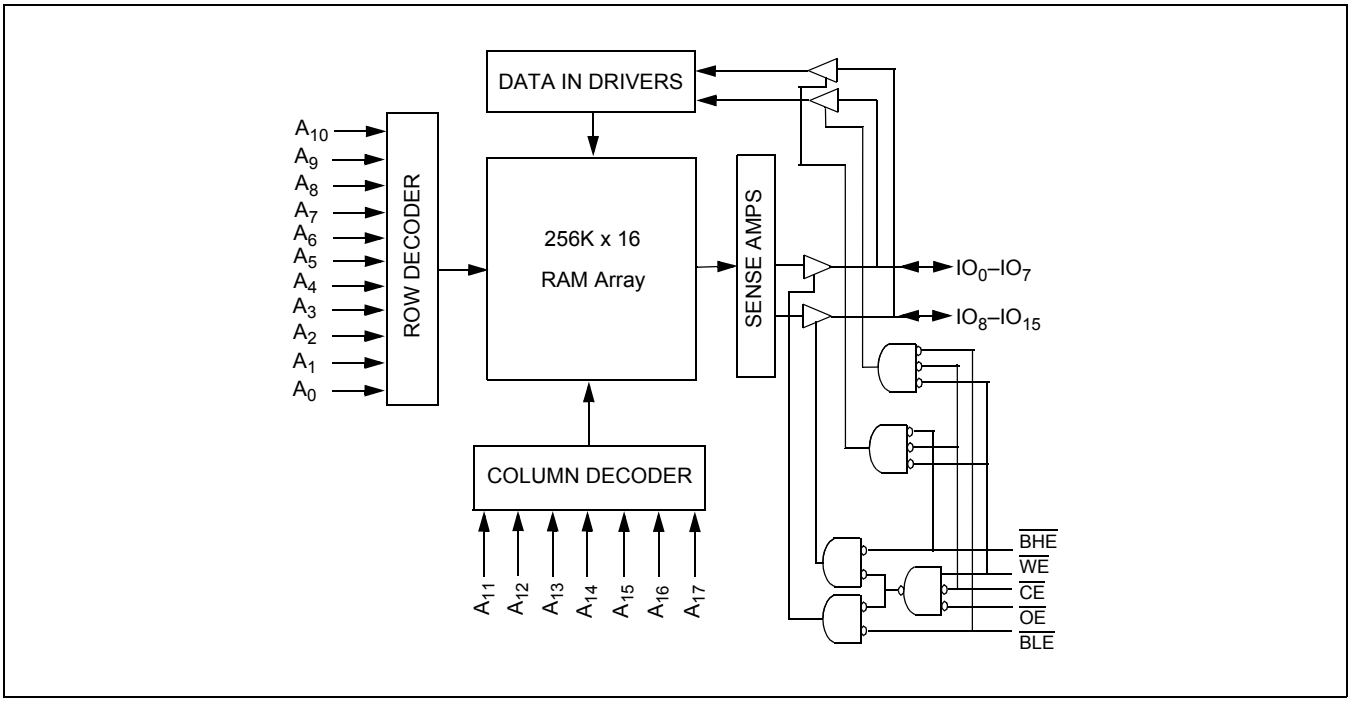
Read from the device by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the "Truth Table" on page 9 for a complete description of read and write modes.

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62146EV30LL	2.2	3.0	3.6	45 ns	2	2.5	15	20	1	7

Notes:
1. For best practice recommendations, please refer to the Cypress application note *System Design Guidelines* on http://www.cypress.com.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

Logic Block Diagram



Pin Configurations [3, 4]

48-ball VFBGA
Top View

	1	2	3	4	5	6	
A	$\overline{BLE}$	$\overline{OE}$	A_0	A_1	A_2	NC	A
B	IO_8	$\overline{BHE}$	A_3	A_4	$\overline{CE}$	IO_0	B
C	IO_9	IO_{10}	A_5	A_6	IO_1	IO_2	C
D	V_{SS}	IO_{11}	A_{17}	A_7	IO_3	V_{CC}	D
E	V_{CC}	IO_{12}	NC	A_{16}	IO_4	V_{SS}	E
F	IO_{14}	IO_{13}	A_{14}	A_{15}	IO_5	IO_6	F
G	IO_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	IO_7	G
H	NC	A_8	A_9	A_{10}	A_{11}	NC	H

44-pin TSOP II
Top View

A_4	1	44	A_5
A_3	2	43	A_6
A_2	3	42	A_7
A_1	4	41	$\overline{OE}$
A_0	5	40	$\overline{BHE}$
$\overline{CE}$	6	39	$\overline{BLE}$
IO_0	7	38	IO_{15}
IO_1	8	37	IO_{14}
IO_2	9	36	IO_{13}
IO_3	10	35	IO_{12}
V_{CC}	11	34	V_{SS}
V_{SS}	12	33	V_{CC}
IO_4	13	32	IO_{11}
IO_5	14	31	IO_{10}
IO_6	15	30	IO_9
IO_7	16	29	IO_8
$\overline{WE}$	17	28	NC
A_{17}	18	27	A_8
A_{16}	19	26	A_9
A_{15}	20	25	A_{10}
A_{14}	21	24	A_{11}
A_{13}	22	23	A_{12}

Notes:
3. NC pins are not connected on the die.
4. Pins H1, G2, and H6 in the BGA package are address expansion pins for 8 Mb, 16 Mb and 32 Mb, respectively.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential .....–0.3V to + 3.9V (V_{CCmax} + 0.3V)

DC Voltage Applied to Outputs in High-Z State [5, 6].....–0.3V to 3.9V (V_{CCmax} + 0.3V)

DC Input Voltage [5, 6]..... –0.3V to 3.9V ($V_{CC\ max}$ + 0.3V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [7]
CY62146EV30	Industrial	–40°C to +85°C	2.2V to 3.6V

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [2]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA		2.0			V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70V		2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA				0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70V				0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3	V
		V_{CC}= 2.7V to 3.6V		2.2		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V		–0.3		0.6	V
		V_{CC}= 2.7V to 3.6V		–0.3		0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$		–1		+1	µA
I_{OZ}	Output Leakage Current	GND $\leq V_O \leq V_{CC}$, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels		15	20	mA
		f = 1 MHz			2	2.5	
I_{SB1}	Automatic CE Power down Current — CMOS Inputs	$\overline{CE} \geq V_{CC}$–0.2V, $V_{IN} \geq V_{CC}$–0.2V or $V_{IN} \leq$ 0.2V f = f_{max} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$ and $\overline{WE}$), V_{CC} = 3.60V			1	7	µA
I_{SB2} [8]	Automatic CE Power down Current — CMOS Inputs	$\overline{CE} \geq V_{CC}$ – 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, V_{CC} = 3.60V			1	7	µA

Notes:

5. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
6. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
7. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.
8. Only chip enable ($\overline{CE}$) and byte enables ($\overline{BHE}$ and $\overline{BLE}$) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

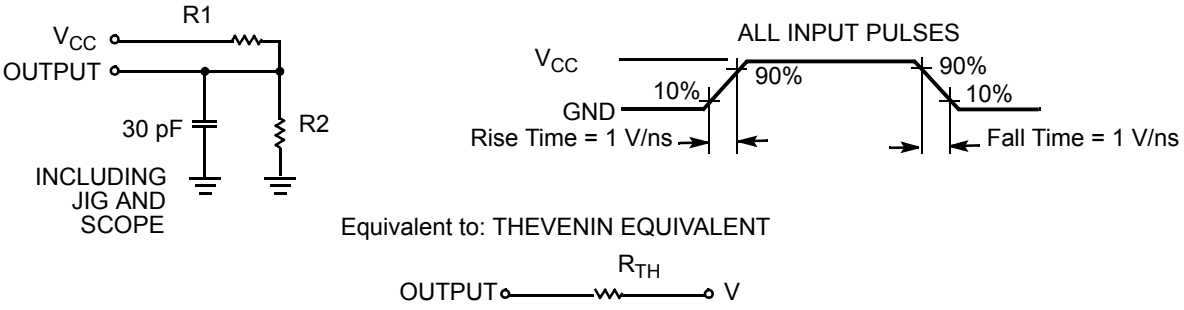
Capacitance (For All Packages) [9]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance [9]

Parameter	Description	Test Conditions	VFBGA Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	75	77	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		10	13	°C/W

AC Test Loads and Waveforms

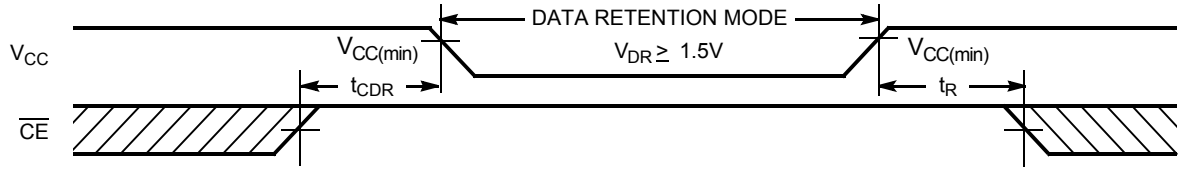


Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min	Typ [2]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR} [8]	Data Retention Current	V_{CC} = 1.5V, $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		0.8	7	µA
t_{CDR} [9]	Chip Deselect to Data Retention Time		0			ns
t_R [10]	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Notes:
9. Tested initially and after any design or process changes that may affect these parameters.
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

Switching Characteristics (Over the Operating Range) [11, 12]

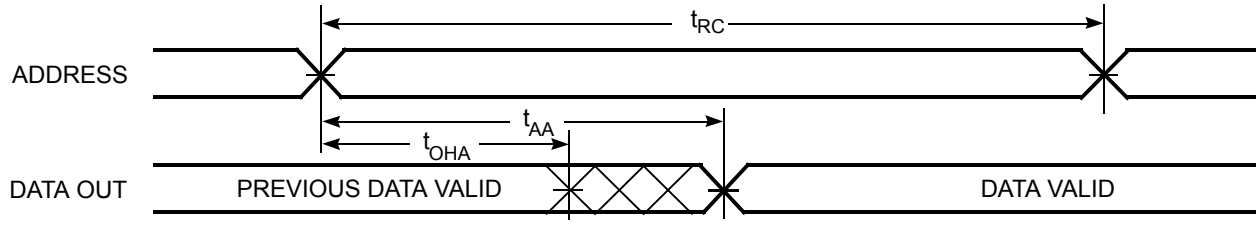
Parameter	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	45		ns
t_{AA}	Address to Data Valid		45	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z [13]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z [13, 14]		18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z [13]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z [13, 14]		18	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		45	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Data Valid		22	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low-Z [13]	5		ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to High-Z [13, 14]		18	ns
Write Cycle [15]				
t_{WC}	Write Cycle Time	45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	35		ns
t_{AW}	Address Setup to Write End	35		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Write End	35		ns
t_{SD}	Data Setup to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z [13, 14]		18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z [13]	10		ns

Notes:

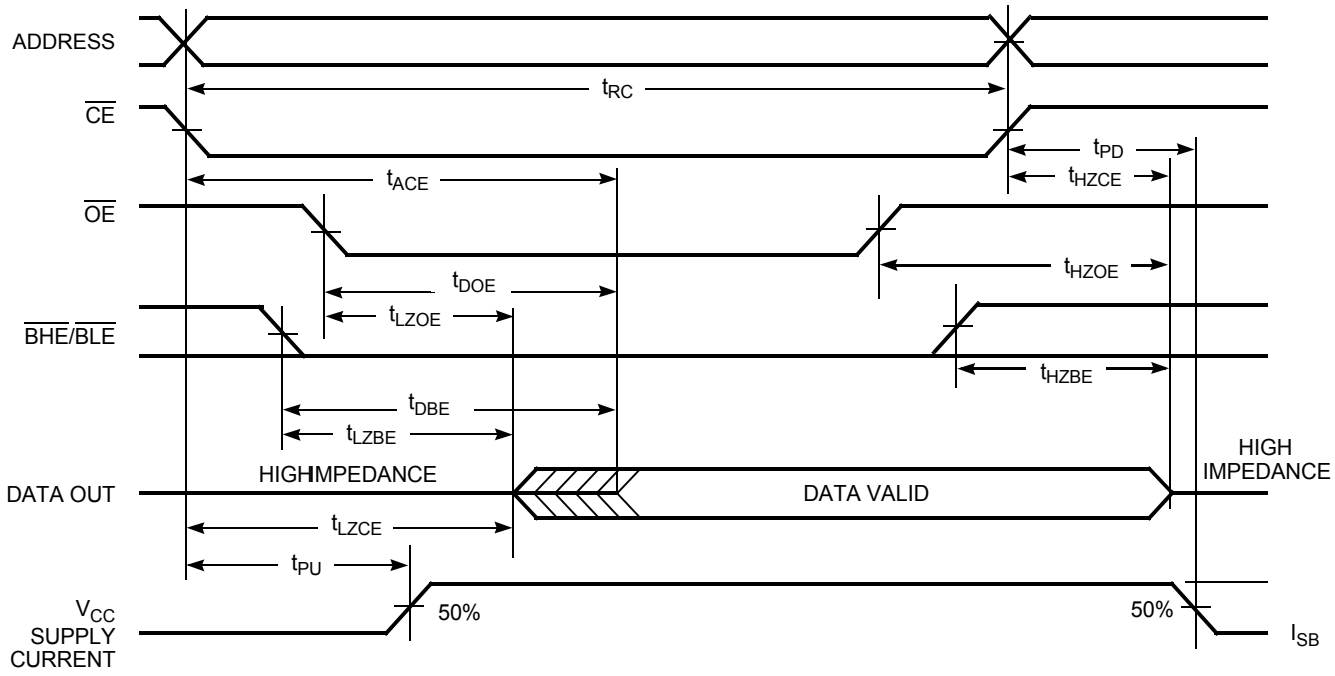
11. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" on page 4.
12. AC timing parameters are subject to byte enable signals ($\overline{BHE}$ or $\overline{BLE}$) not switching when chip is disabled. Please see application note AN13842 for further clarification.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
15. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled) [16, 17]



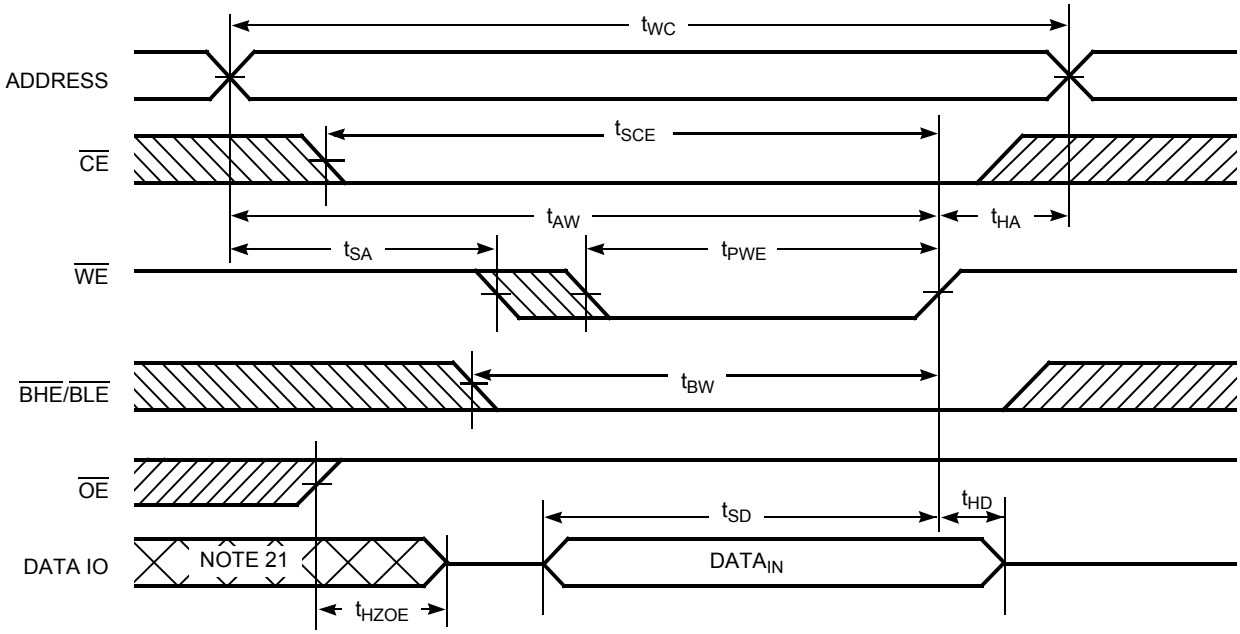
Read Cycle No. 2 ($\overline{OE}$ Controlled) [17, 18]



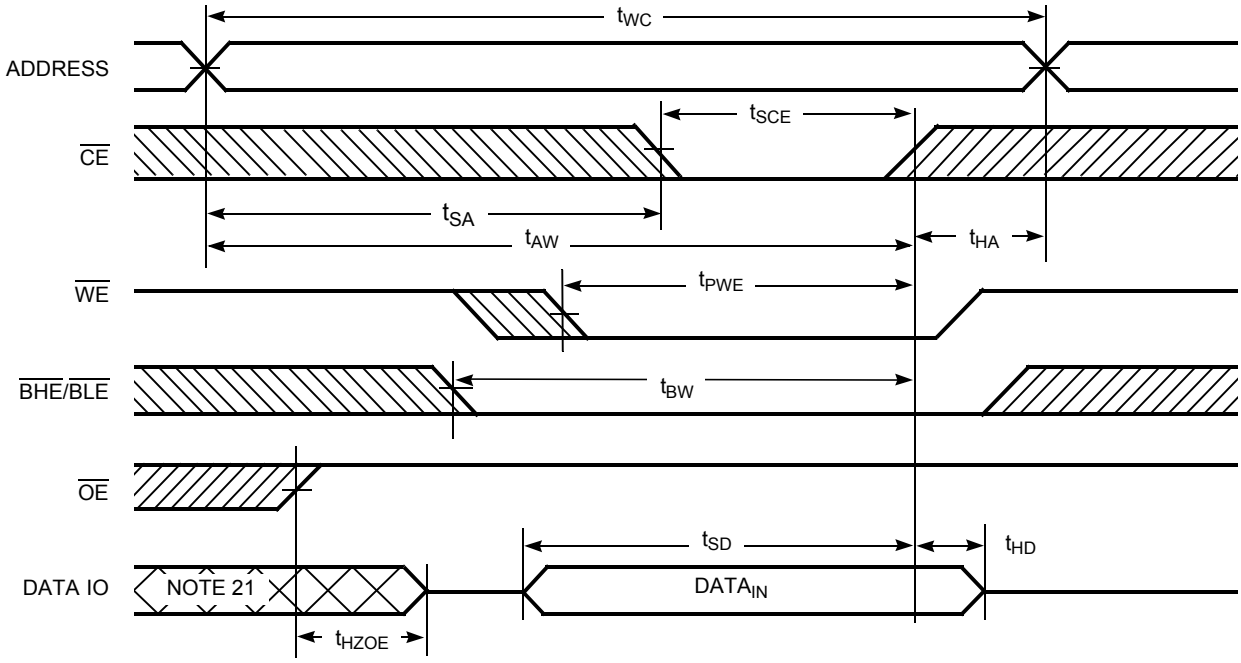
Notes:
16. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
17. $\overline{WE}$ is HIGH for read cycle.
18. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled) [15, 19, 20]



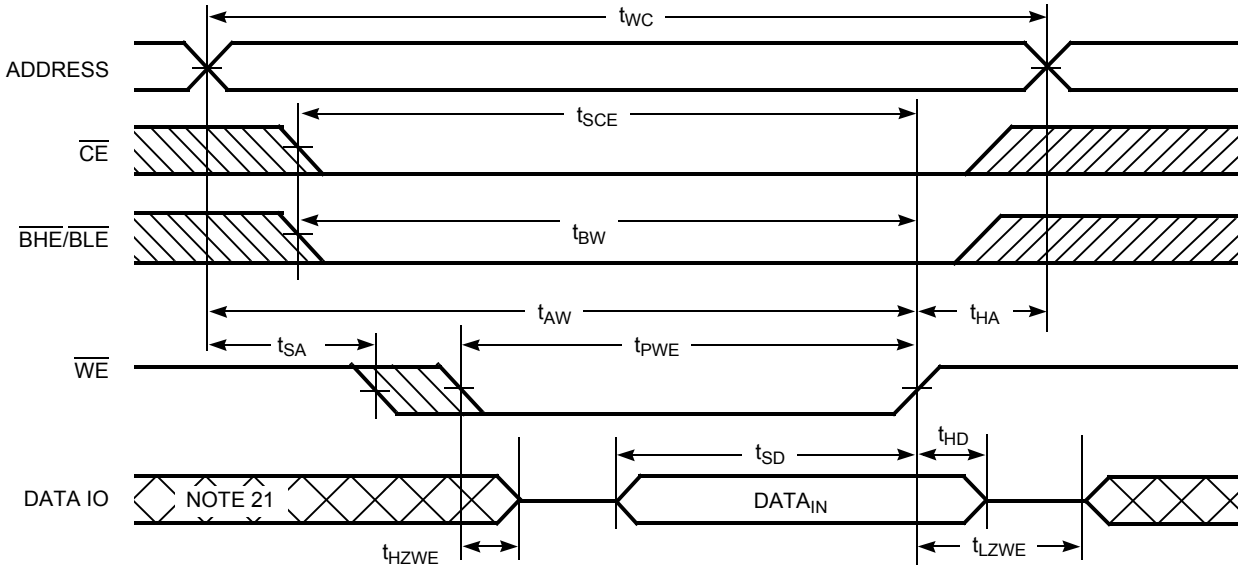
Write Cycle No. 2 ($\overline{CE}$ Controlled) [15, 19, 20]



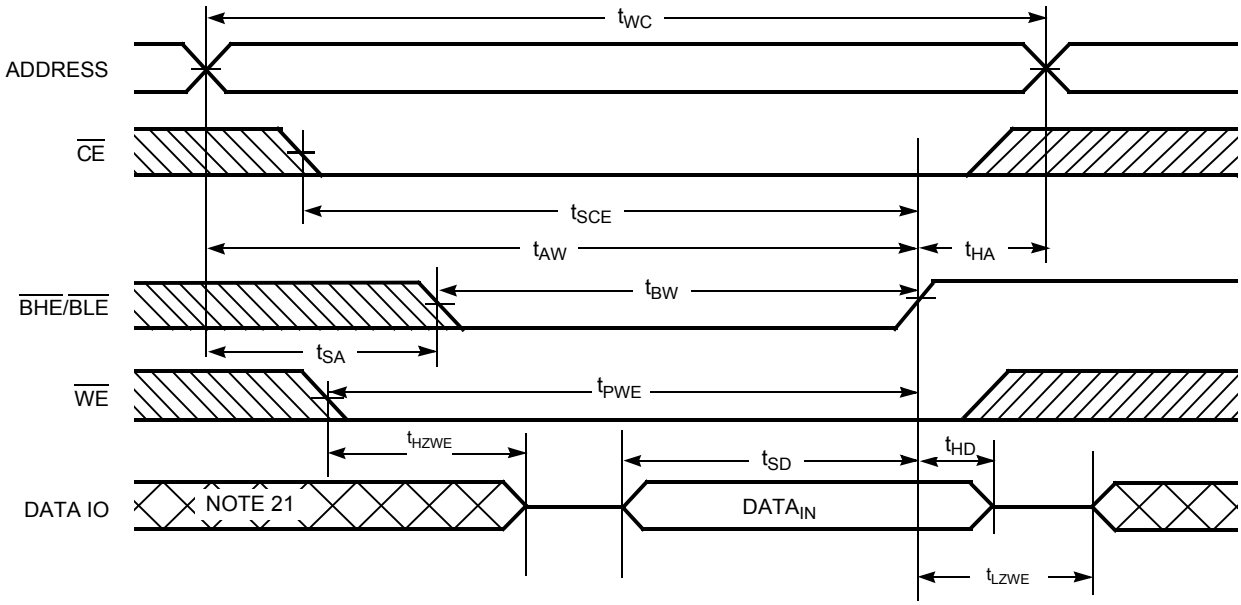
Notes:
19. Data IO is high impedance if $\overline{OE}$ = V_{IH}.
20. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
21. During this period, the IOs are in output state and input signals must not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (WE Controlled, OE LOW) [20]



Write Cycle No. 4 (BHE/BLE Controlled, OE LOW) [20]



Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (IO_0–IO_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (IO_0–IO_7); IO_8–IO_{15} in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (IO_8–IO_{15}); IO_0–IO_7 in High-Z	Read	Active (I_{CC})
L	H	H	L	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (IO_0–IO_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (IO_0–IO_7); IO_8–IO_{15} in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (IO_8–IO_{15}); IO_0–IO_7 in High-Z	Write	Active (I_{CC})

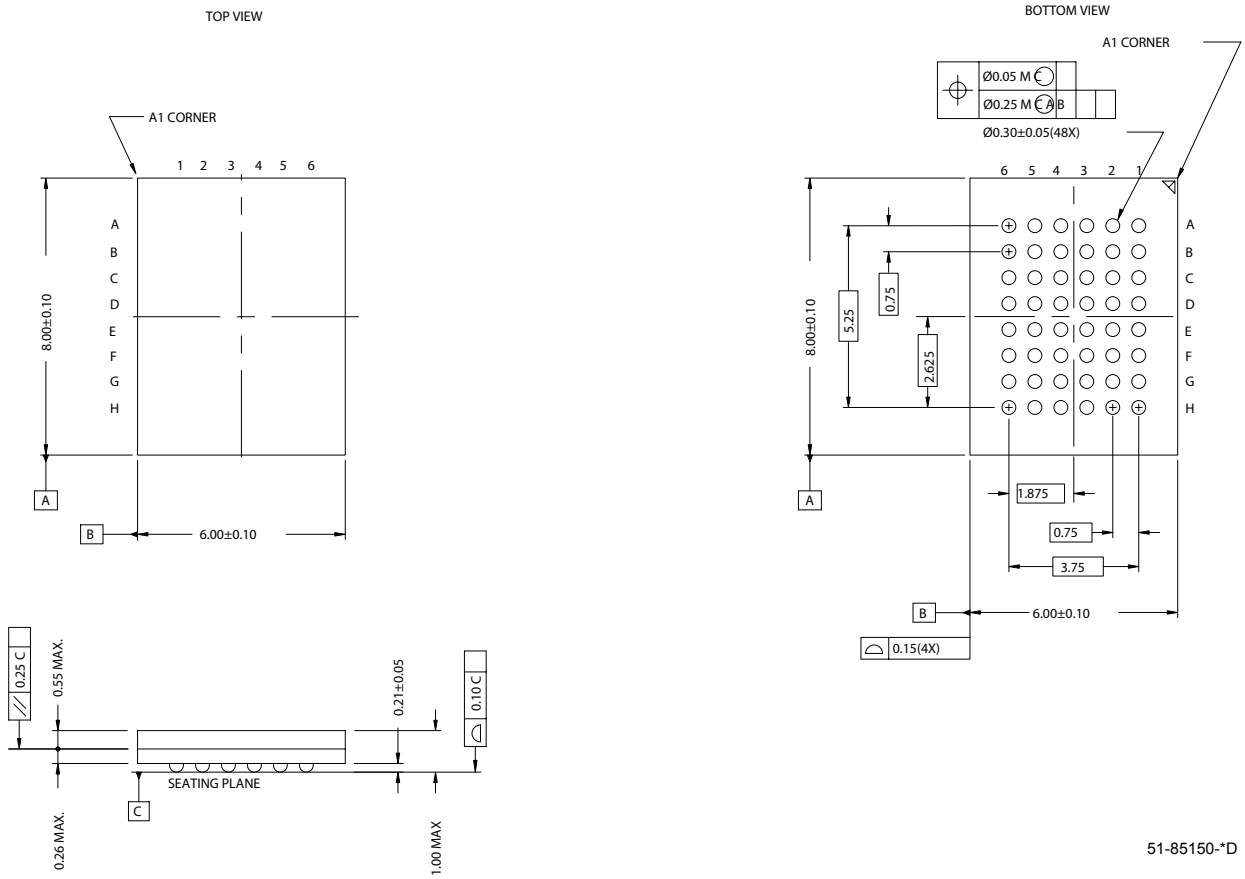
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62146EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial
	CY62146EV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	

Please contact your local Cypress sales representative for availability of other parts

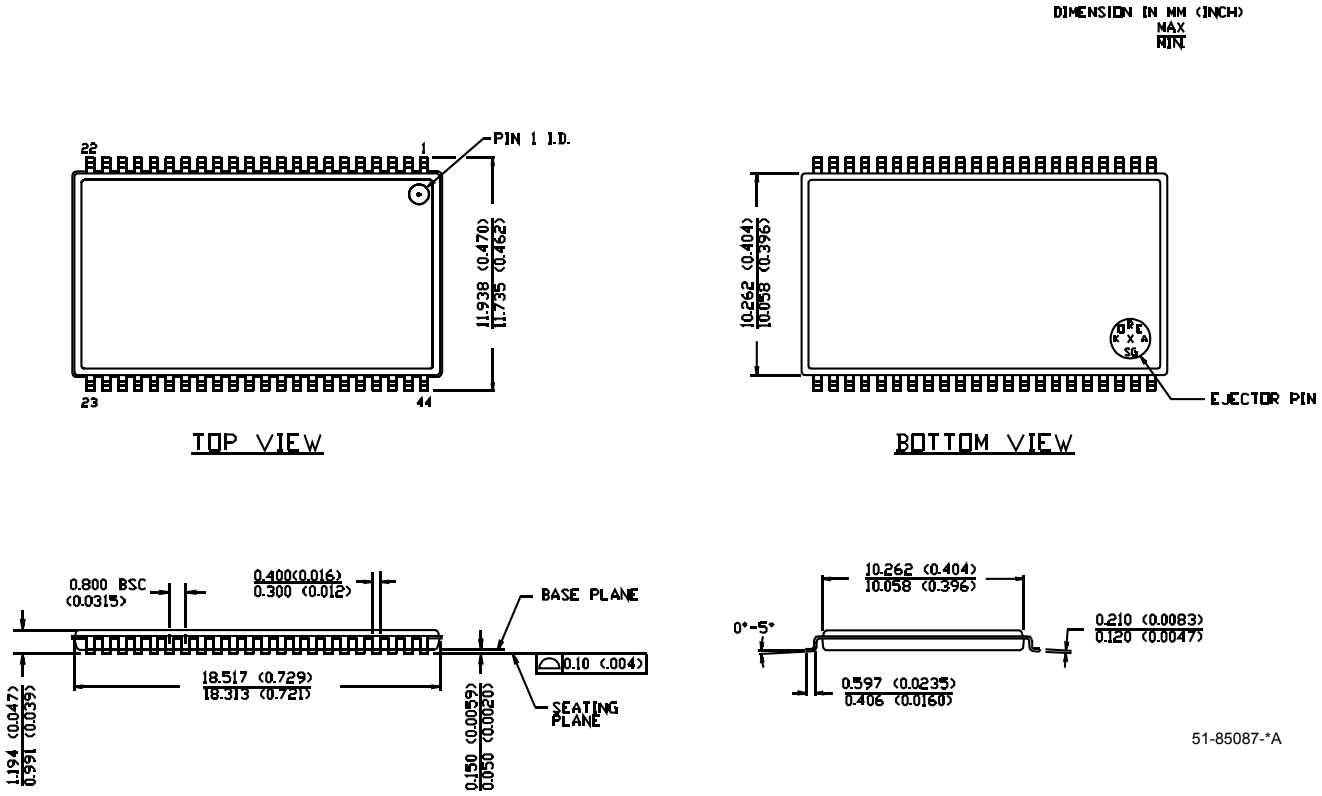
Package Diagrams

Figure 1. 48-ball VFBGA (6 x 8 x 1 mm), 51-85150



Package Diagrams (continued)

Figure 2. 44-pin TSOP II, 51-85087



Document History Page

Document Title:CY62146EV30 MoBL®, 4-Mbit (256K x 16) Static RAM Document Number: 38-05567				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	223225	See ECN	AJU	New Data Sheet
*A	247373	See ECN	SYT	Changed Advance Information to Preliminary Moved Product Portfolio to Page 2 Changed V_{CC} stabilization time in footnote #8 from 100 μs to 200 μs Removed Footnote #14(t_{LZBE}) from Previous revision Changed I_{CCDR} from 2.0 μA to 2.5 μA Changed typo in Data Retention Characteristics(t_R) from 100 μs to t_{RC} ns Changed t_{OHA} from 6 ns to 10 ns for both 35 ns and 45 ns Speed Bin Changed t_{HZOE}, t_{HZBE}, t_{HZWE} from 12 to 15 ns for 35 ns Speed Bin and 15 to 18 ns for 45 ns Speed Bin Changed t_{SCE} and t_{BW} from 25 to 30 ns for 35 ns Speed Bin and 40 to 35 ns for 45 ns Speed Bin Changed t_{HZCE} from 12 to 18 ns for 35 ns Speed Bin and 15 to 22 ns for 45 ns Speed Bin Changed t_{SD} from 15 to 18 ns for 35 ns Speed Bin and 20 to 22 ns for 45 ns Speed Bin Changed t_{DOE} from 15 to 18 ns for 35 ns Speed Bin Changed t_{DBE} from 15 to 18 ns for 35 ns Speed Bin Changed Ordering Information to include Pb-Free Packages
*B	414807	See ECN	ZSD	Changed from Preliminary information to Final Changed the address of Cypress Semiconductor Corporation on Page #1 from “3901 North First Street” to “198 Champion Court” Removed 35ns Speed Bin Removed “L” version of CY62146EV30 Changed ball E3 from DNU to NC Removed the redundant foot note on DNU. Changed I_{CC} (Max) value from 2 mA to 2.5 mA and I_{CC} (Typ) value from 1.5 mA to 2 mA at f=1 MHz Changed I_{CC} (Typ) value from 12 mA to 15 mA at f = f_{max} Changed I_{SB1} and I_{SB2} Typ values from 0.7 μA to 1 μA and Max values from 2.5 μA to 7 μA. Changed the AC test load capacitance from 50pF to 30pF on Page# 4 Changed I_{CCDR} from 2.5 μA to 7 μA. Added I_{CCDR} typical value. Changed t_{LZOE} from 3 ns to 5 ns Changed t_{LZCE} and t_{LZWE} from 6 ns to 10 ns Changed t_{LZBE} from 6 ns to 5 ns Changed t_{HZCE} from 22 ns to 18 ns Changed t_{PWE} from 30 ns to 35 ns. Changed t_{SD} from 22 ns to 25 ns. Updated the package diagram 48-ball VFBGA from *B to *D Updated the ordering information table and replaced the Package Name column with Package Diagram.
*C	925501	See ECN	VKN	Added footnote #8 related to I_{SB2} and I_{CCDR} Added footnote #12 related AC timing parameters