ELPIDA

PRELIMINARY DATA SHEET

512M bits DDR-II SDRAM

EDE5104GBSA (128M words × 4 bits)
EDE5108GBSA (64M words × 8 bits)
EDE5116GBSA (32M words × 16 bits)

Description

The EDE5104GB is a 512M bits DDR-II SDRAM organized as 33,554,432 words × 4 bits × 4 banks.

The EDE5108GB is a 512M bits DDR-II SDRAM organized as 16,777,216 words × 8 bits × 4 banks.

It packaged in 64-ball μBGA® package.

The EDE5116GB is a 512M bits DDR-II SDRAM organized as 8,388,608 words × 16 bits × 4 banks.

It is packaged in 84-ball μBGA package.

Features

- 1.8V power supply
- Double-data-rate architecture: two data transfers per clock cycle
- Bi-directional, differential data strobe (DQS and /DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge aligned with data for READs: center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge: data and data mask referenced to both edges of DQS
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths: 4, 8
- /CAS Latency (CL): 3, 4, 5
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- 7.8μs average periodic refresh interval
- 1.8V (SSTL_18 compatible) I/O
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver Impedance Adjustment and On-Die-Termination for better signal quality
- Programmable RDQS, /RDQS output for making × 8 organization compatible to × 4 organization
- /DQS, (/RDQS) can be disabled for single-ended Data Strobe operation.
- μBGA package is lead free solder (Sn-Ag-Cu)

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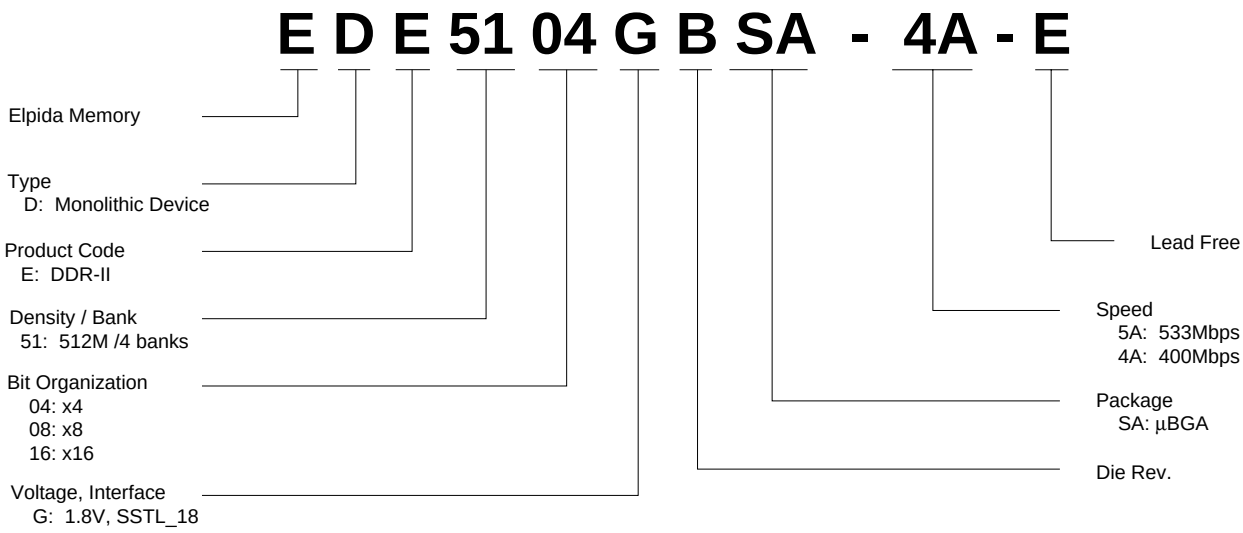
Ordering Information

Part number	Mask version	Organization (words × bits)	Internal Banks	Data rate (Mbps)	/CAS latency	Package
EDE5104GBSA-5A-E	B	128M × 4	4	533	4, 5	64-ball µBGA
EDE5104GBSA-4A-E				400	3, 4, 5	
EDE5108GBSA-5A-E		64M × 8		533	4, 5	
EDE5108GBSA-4A-E				400	3, 4, 5	
EDE5116GBSA-5A-E		32M × 16		533	4, 5	84-ball µBGA
EDE5116GBSA-4A-E				400	3, 4, 5	

Part Number



Pin Configurations

/xxx indicates active low signal.

64-ball μBGA
(×8, ×4 organization)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NU/ (NC)* /RDQS	VSS	VSSQ	/DQS	VDDQ
F	DQ6 (NC)*	VSSQ	DM/RDQS (DM)*	DQS	VSSQ	DQ7 (NC)*
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4 (NC)*	VSSQ	DQ3	DQ2	VSSQ	DQ5 (NC)*
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	/WE	/RAS	/CK	ODT
L	NC	BA0	BA1	/CAS	/CS	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	NC	NC	A13	

(Top view)

84-ball μBGA
(×16 organization)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	/UDQS	VDDQ
B	DQ14	VSSQ	UDM	UDQS	VSSQ	DQ15
C	VDDQ	DQ9	VDDQ	VDDQ	DQ8	VDDQ
D	DQ12	VSSQ	DQ11	DQ10	VSSQ	DQ13
E	VDD	NC	VSS	VSSQ	/LDQS	VDDQ
F	DQ6	VSSQ	LDM	LDQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	/WE	/RAS	/CK	ODT
L	NC	BA0	BA1	/CAS	/CS	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	NC	NC	NC	

(Top view)

Note: ( )* marked pins are for ×4 organization.

Pin name	Function	Pin name	Function
A0 to A13	Address inputs	ODT	ODT control
BA0, BA1	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ15	Data input/output	VSS	Ground for internal circuit
DQS, /DQS UDQS, /UDQS LDQS, /LDQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
RDQS, /RDQS	Differential data strobe for read	VSSQ	Ground for DQ circuit
/CS	Chip select	VREF	Reference supply voltage
/RAS, /CAS, /WE	Command input	VDDL	Supply voltage for DLL circuit
CKE	Clock enable	VSSDL	Ground for DLL circuit
CK, /CK	Differential Clock input	NC*1	No connection
DM, UDM, LDM	Write Data mask	NU*2	Not usable

Notes: 1. Not internally connected with die.
2. Don't use other than reserved functions.

CONTENTS

Electrical Specifications

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Power supply voltage	VDD	–0.5 to +2.3	V	1
Power supply voltage for output	VDDQ	–0.5 to +2.3	V	1
Input voltage	VIN	–0.5 to +2.3	V	1
Output voltage	VOUT	–0.5 to +2.3	V	1
Operating temperature (ambient)	TA	0 to +70	°C	1
Storage temperature	TSTG	–55 to +150	°C	1
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

Note: 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (SSTL_18)

- There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must be less than or equal to VDD.

Parameter	Symbol	min.	Typ.	max.	Unit	Notes
Supply voltage	VDD	1.7	1.8	1.9	V	4
Supply voltage for output	VDDQ	1.7	1.8	1.9	V	4
Input reference voltage	VREF	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	1, 2
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	3
DC input logic high	VIH (dc)	VREF + 0.125	—	VDDQ + 0.3V	V	
DC input low	VIL (dc)	–0.3	—	VREF – 0.125	V	
AC input logic high	VIH (ac)	VREF + 0.250	—	—	V	
AC input low	VIL (ac)	—	—	VREF – 0.250	V	

Notes: 1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 × VDDQ of the transmitting device and VREF are expected to track variations in VDDQ.

2. Peak to peak AC noise on VREF may not exceed ±2% VREF (dc).
3. VTT of transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together.

DC Characteristics 1 (TA = 0 to +70ºC, VDD, VDDQ = 1.8V ± 0.1V)

Parameter	Symbol	Grade	max.		Unit	Test condition
			× 4, × 8	× 16		
Operating current (ACT-PRE)	IDD0		TBD	TBD	mA	one bank; tRC = tRC (min.) ; tCK = tCK (min.) ; DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle
Operating current (ACT-READ-PRE)	IDD1		TBD	TBD	mA	one bank; Burst = 4; tRC = tRC (min.) ; CL = 4; tCK = tCK (min.) ; IOUT = 0mA; address and control inputs changing once per clock cycle
Precharge power-down standby current	IDD2P		TBD	TBD	mA	all banks idle; power-down mode; CKE = VIL (max.); tCK = tCK (min.)
Idle standby current	IDD2N		TBD	TBD	mA	/CS = VIH (min.); all banks idle; CKE = VIH (min.); tCK = tCK (min.) ; address and control inputs changing once per clock cycle
Active power-down standby current	IDD3P		TBD	TBD	mA	one bank active; power-down mode; CKE = VIL (max.); tCK = tCK (min.)
Active standby current	IDD3N		TBD	TBD	mA	one bank; active;/CS = VIH (min.); CKE = VIH (min.); tRC = tRAS max; tCK = tCK (min.); DQ, DM, and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle
Operating current (Burst read operating)	IDD4R		TBD	TBD	mA	one bank; Burst = 4; burst; address and control inputs changing once per clock cycle; DQ and DQS outputs changing twice per clock cycle; CL = 4; tCK = tCK (min.) ; IOUT = 0mA
Operating current (Burst write operating)	IDD4W		TBD	TBD	mA	one bank; Burst = 4; writes; continuous burst; address and control inputs changing once per clock cycle; DQ and DQS inputs changing twice per clock cycle; CL = 4; tCK = tCK (min.)
Auto-refresh current	IDD5		TBD	TBD	mA	tRC = tRFC (min.)
Self-refresh current	IDD6		TBD	TBD	mA	Self Refresh Mode; CKE = 0.2V
Operating current (Bank interleaving)	IDD7		TBD	TBD	mA	Four bank interleaving READs (BL4) with auto precharge, tRC = tRC (min.); Address and control inputs change during Active, READ, or WRITE commands.

DC Characteristics 2 (TA = 0 to +70ºC, VDD, VDDQ = 1.8V ± 0.1V)

Parameter	Symbol		Unit	Notes
Minimum required output pull-up under AC test load	VOH	VTT + 0.603	V	5
Maximum required output pull-down under AC test load	VOL	VTT – 0.603	V	5
Output timing measurement reference level	VOTR	0.5 × VDDQ	V	1
Output minimum sink DC current	IOL	+13.4	mA	3, 4, 5
Output minimum source DC current	IOH	–13.4	mA	2, 4, 5

Note: 1. The VDDQ of the device under test is referenced.
2. VDDQ = 1.7V; VOUT = 1.42V.
3. VDDQ = 1.7V; VOUT = 0.28V.
4. The DC value of VREF applied to the receiving device is expected to be set to VTT.
5. After OCD calibration to 18Ω at TA = 25°C, VDD = VDDQ = 1.8V.

Pin Capacitance (TA = 25°C, VDD, VDDQ = 1.8V ± 0.1V)

Parameter	Symbol	Pins	min.	Typ	max.	Unit	Notes
CLK input pin capacitance	CCK	CK	1.5	2.0	2.5	pF	1
Input pin capacitance	CIN	/RAS, /CAS, /WE, /CS, CKE. ODT, Address	1.5	2.0	2.5	pF	1
Input/output pin capacitance	CI/O	DQ, DQS, /DQS, UDQS, /UDQS, LDQS, /LDQS, /RDQS, /RDQS, DM, UDM, LDM	3.0	3.5	4.0	pF	2

Notes: 1. Matching within 0.25pF.
2. Matching within 0.50pF.

AC Characteristics (TA = 0 to +70°C, VDD, VDDQ = 1.8V ± 0.1V, VSS, VSSQ = 0V)

		-5A		-4A			
Frequency (Mbps)		533		400			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
DQ output access time from CK, /CK	tAC	–500	+500	–600	+600	ps	
DQS output access time from CK, /CK	tDQSCK	–450	+450	–500	+500	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min. (tCL, tCH)	—	min. (tCL, tCH)	—	ps	
Clock cycle time	tCK	3750	8000	5000	8000	ps	
DQ and DM input hold time	tDH	350	—	400	—	ps	
DQ and DM input setup time	tDS	350	—	400	—	ps	
Control and Address input pulse width for each input	tIPW	0.6	—	0.6	—	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	—	0.35	—	tCK	
Data-out high-impedance time from CK,/CK	tHZ	—	tAC max.	—	tAC max.	ps	
Data-out low-impedance time from CK,/CK	tLZ	tAC min.	tAC max.	tAC min.	tAC max.	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	—	300	—	350	ps	
DQ hold skew factor	tQHS	—	400	—	450	ps	
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	tHP – tQHS	—	ps	
Write command to first DQS latching transition	tDQSS	WL – 0.25	WL + 0.25	WL – 0.25	WL + 0.25	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	0.2	—	tCK	
Mode register set command cycle time	tMRD	2	—	2	—	tCK	
Write preamble setup time	tWPRES	0	—	0	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	
Write preamble	tWPRE	0.25	—	0.25	—	tCK	

		-5A		-4A			
Frequency (Mbps)		533		400			
Parameter	Symbol	min.	max.	min.	max.	Unit	Notes
Address and control input hold time	tIH	500	—	600	—	ps	
ddress and A control input setup time	tIS	500	—	600	—	ps	
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	
Active to precharge command	tRAS	45	—	45	—	ns	
Active to active/auto refresh command time	tRC	60	—	65	—	ns	
Active to read or write command delay	tRCD	15	—	20	—	ns	
Precharge command period	tRP	15	—	20	—	ns	
Active to auto-precharge delay	tRAP	tRCD min.	—	tRCD min.	—	ns	
Active bank A to active bank B command period (EDE5104GB, EDE5108GB)	tRRD	7.5	—	10	—	ns	
(EDE5116GB)	tRRD	10	—	10	—	ns	
Write recovery time	tWR	15	—	15	—	ns	
Auto precharge write recovery + precharge time	tDAL	(tWR/tCK)+ (tRP/tCK)	—	(tWR/tCK)+ (tRP/tCK)	—	tCK	1
Internal write to read command delay	tWTR	7.5	—	10	—	ns	
Exit self refresh to any command	tXSC	200	—	200	—	tCK	
Exit power down to any non-read command	tXPNR	2	—	2	—	tCK	
Exit precharge power down to read command	tXPRD	6 – AL	—	6 – AL	—	tCK	2
Exit active power down to read command	tXARD	2	—	2	—	tCK	3
Exit active power down to read command (slow exit/low power mode)	tXARDS	6 – AL	—	6 – AL	—	tCK	3
Output impedance test driver delay	tOIT	0	12	0	12	ns	
Auto refresh to active/auto refresh command time	tRFC	105	—	105	—	ns	
Average periodic refresh interval	tREFI	—	7.8	—	7.8	µs	

Notes: 1. For each of the terms above, if not already an integer, round to the next highest integer.
2. AL: Additive Latency.
3. MRS A12 bit define which active power down exit timing to be applied.

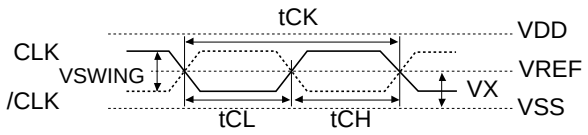
AC Electrical Characteristics and Operating Conditions

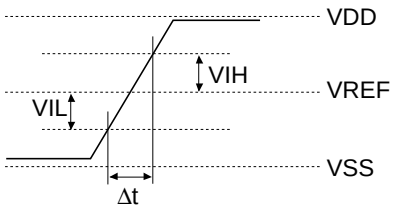
Parameter	Symbol	min	max	Unit	Notes
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on	tAON	tAC(min)	tAC(max) + 1000	ps	1
ODT turn-on (power - down mode)	tAONPD	tAC(min) + 2000	2tCK + tAC(max) + 1000	ps	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC(min)	tAC(max) + 600	ps	2
ODT turn-off (power - down mode)	tAOFPD	tAC(min) + 2000	2.5tCK + tAC(max) + 1000	ns	

Notes: 1. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

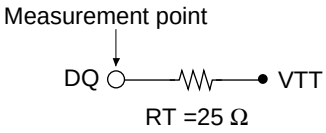
2. ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

Test Conditions

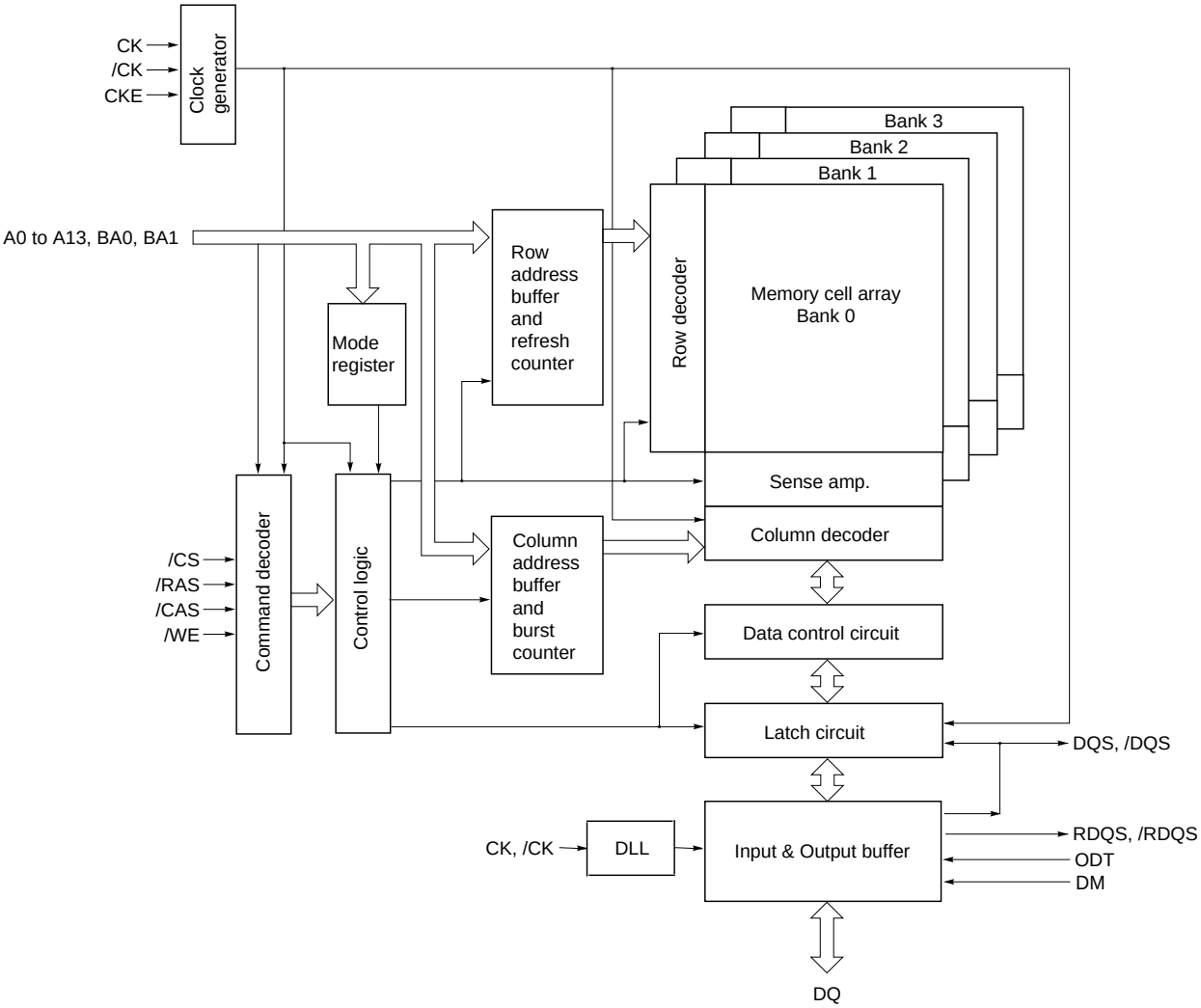




SLEW = (VIH (ac) – VIL (ac))/Δt



Block Diagram



Pin Function

CK, /CK (input pins)

CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).

/CS (input pin)

All commands are masked when /CS is registered High. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.

/RAS, /CAS, /WE (input pins)

/RAS, /CAS and /WE (along with /CS) define the command being entered.

A0 to A13 (input pins)

Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank.

[Address Pins Table]

	Address (A0 to A13)		
Part number	Row address	Column address	Notes
EDE5104GB	AX0 to AX13	AY0 to AY9, AY11	
EDE5108GB	AX0 to AX13	AY0 to AY9	
EDE5116GB	AX0 to AX12	AY0 to AY9	1

Notes: 1. A13 pin is NC for ×16 organization.

A10 (AP) (input pin)

A10 is sampled during a precharge command to determine whether the precharge applies to one bank (A10 = Low) or all banks (A10 = High). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during mode register set commands.

BA0, BA1 (input pins)

BA0 and BA1 define to which bank an active, read, write or precharge command is being applied. BA0 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE High activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides precharge power-down and Self Refresh operation (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, /CK and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.

DM, UDM and LDM (input pins)

DM is an input mask signal for write data. In 32M × 16 products, UDM and LDM control upper byte (DQ8 to DQ15) and lower byte (DQ0 to DQ7). Input data is masked when DM is sampled High coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For ×8 configuration, DM function will be disabled when RDQS function is enabled by EMRS.

DQ (input/output pins)

Bi-directional data bus.

DQS, /DQS, UDQS, /UDQS, LDQS, /LDQS (input/output pins)

Output with read data, input with write data for source synchronous operation. In 32M × 16 products, UDQS, /UDQS and LDQS, /LDQS control upper byte (DQ8 to DQ15) and lower byte (DQ0 to DQ7). Edge-aligned with read data, centered in write data. Used to capture write data. /DQS can be disabled by EMRS.

RDQS, /RDQS (output pins)

Differential Data Strobe for READ operation only. DM and RDQS functions are switch able by EMRS. These pins exist only in ×8 configuration. /RDQS output will be disabled when /DQS is disabled by EMRS**.**

ODT (input pins)

ODT (On Die Termination control) is a registered High signal that enables termination resistance internal to the DDR II SDRAM. When enabled, ODT is only applied to each DQ, DQS, /DQS, RDQS, /RDQS, and DM signal for × 4, × 8 configurations. For × 16 configuration, ODT is applied to each DQ, UDQS, /UDQS, LDQS, /LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.

VDD, VSS, VDDQ, VSSQ (power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

VDDL and VSSDL (power supply)

VDDL and VSSDL are power supply pins for DLL circuits.

VREF (Power supply)

SSTL_18 reference voltage: (0.50 ± 0.01) × VDDQ

Command Operation

Command Truth Table

The DDR-II SDRAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Function	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA1, BA0	A13 to A11	A10	A0 to A9	Notes
		Previous cycle	Current cycle									
Mode register set	MRS	H	H	L	L	L	L	BA0 = 0 and MRS OP Code				1
Extended mode register set	EMRS	H	H	L	L	L	L	BA0 = 1 and EMRS OP Code				1
Auto (CBR) refresh	REF	H	H	L	L	L	H	×	×	×	×	1
Self refresh entry	SELF	H	L	L	L	L	H	×	×	×	×	1
Self refresh exit	SELFX	L	H	H	×	×	×	×	×	×	×	1
Single bank precharge	PRE	H	H	L	L	H	L	BA	×	L	×	1, 2
Precharge all banks	PALL	H	H	L	L	H	L	×	×	H	×	1
Bank activate	ACT	H	H	L	L	H	H	BA	Row Address			1, 2
Write	WRIT	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with auto precharge	WRITA	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	READ	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with auto precharge	READA	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No operation	NOP	H	×	L	H	H	H	×	×	×	×	1
Device deselect	DESL	H	×	H	×	×	×	×	×	×	×	1
Power down mode entry	PDEN	H	L	×	×	×	×	×	×	×	×	1, 4, 5
Power down mode exit	PDEX	L	H	×	×	×	×	×	×	×	×	1, 4, 5

Remark: H = VIH. L = VIL. × = VIH or VIL

Notes: 1. All DDR-II commands are defined by states of /CS, /RAS, /CAS, /WE, and CKE at the rising edge of the clock.

2. Bank Select (BA0, BA1), determine which bank is to be operated upon.

3. Burst reads or writes should not be terminated other than specified as ″Reads interrupted by a Read″ in Burst Read command [READ] or ″Writes interrupted by a Write″ in Burst Write command [WRIT].

4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements of the device. One clock delay is required for mode entry and exit.

5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

CKE Truth Table

Current state	Function	CKE		Command					Notes
		Previous Cycle	Current Cycle	/CS	/RAS	/CAS	/WE	BA1,BA0, A13 to A0	
Self refresh	INVALID	H	×	×	×	×	×	×	1
	Exit self refresh with device deselect	L	H	H	×	×	×	×	2
	Exit self refresh with no operation	L	H	L	H	H	H	×	2
	Illegal	L	H	L	Command			Address	2
	Maintain self refresh	L	L	×	×	×	×	×	
Power down	INVALID	H	×	×	×	×	×	×	1
	Power down mode exit	L	H	H	×	×	×	×	2
	ILLEGAL	L	H	L	Command except NOP			Address	2
	Maintain power down mode	L	L	×	×	×	×	×	
All banks idle	Device deselect	H	H	H	×	×	×		3
	Refer to the current state truth table	H	H	L	Command			Address	3
	Power down	H	L	H	×	×	×		
	Register command begin power down next cycle	H	L	L	Command			Address	3
	Entry self refresh	H	L	L	L	L	H	×	4
Any state other than listed above	Refer to operations in the current state truth table	H	H	×	×	×	×	×	
	Power down entry	H	L	×	×	×	×	×	5
	ILLEGAL	L	×	×	×	×	×	×	

Remark: H = VIH. L = VIL. × = VIH or VIL

Notes: 1. For the given Current State CKE must be low in the previous cycle.

2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE (tCES) must be satisfied before any command other than self refresh exit.
3. The inputs (BA1, BA0, A13 to A0) depend on the command that is issued. See the Command Truth Table for more information.
4. The Auto Refresh, Self Refresh mode, and the Mode Register Set modes can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Command Truth Table.

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR SDRAM.

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Notes
Idle	H	×	×	×	×	DESL	Nop or Power down	
	L	H	H	H	×	NOP	Nop or Power down	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10 (AP)	PRE	Precharge	
	L	L	H	L	A10 (AP)	PALL	Precharge all banks	
	L	L	L	H	×	REF	Auto refresh	2
	L	L	L	H	×	SELF	Self refresh	2
	L	L	L	L	BA, MRS-OPCODE	MRS	Mode register accessing	2
	L	L	L	L	BA, EMRS-OPCODE	EMRS	Extended mode register accessing	2
Bank(s) active	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	L	H	BA, CA, A10 (AP)	READ	Begin Read	
	L	H	L	H	BA, CA, A10 (AP)	READA	Begin Read	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	Begin Write	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	Begin Write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	Precharge	
	L	L	H	L	A10 (AP)	PALL	Precharge all banks	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end -> Row active	
	L	H	H	H	×	NOP	Continue burst to end -> Row active	
	L	H	L	H	BA, CA, A10 (AP)	READ	Burst interrupt	1, 4
	L	H	L	H	BA, CA, A10 (AP)	READA	Burst interrupt	1, 4
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Write	H	×	×	×	×	DESL	Continue burst to end -> Write recovering	
	L	H	H	H	×	NOP	Continue burst to end -> Write recovering	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	Burst interrupt	1, 4
	L	H	L	L	BA, CA, A10 (AP)	WRITA	Burst interrupt	1, 4
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Read with	H	×	×	×	×	DESL	Continue burst to end -> Precharging	
auto precharge	L	H	H	H	×	NOP	Continue burst to end -> Precharging	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Write with auto Precharge	H	×	×	×	×	DESL	Continue burst to end ->Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end ->Write recovering with auto precharge	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Precharging	H	×	×	×	×	DESL	Nop -> Enter idle after tRP	
	L	H	H	H	×	NOP	Nop -> Enter idle after tRP	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	Nop -> Enter idle after tRP	
	L	L	H	L	A10 (AP)	PALL	Nop -> Enter idle after tRP	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop -> Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop -> Enter bank active after tRCD	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop -> Enter bank active after tWR	
	L	H	H	H	×	NOP	Nop -> Enter bank active after tWR	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	New write	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

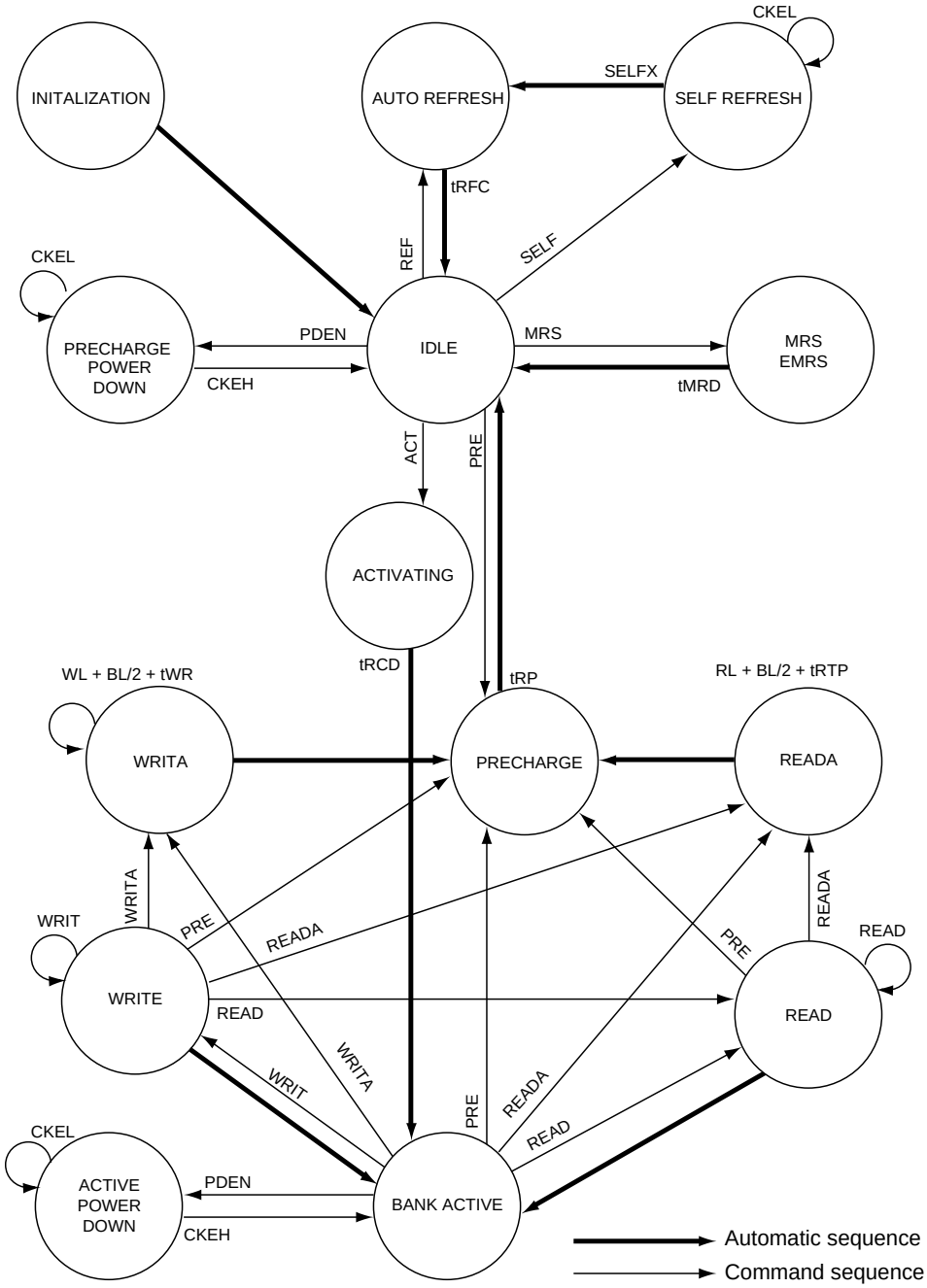
Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Write recovering with	H	×	×	×	×	DESL	Nop -> Enter bank active after tWR	
auto precharge	L	H	H	H	×	NOP	Nop -> Enter bank active after tWR	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	1
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	1
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	1
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop -> Enter idle after tRFC	
	L	H	H	H	×	NOP	Nop -> Enter idle after tRFC	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	
Mode register accessing	H	×	×	×	×	DESL	Nop -> Enter idle after tMRD	
	L	H	H	H	×	NOP	Nop -> Enter idle after tMRD	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Note
Extended Mode	H	×	×	×	×	DESL	Nop -> Enter idle after tMRD	
register accessing	L	H	H	H	×	NOP	Nop -> Enter idle after tMRD	
	L	H	L	H	BA, CA, A10 (AP)	READ	ILLEGAL	
	L	H	L	H	BA, CA, A10 (AP)	READA	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRIT	ILLEGAL	
	L	H	L	L	BA, CA, A10 (AP)	WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10 (AP)	PRE	ILLEGAL	
	L	L	H	L	A10 (AP)	PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	H	×	SELF	ILLEGAL	
	L	L	L	L	BA, MRS-OPCODE	MRS	ILLEGAL	
	L	L	L	L	BA, EMRS-OPCODE	EMRS	ILLEGAL	

Remark: H = VIH. L = VIL. × = VIH or VIL

Notes: 1. This command may be issued for other banks, depending on the state of the banks.
2. All banks must be in "IDLE".
3. All AC timing specs must be met.
4. Only allowed at the boundary of 4 bits burst. Burst interruption at other timings are illegal.

Simplified State Diagram



Simplified State Diagram

Operation of DDR-II SDRAM

Read and write accesses to the DDR-II SDRAM are burst oriented; accesses start at a selected location and continue for the fixed burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the active command is used to select the bank and row to be accessed (BA0, BA1 select the bank; A0 to A13 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the auto precharge command is to be issued. Prior to normal operation, the DDR-II SDRAM must be initialized. The following sections provide detailed information covering device initialization; register definition, command descriptions and device operation.

Power On and Initialization

DDR-II SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD, then to VDDQ, and finally to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied any time after VDDQ, but is expected to be nominally coincident with VTT. By attempting to maintain CKE Low, the DQ and DQS outputs are in the High-Z state during power-up. After all power supply, reference voltages, and the clocks are stable, the DDR-II SDRAM requires a 200µs delay prior to applying an executable command.

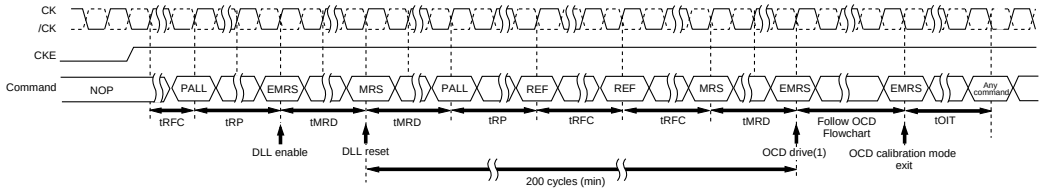
Once the 200µs delay has been satisfied, a Deselect or NOP command should be applied, and CKE must be brought high. Issuing the NOP command during tRFC period, a Precharge ALL command must be applied. Next a mode register set command must be issued for the extended mode register, to enable the DLL. Then a mode register set command must be issued for the mode register, to reset the DLL and to program the operating parameters. 200 clock cycles are required between the DLL reset and any read command. Precharge ALL command should be applied, placing the device in the “all banks idle” state.

Once in the idle state, two Auto Refresh cycles must be performed. Additionally, a mode register set command for the mode register, with the reset DLL bit deactivated (i.e. to program operating parameters without resetting the DLL) must be performed. Finally, OCD impedance adjustment should be performed. At least, ERMS OCD Default command must be issued. Following these cycles, the DDR-II SDRAM is ready for normal operation. Failure to follow these steps may lead to unpredictable start-up modes.

Power-Up and Initialization Sequence

The following sequence is required for Power-up and Initialization.

1. Apply power and attempt to maintain CKE and ODT at a low state (all other inputs may be undefined.)
   - Apply VDD before or at the same time as VDDQ.
   - Apply VDDQ before or at the same time as VTT and VREF.
2. Start clock and maintain stable condition for a minimum of 200µs.
3. The minimum of 200µs after stable power and clock(CK, /CK), apply NOP and take CKE High.
4. Wait tRFC then issue precharge commands for all banks of the device.
5. Issue EMRS to enable DLL. (To issue "DLL Enable" command, provide Low to A0, High to BA0 and Low to all of the rest address pins, A1 to A11 and BA1)
6. Issue a mode register set command for DLL reset. The additional 200 cycles of clock input is required to lock the DLL. (To issue DLL reset command, provide High to A8 and Low to BA0)
7. Issue precharge commands for all banks of the device.
8. Issue 2 or more auto-refresh commands.
9. Issue a mode register set command with low to A8 to initialize device operation.
10. Carry out OCD impedance adjustment (Follow “OCD Flow Chart” in the chapter of Off-Chip Driver (OCD) Impedance Adjustment). At least, EMRS OCD Default Command (A9=A8=A7=1) must be issued. Whenever issue extended mode register set command for OCD, keep previous setting of A0 to A6, A0 to A13 and BA1



Power up and Initialization Sequence

Programming the Mode Register

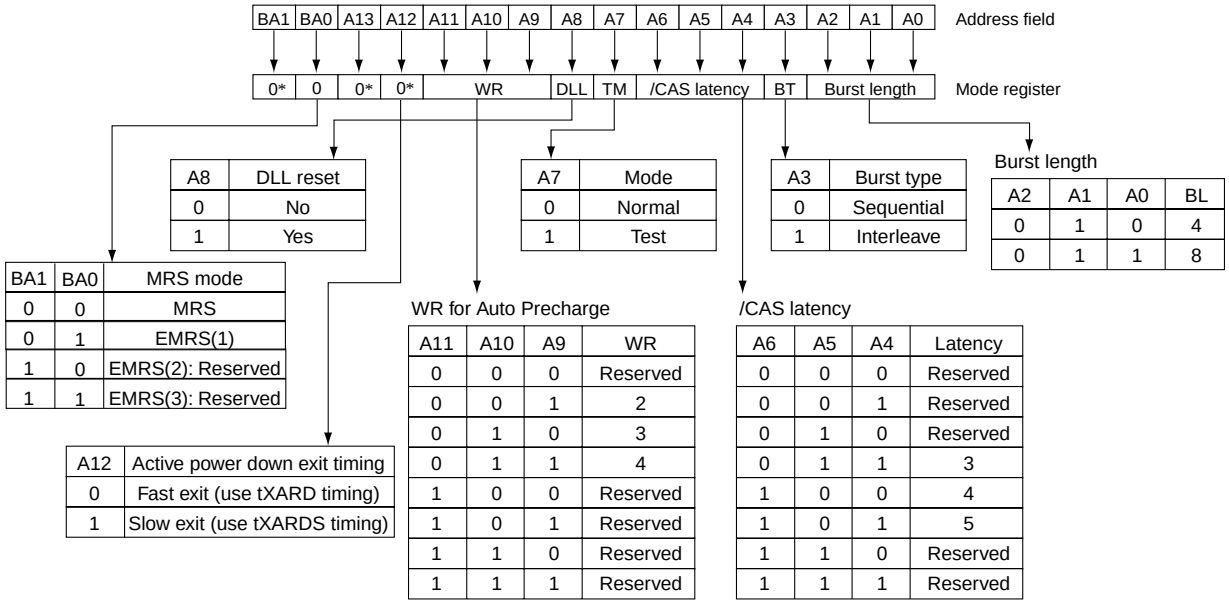
For application flexibility, burst type, /CAS latency, DLL reset function are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive /CAS latency, and variable data-output impedance adjustment are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Re-executing the MRS and EMRS Commands can alter contents of the MRS and EMRS. Even though the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued.

After initial power up, the both MRS and EMRS Commands must be issued before read or write cycles may begin. All four banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. Either MRS or EMRS Commands are activated by the low signals of /CS, /RAS, /CAS and /WE at the positive edge of the clock. When the bank address 0 (BA0) is low, the DDR-II SDRAM enables the MRS command. When the bank address 0 (BA0) is high, the DDR-II SDRAM enables the EMRS command. The address input data during this cycle defines the parameters to be set as shown in the MRS and EMRS table. A new command may be issued after the mode register set command cycle time (tMRD). MRS, EMRS and Reset DLL do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

DDR-II SDRAM Mode Register Set [MRS]

The mode register stores the data for controlling the various operating modes of DDR-II SDRAM. It controls /CAS latency, burst sequence, test mode, DLL reset and various vendor specific options to make DDR-II SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0, while controlling the state of address pins A0 to A13. The DDR-II SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst address sequence type is defined by A3, and, /CAS latency is defined by A4 to A6. The DDR-II doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. A9 to A11 are used for define Write Recovery time in clocks using for Auto Precharge. Users are required to set the appropriate values according to tWR spec and operating frequency of the systems.

A12 is used for Active Power Down exit timing selection. If Slow exit is set, DLL is turned off during Active Power Down, then Asynchronous ODT timings and tXARDS timing for exit should be used. Refer to the table for specific codes.



*BA1, A12 and A13 are reserved for future use and must be programmed to 0 when setting the mode register.

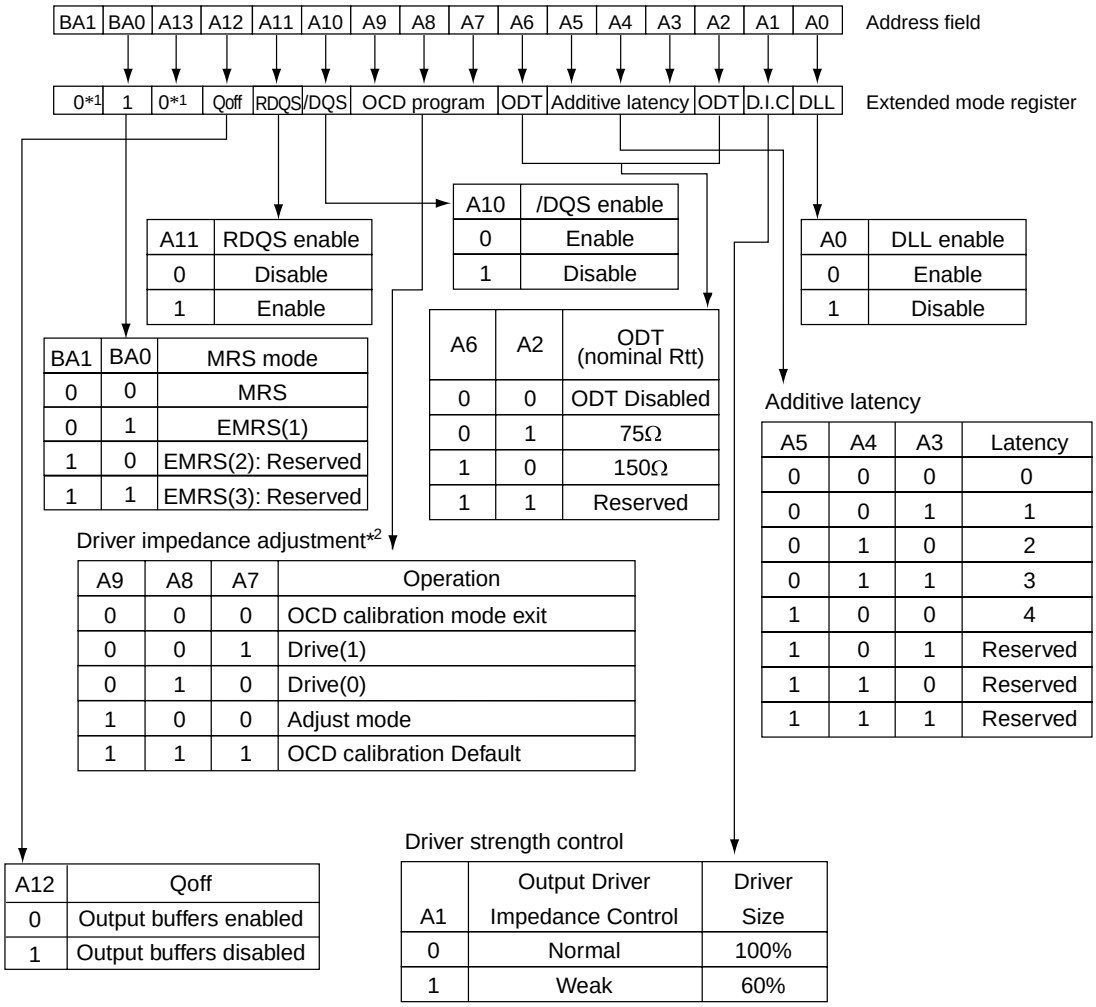
Mode Register Set (MRS)

DDR-II SDRAM Extended Mode Register Set [EMRS]

The extended mode register stores the data for enabling or disabling the DLL, output driver strength and additive latency. The default value of the extended mode register is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and High on BA0, while controlling the states of address pins A0 to A13. The DDR-II SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register. Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a half strength data-output driver. A3 to A5 determines the additive latency, A7 to A9 are used for OCD control, A10 is used for /DQS enable and A11 is used for RDQS enable. A12 is used for Qoff (output buffers disable).

DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering self refresh operation and is automatically re-enabled upon exit of self refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.



A11	RDQS enable
0	Disable
1	Enable

A10	/DQS enable
0	Enable
1	Disable

A0	DLL enable
0	Enable
1	Disable

BA1	BA0	MRS mode
0	0	MRS
0	1	EMRS(1)
1	0	EMRS(2): Reserved
1	1	EMRS(3): Reserved

A6	A2	ODT (nominal Rtt)
0	0	ODT Disabled
0	1	75Ω
1	0	150Ω
1	1	Reserved

Additive latency

A5	A4	A3	Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Driver impedance adjustment*2

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive(1)
0	1	0	Drive(0)
1	0	0	Adjust mode
1	1	1	OCD calibration Default

A12	Qoff
0	Output buffers enabled
1	Output buffers disabled

Driver strength control

A1	Output Driver Impedance Control	Driver Size
0	Normal	100%
1	Weak	60%

*1: BA1 and A13 are reserved for future use, and must be programmed to 0 when setting the extended mode register.
*2: Refer to the chapter "Off-chip Driver (OCD) impedance Adjustment" for detailed information

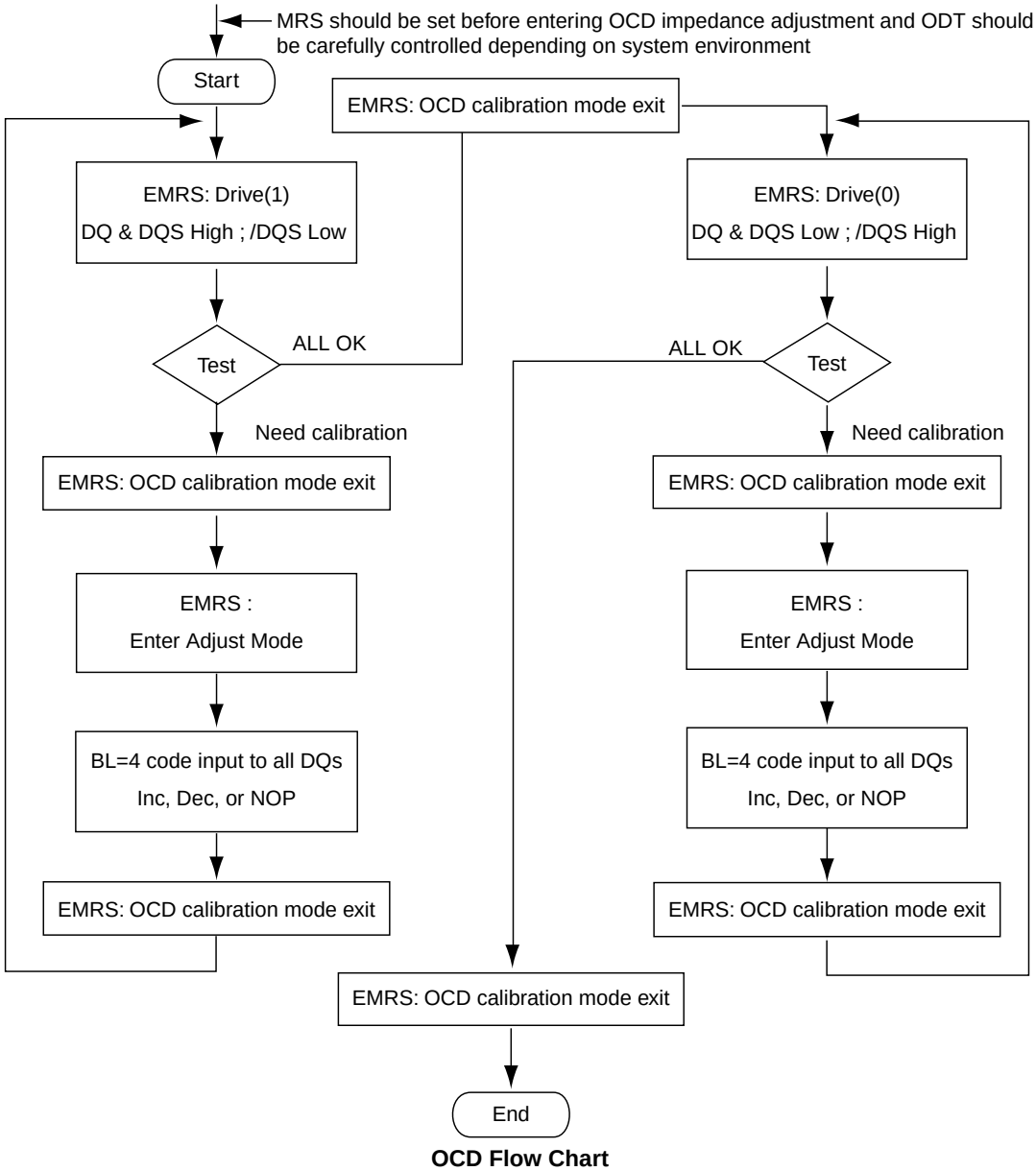
Extended Mode Register Set (EMRS)

[Pin Function Matrix for RDQS, /RDQS, /DQS]

RDQS enable (A11)	/DQS enable (A10)	DM/ RDQS	/RDQS	/DQS
0(disable)	0(enable)	DM	High - Z	/DQS
0(disable)	1(disable)	DM	High - Z	High - Z
1(enable)	0(enable)	RDQS	/RDQS	/DQS
1(enable)	1(disable)	RDQS	High - Z	High - Z

Off-Chip Driver (OCD) Impedance Adjustment

DDR-II SDRAM supports driver calibration feature and the “OCD Flow Chart ” is an example of sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



OCD Flow Chart

Extended Mode Register Set for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR-II SDRAM and drive of RDQS is dependent on EMRS bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all /DQS signals are driven low. In drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all /DQS signals are driven high.

In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics follow approximate nominal V/I curve for 18Ω output drivers, but are not guaranteed. If tighter control is required, which is controlled within 18Ω ± 3Ω driver impedance range, OCD must be used.

[OCD Mode Set Program]

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS, (RDQS) High and /DQS Low
0	1	0	Drive (0) DQ, DQS, (RDQS) Low and /DQS High
1	0	0	Adjust mode
1	1	1	OCD calibration default

OCD Impedance Adjustment

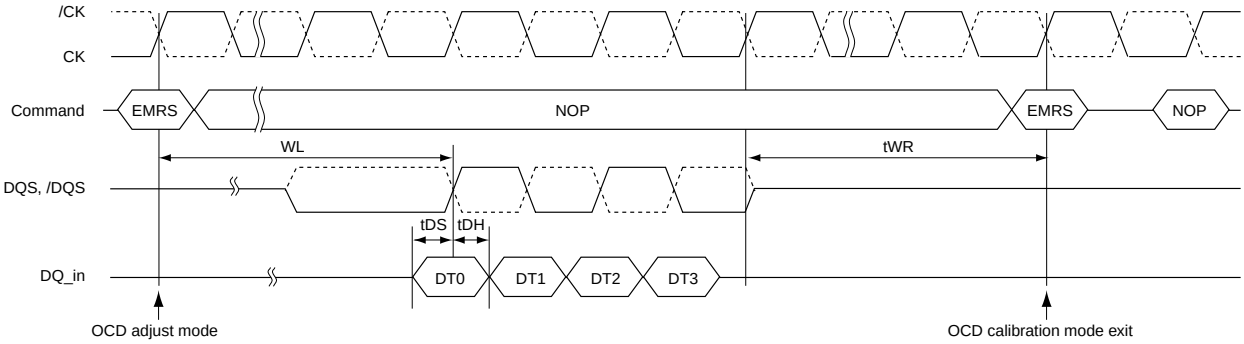
To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4bit burst code to DDR-II SDRAM as in table X. For this operation, burst length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive this burst code to all DQs at the same time. DT0 in table X means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR-II SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR-II SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range.

[OCD Adjustment Program]

4bits burst data inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP	NOP
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other combinations				Reserved	

For proper operation of adjust mode, WL = RL − 1 = AL + CL − 1 clocks and tDS/tDH should be met as the following timing diagram. For input data pattern for adjustment, DT0 to DT3 is a fixed order and not affected by MRS addressing mode (ie.sequentialorinterleave).

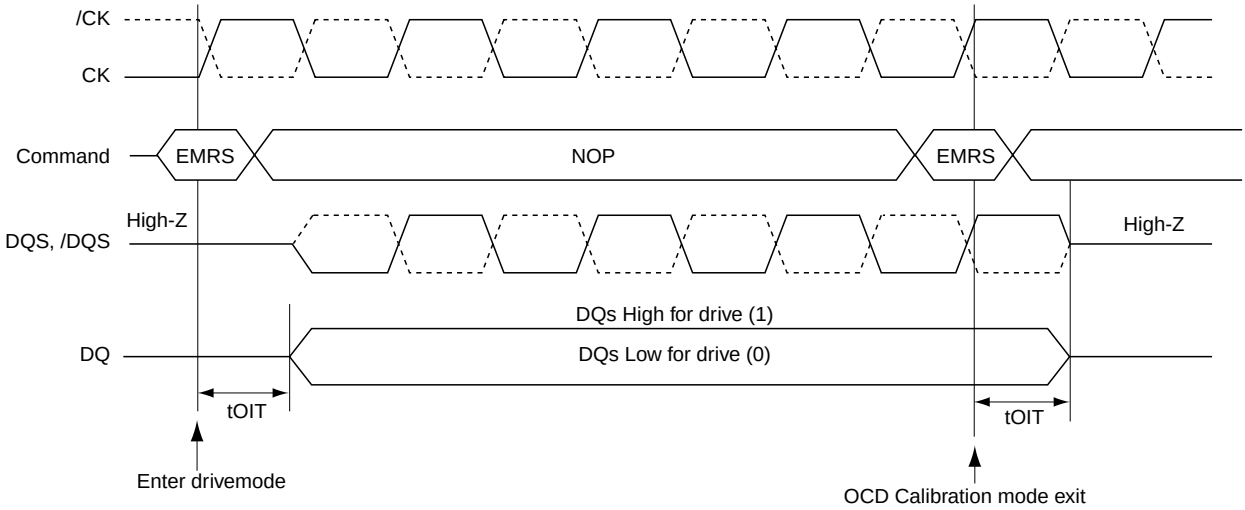
For proper operation of adjust mode, WL = RL – 1 = AL + CL – 1 clocks and tDS/tDH should be met as the “Output Impedance Control Register Set Cycle”. For input data pattern for adjustment, DT0 to DT3 is a fixed order and not affected by MRS addressing mode (i.e. sequential or interleave).



Output Impedance Control Register Set Cycle

Drive Mode

Drive mode, both drive (1) and drive (0), is used for controllers to measure DDR-II SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after “Enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the ”Output Impedance Measurement/Verify Cycle”.

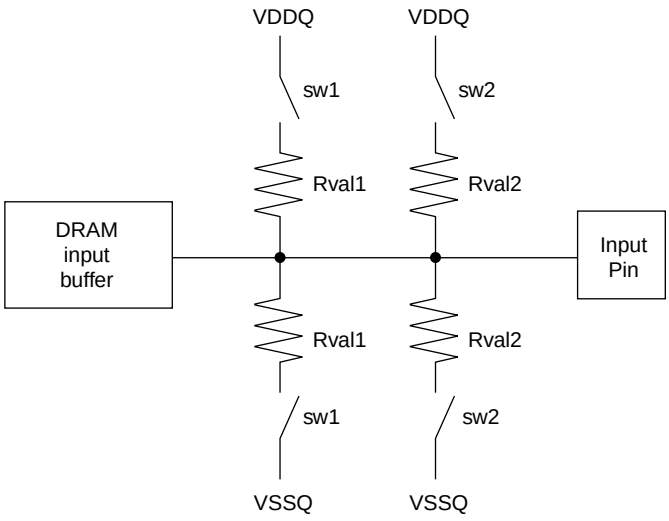


Output Impedance Measurement/Verify Cycle

ODT(On Die Termination)

On Die Termination (ODT), is a feature that allows a DRAM to turn on/off termination resistance for each DQ, DQS, /DQS, RDQS, /RDQS, and DM signal for × 4 × 8 configurations via the ODT control pin. For × 16 configuration ODT is applied to each DQ, UDQS, /UDQS, LDQS, /LDQS, UDM, and LDM signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function is turned off and not supported in self refresh mode.



Switch sw1 or sw2 is enabled by ODT pin.
Selection between sw1 or sw2 is determined by Rtt (nomial) in EMRS
Termination included on all DQs, DM, DQS, /DQS, RDQS and /RDQS pins.
Target Rtt (Ω) = (Rval1) / 2 or (Rval2) / 2

Functional Representation of ODT

DC Electrical Characteristics and Operating Conditions

Parameter	Symbol	min	Typ	max	Unit	Notes
Rtt effective impedance value for EMRS (A6, A2) = 0,1 ; 75 Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS (A6, A2) = 1,0 ; 150 Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt mismatch tolerance between any pull-up and pull-down pair	Rtt(mis)	–3.75	—	+3.75	%	1

Test Condition For Rtt Measurements [*1]

Measurement Definition for Rtt(eff)

Apply VIH (AC) and VIL (AC) to test pin separately, then measure current I(VIH(AC)) and I(VIL(AC)) respectively.

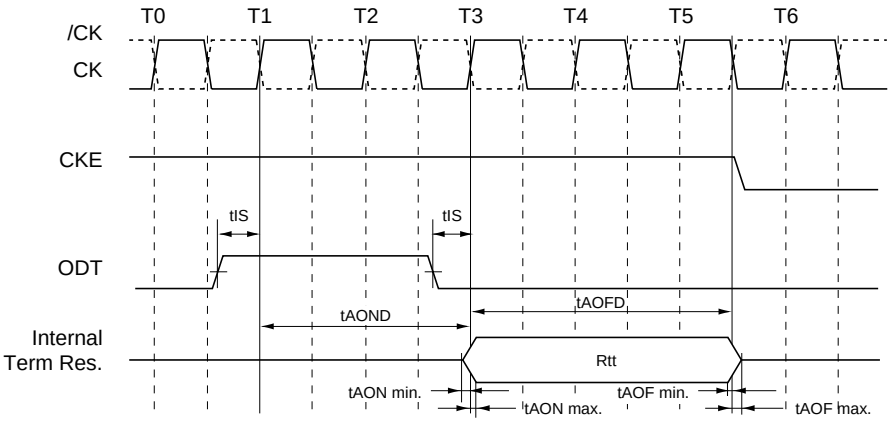
$$Rtt(eff) = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

Measurement Definition for Rtt(mis)

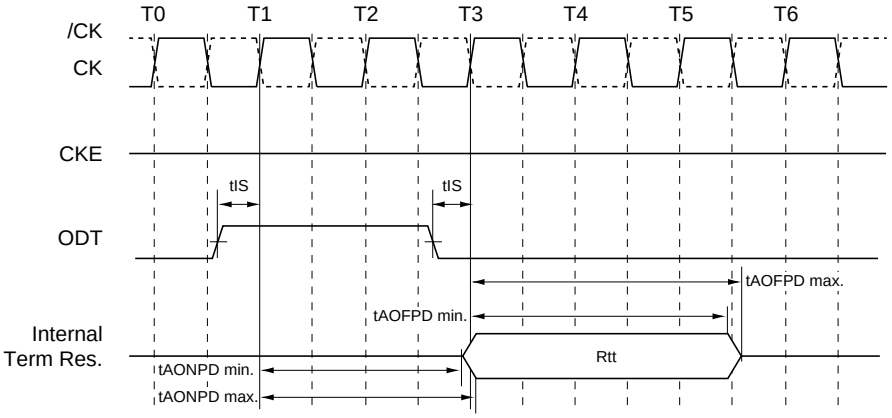
Measure voltage (Vm) at test pin (midpoint) with no load.

$$Rtt(mis) = \left(\frac{2 \times Vm}{VDDQ} - 1\right) \times 100\%$$

Notes: 1. VIH(AC), and VDDQ values defined in SSTL_18.



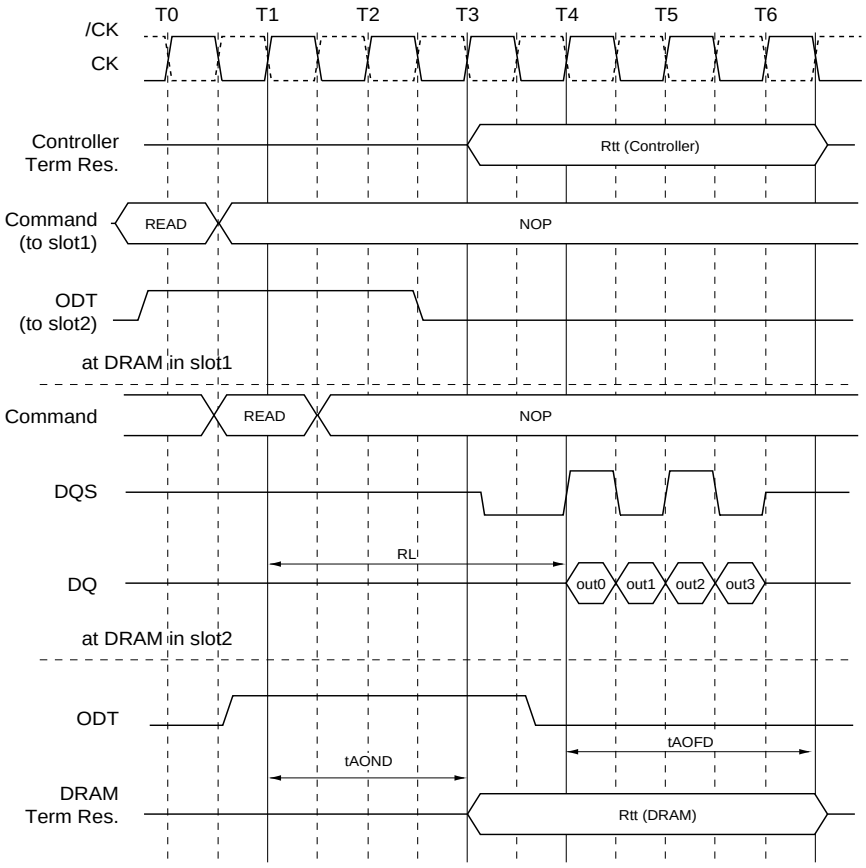
ODT Timing for Active and Standby Mode



ODT Timing for Power down Mode

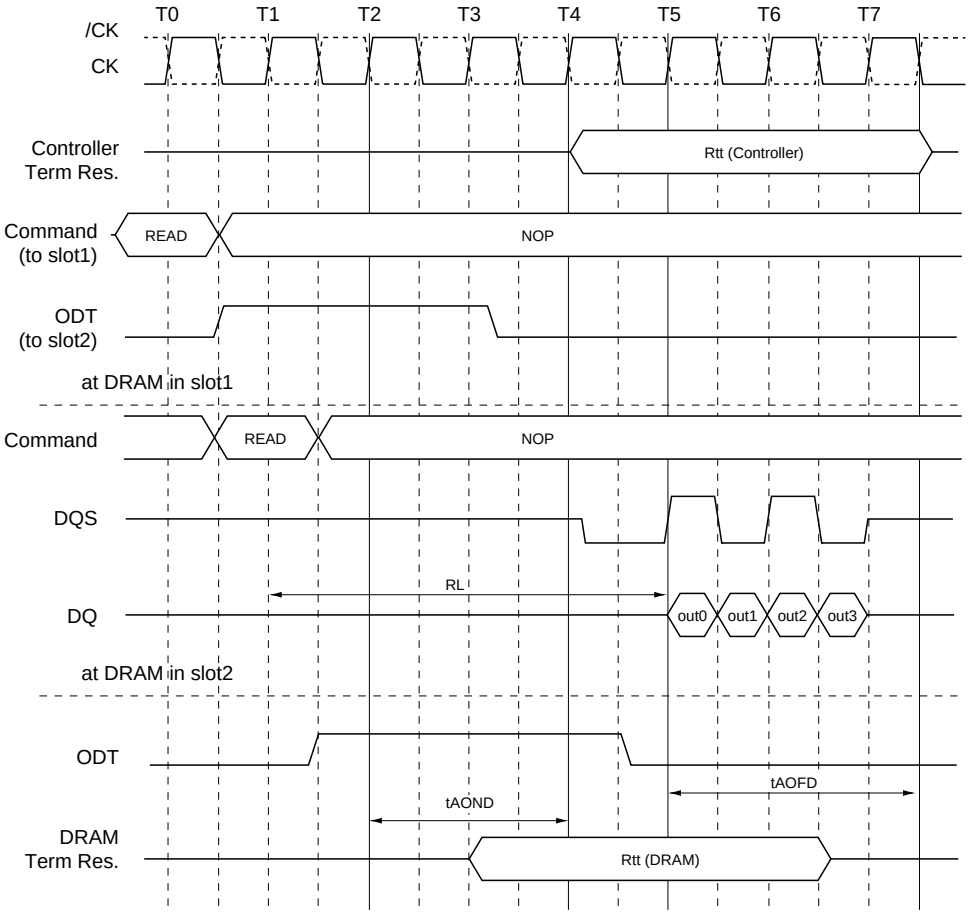
ODT Control of Reads

At a minimum, ODT must be latched High by CK at (Read Latency – 3tCK) after the READ command and remain High until (Read Latency + BL/2 – 2tCK) after the READ command (where Read Latency = AL + CL). The controller is also required to activate it´s own termination with a turn on time the same as the DRAM and keeping it on until valid data is no longer on the system bus.



Read Example for a 2 Slot Registered System with 2nd Slot in Active Mode

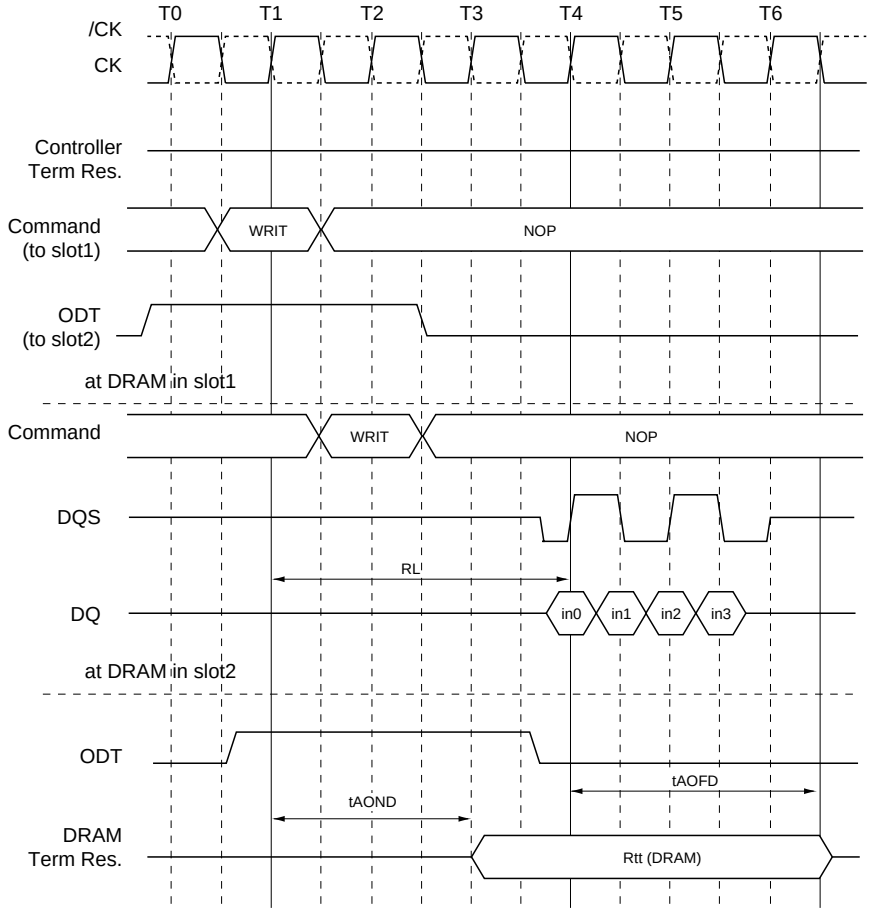
(Read Latency = 3tCK ; tAOND = 2tCK ; tAOFD = 2.5tCK)



Read Example for a 2 Slot Registered System with 2nd Slot in Active Mode

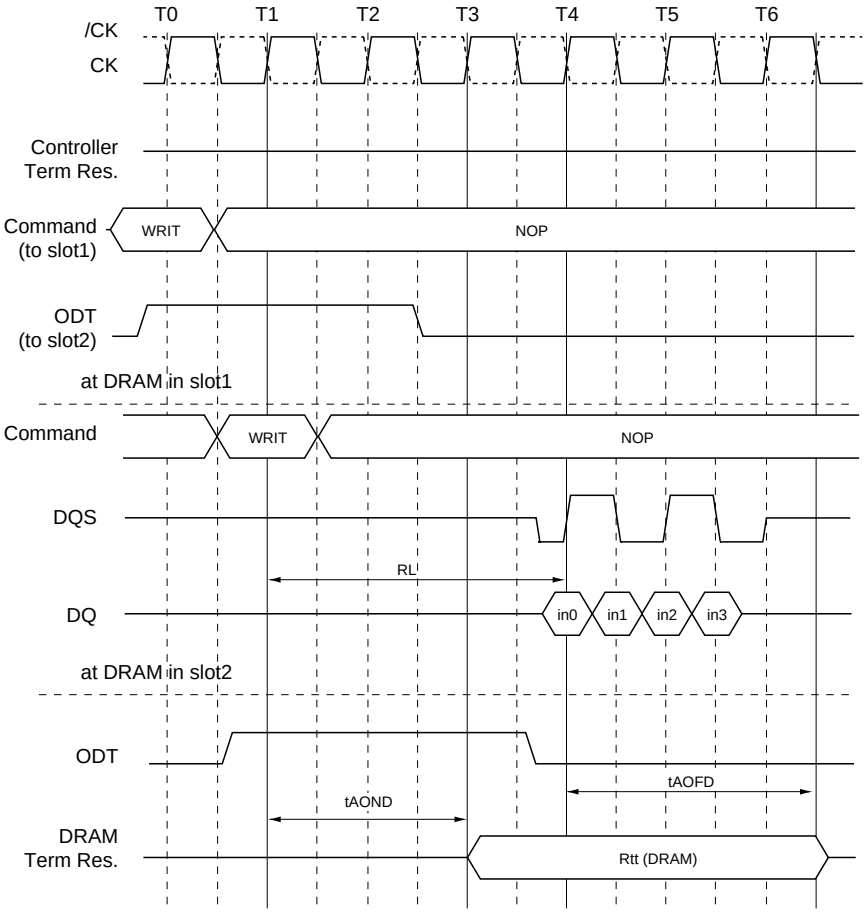
(Read Latency = 4tCK ; tAOND = 2tCK ; tAOFD = 2.5tCK)

At a minimum, ODT must be latched High by CK at (Write Latency – 3 tCK) after the WRIT command and remain high until (Write Latency + BL/2 – 2tCK) after the WRIT command(Where Write Latency = Read Latency – 1tCK). During writes, no ODT is required at the controller.



Write Example for a 2 Slot Registered System with 2nd Slot in Active Mode

(Read Latency = 3tCK ; tAOND = 2tCK ; tAOFD = 2.5tCK)

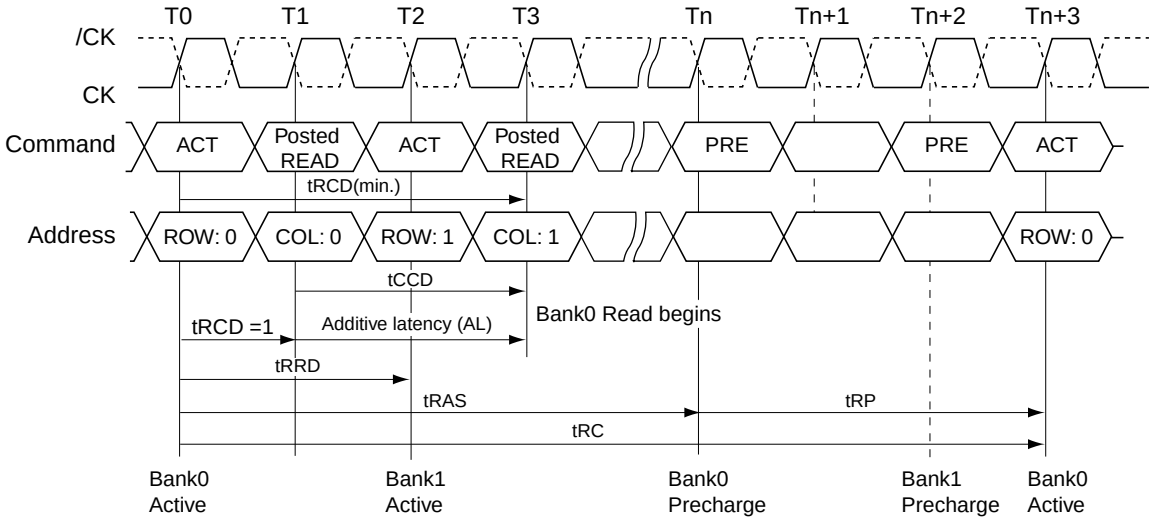


Write Example for a 2 Slot Registered System with 2nd Slot in Active Mode

(Read Latency = 4tCK ; tAOND = 2tCK ; tAOFD = 2.5tCK)

Bank Activate Command [ACT]

The bank activate command is issued by holding /CAS and /WE High with /CS and /RAS Low at the rising edge of the clock. The bank addresses BA0 and BA1, are used to select the desired bank. The row address A0 through A13 is used to determine which row to activate in the selected bank. The Bank activate command must be applied before any read or write operation can be executed. Immediately after the bank active command, the DDR-II SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCD (min.) specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure tRCD (min.) is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another bank activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive bank activate commands to the same bank is determined by the /RAS cycle time of the device (tRC), which is equal to tRAS + tRP. The minimum time interval between successive bank activate commands to the different bank is determined by (tRRD).



Bank Activate Command Cycle (tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2)

Read and Write Access Modes

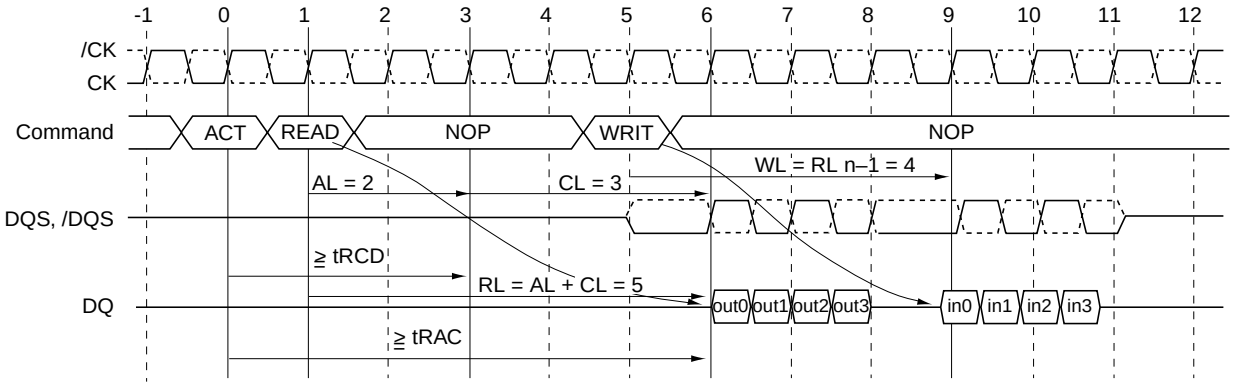
After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /RAS High, /CS and /CAS Low at the clock's rising edge. /WE must also be defined at this time to determine whether the access cycle is a read operation (/WE high) or a write operation (/WE low).

The DDR-II SDRAM provides a fast column access operation. A single read or write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length. For example, the 32M bits × 4 I/O × 4 Banks chip has a page length of 2048 bits (defined by CA0 to CA9, CA11). The page length of 2048 is divided into 512 uniquely addressable boundary segments (4 bits each). A 4 bits burst operation will occur entirely within one of the 512 groups beginning with the column address supplied to the device during the read or write Command (CA0 to CA9, CA11). The second, third and fourth access will also occur within this group segment, however, the burst order is a function of the starting address, and the burst sequence.

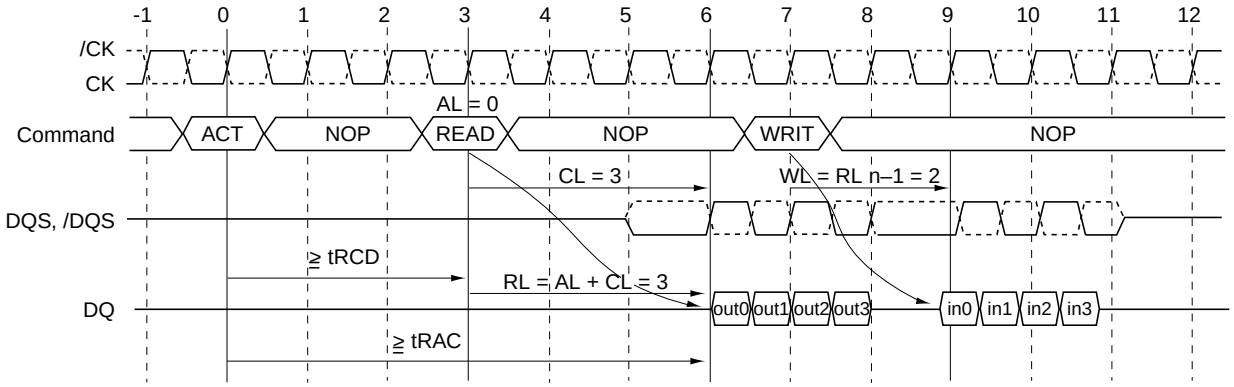
A new burst access must not interrupt the previous 4-bit burst operation. The minimum /CAS to /CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

Posted /CAS

Posted /CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR-II SDRAM. In this operation, the DDR-II SDRAM allows a /CAS read or write command to be issued immediately after the /RAS bank activate command (or any time during the /RAS-/CAS-delay time, tRCD, period). The command is held for the time of the additive latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the /CAS latency (CL). Therefore if a user chooses to issue a R/W command before the tRCD (min), then AL (greater than 0) must be written into the EMRS. The Write Latency (WL) is always defined as RL – 1 (read latency –1) where read latency is defined as the sum of additive latency plus /CAS latency (RL=AL+CL).



Read followed by a write to the same bank
[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4]



Read followed by a write to the same bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2]

Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. DDR-II SDRAM supports 4 bits burst and 8bits burst modes only. For 8 bits burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS, which is similar to the DDR-I SDRAM operation. Seamless burst read or write operations are supported.

Unlike DDR-I devices, interruption of a burst read or writes operation is limited to ready by Read or Write by Write at the boundary of Burst 4. Therefore the burst stop command is not supported on DDR-II SDRAM devices.

[Burst Length and Sequence]

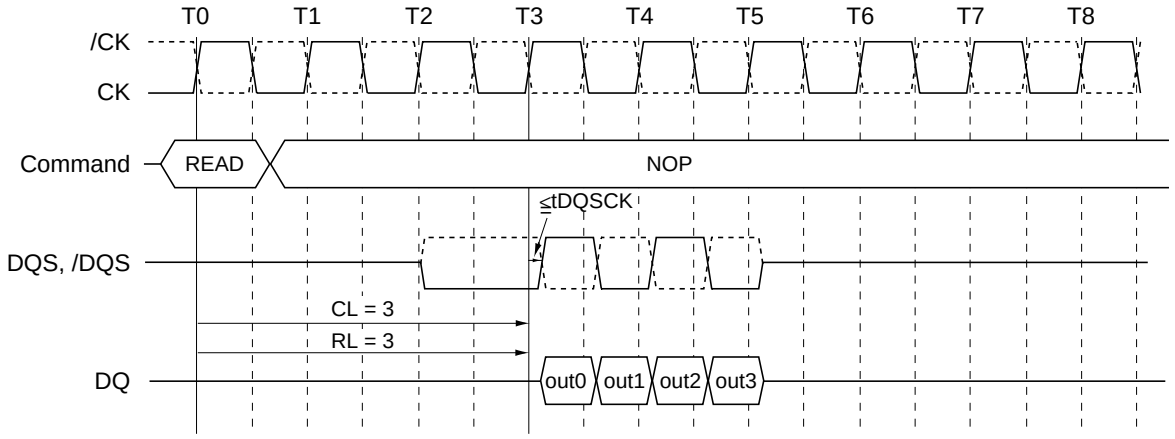
Burst length	Starting address (A2, A1, A0)	Sequential addressing (decimal)	Interleave addressing (decimal)
4	000	0, 1, 2, 3	0, 1, 2, 3
	001	1, 2, 3, 0	1, 0, 3, 2
	010	2, 3, 0, 1	2, 3, 0, 1
	011	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Note: Page length is a function of I/O organization and column addressing
32M bits × 4 organization (CA0 to CA9, CA11); Page Length = 2048 bits
16M bits × 8 organization (CA0 to CA9); Page Length = 1024 bits
8M bits × 16 organization (CA0 to CA9); Page Length = 1024 bits

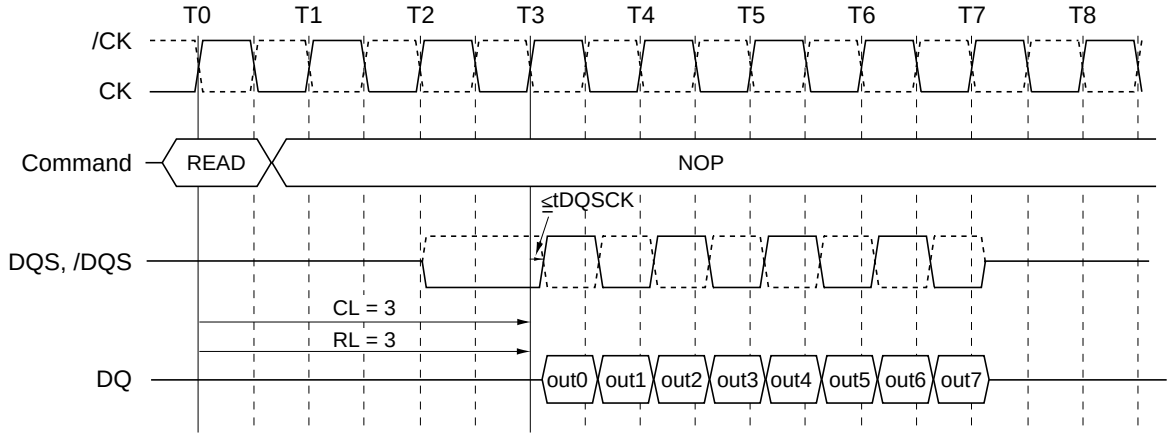
Burst Read Command [READ]

The Burst Read command is initiated by having /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low 1 clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner.

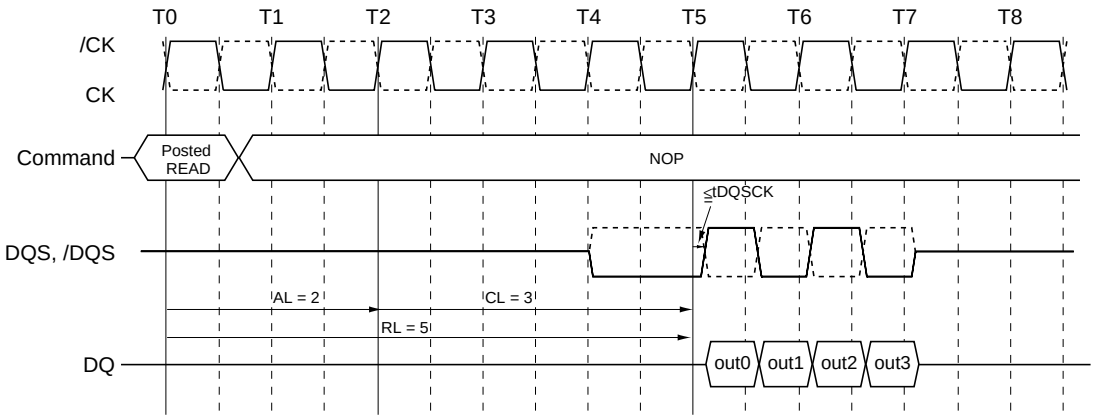
The RL is equal to an additive latency (AL) plus /CAS latency (CL). The CL is defined by the mode register set (MRS), similar to the existing SDR and DDR-I SDRAMs. The AL is defined by the extended mode register set (EMRS).



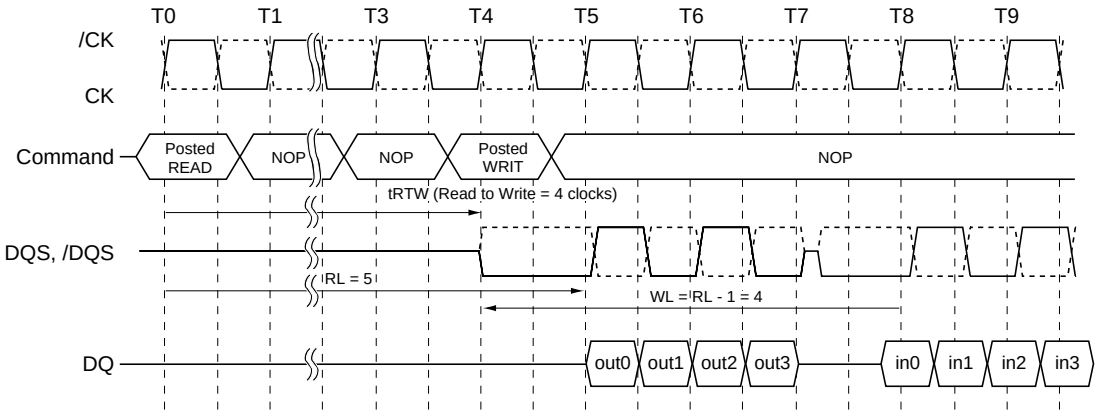
Burst Read Operation (RL = 3, BL = 4 (AL = 0 and CL = 3))



Burst Read Operation (RL = 3, BL = 8 (AL = 0 and CL = 3))

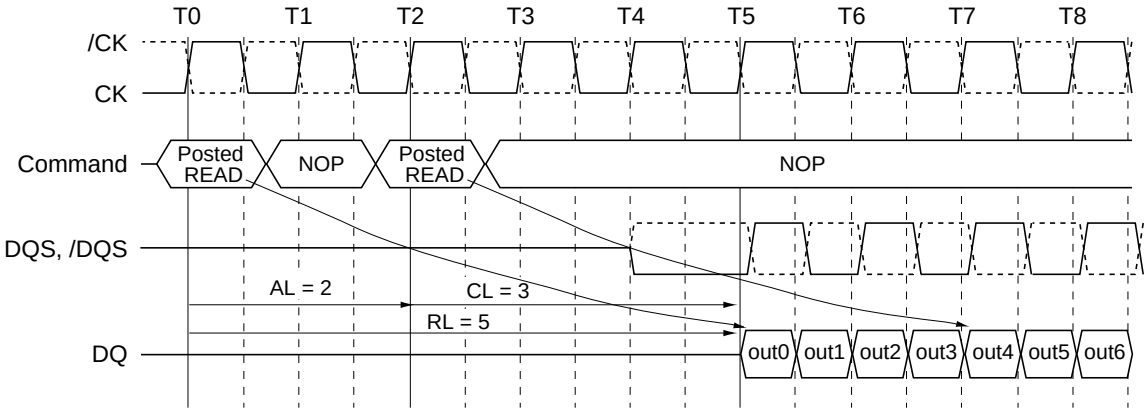


Burst Read Operation (RL = 5, BL = 4 (AL = 2, CL = 3))



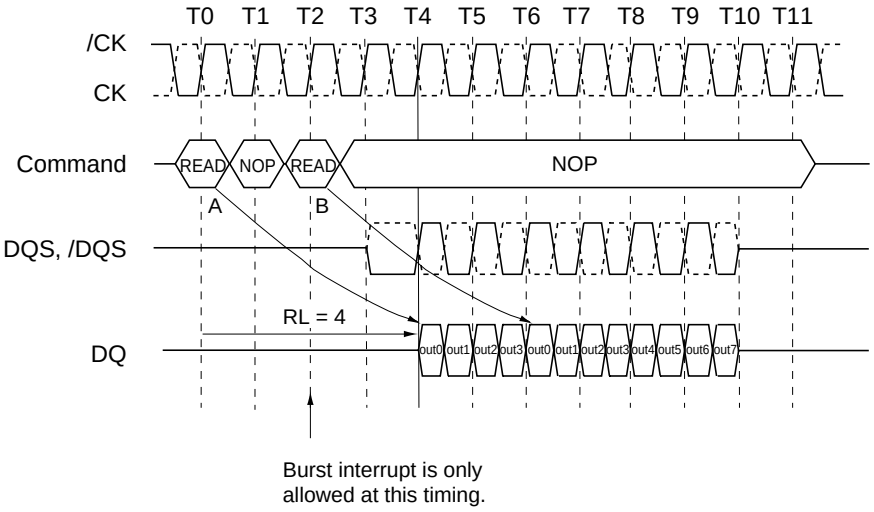
Burst Read followed by Burst Write (RL = 5, WL = RL-1 = 4, BL = 4)

The minimum time from the burst read command to the burst write command is defined by a read-to-write-turn-around-time, which is 4 clocks.



Seamless Burst Read Operation (RL = 5, AL = 2, and CL = 3))

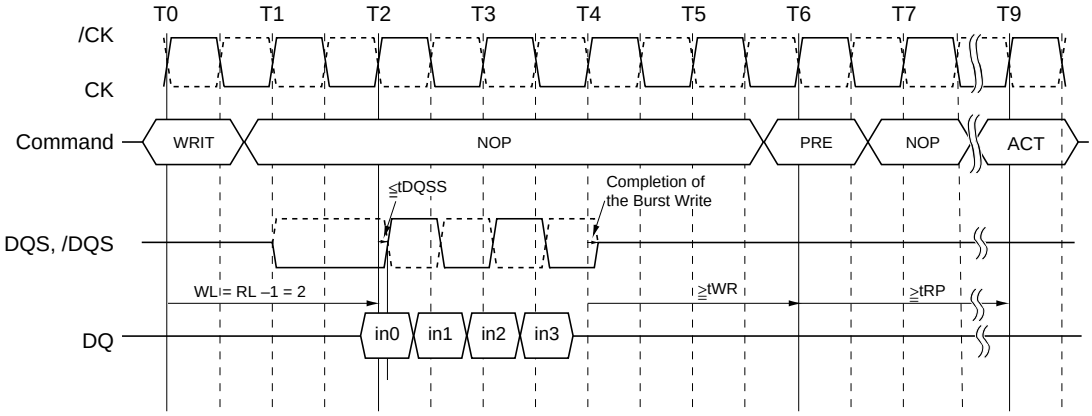
Enabling a read command at every other clock supports the seamless burst read operation. This operation is allowed regardless of same or different banks as long as the banks are activated.



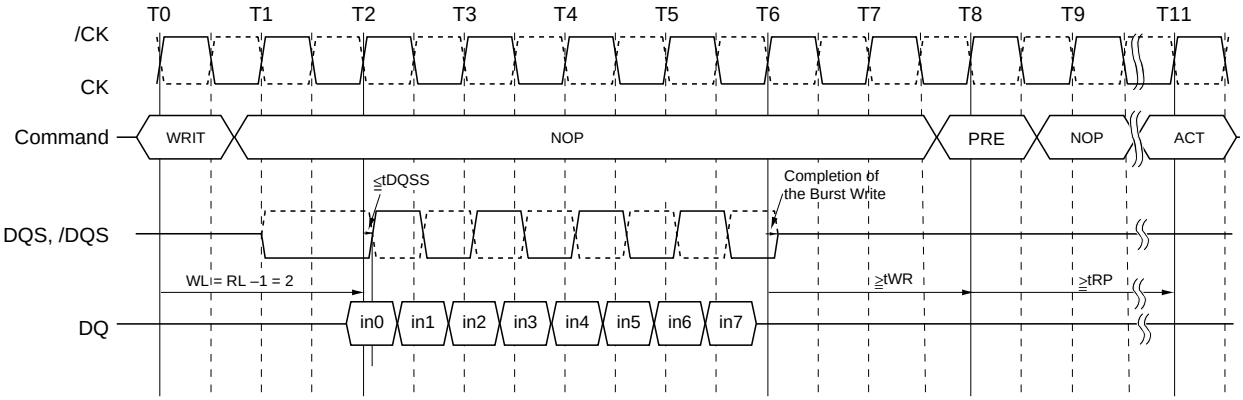
Burst Read Interrupt by Read

Burst Write Command [WRIT]

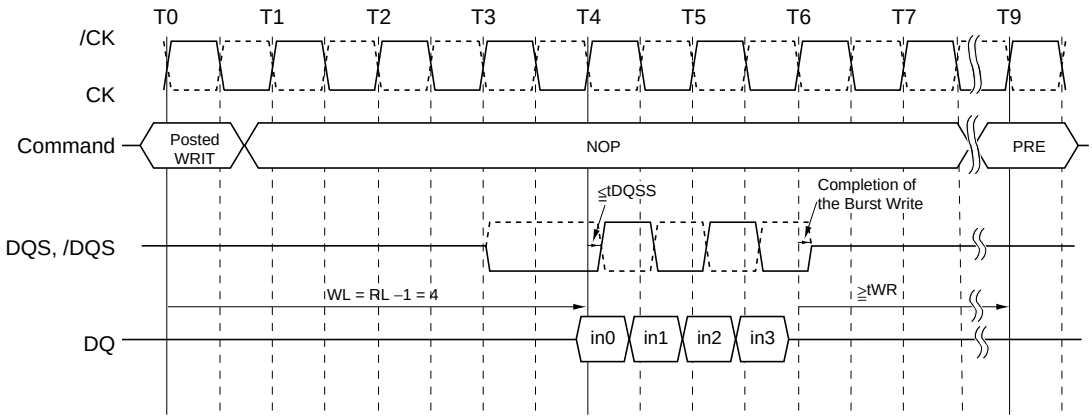
The Burst Write command is initiated by having /CS, /CAS and /WE low while holding /RAS high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL −1). A data strobe signal (DQS) should be driven low (preamble) one clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length of 4 is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (tWR).



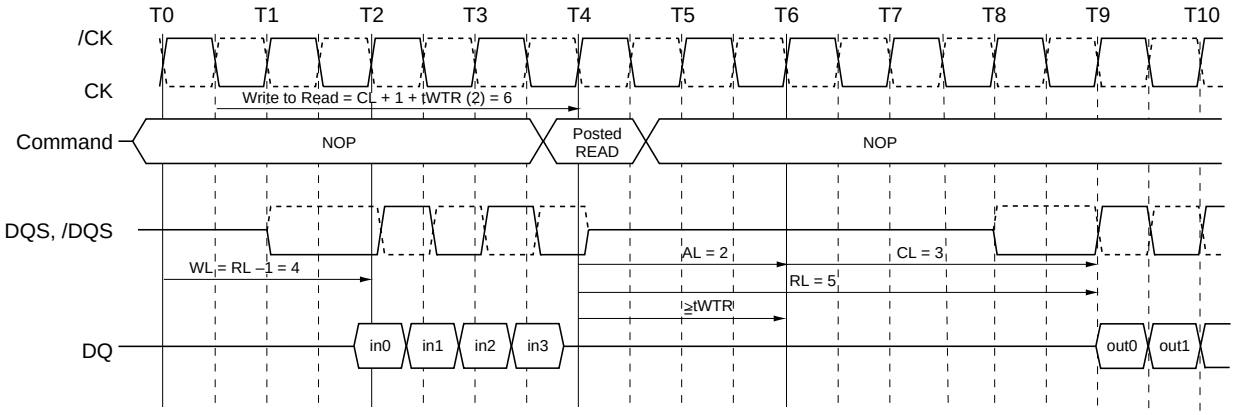
Burst Write Operation (RL = 3, WL = 2, BL = 4 tWR = 2 (AL=0, CL=3))



Burst Write Operation (RL = 3, WL = 2, BL = 8 (AL=0, CL=3))

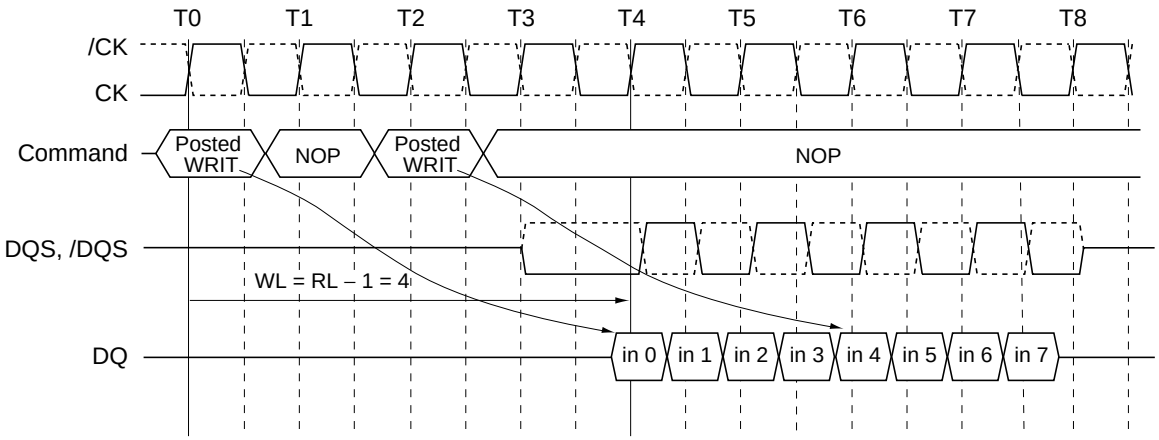


Burst Write Operation (RL = 5, WL = 4, BL = 4 tWR = 3 (AL=2, CL=3))



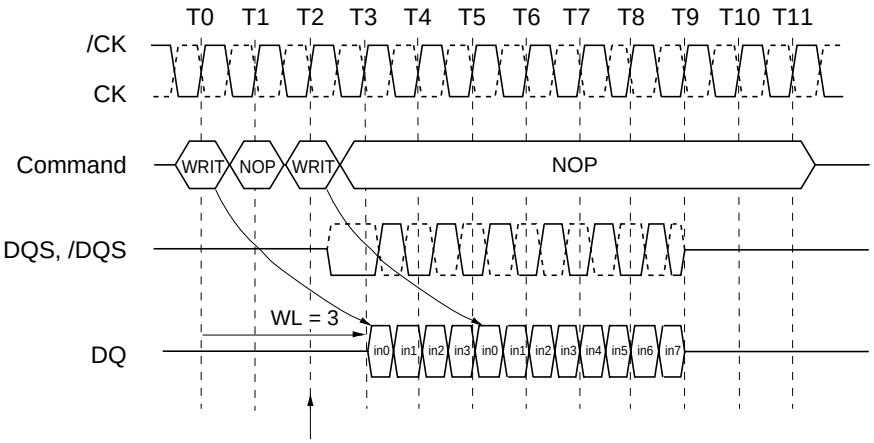
Burst Write followed by Burst Read (RL = 5, BL = 4, WL = 4, tWTR = 2 (AL=2, CL=3))

The minimum number of clock from the burst write command to the burst read command is CL + 1 + a write to-read-turn-around-time (tWTR). This tWTR is not a write recovery time (tWR) but the time required to transfer the 4bit write data from the input buffer into sense amplifiers in the array.



Seamless Burst Write Operation (RL = 5, WL = 4, BL = 4)

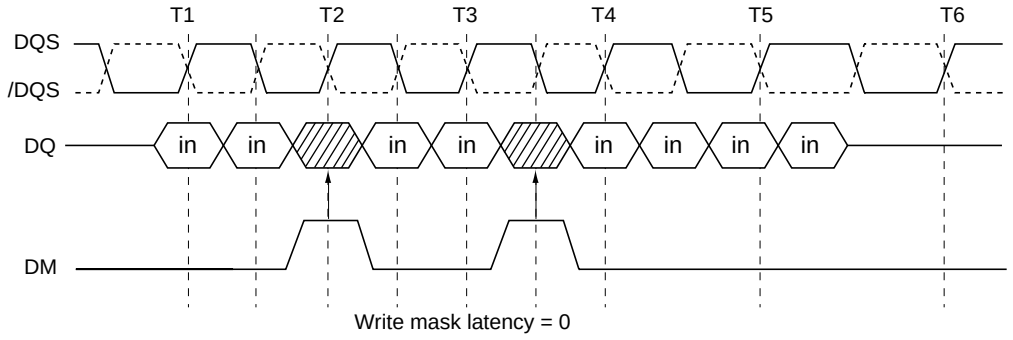
Enabling a write command every other clock supports the seamless burst write operation. This operation is allowed regardless of same or different banks as long as the banks are activated.



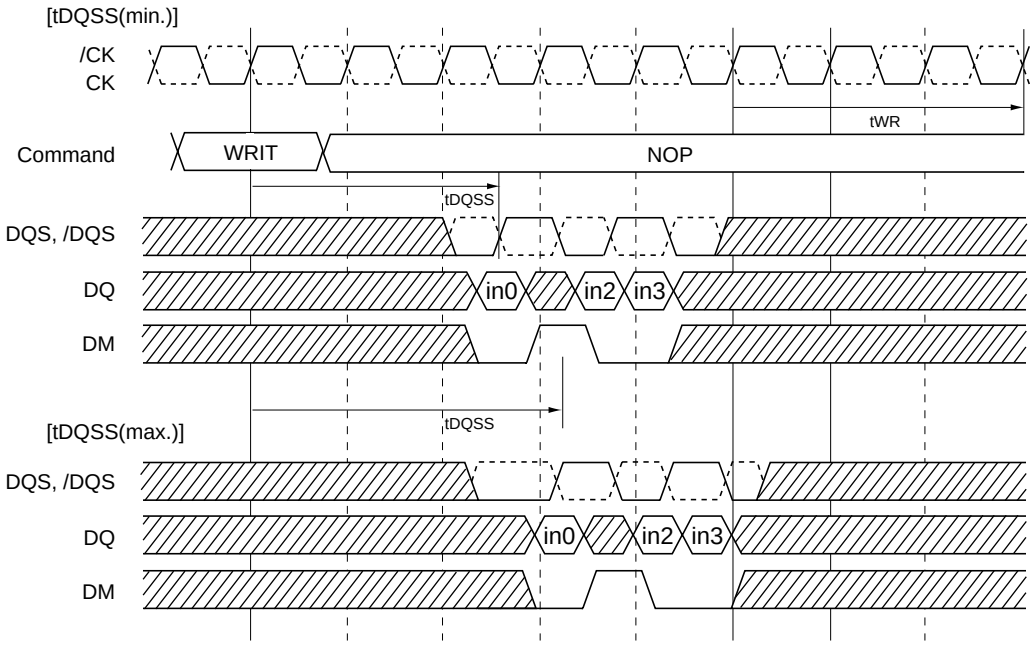
Write interrupt by Write (WL = 3, BL = 8)

Write data mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR-II SDRAMs, Consistent with the implementation on DDR-I SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles.



Data Mask Timing



Data Mask Function, WL = 3, AL = 0 shown

Precharge Command [PRE]

The precharge command is used to precharge or close a bank that has been activated. The precharge command is triggered when /CS, /RAS and /WE are low and /CAS is high at the rising edge of the clock. The precharge command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 are used to define which bank to precharge when the command is issued.

[Bank Selection for Precharge by Address Bits]

A10	BA0	BA1	Precharged Bank(s)
L	L	L	Bank 0 only
L	H	L	Bank 1 only
L	L	H	Bank 2 only
L	H	H	Bank 3 only
H	×	×	All banks 0 to 3

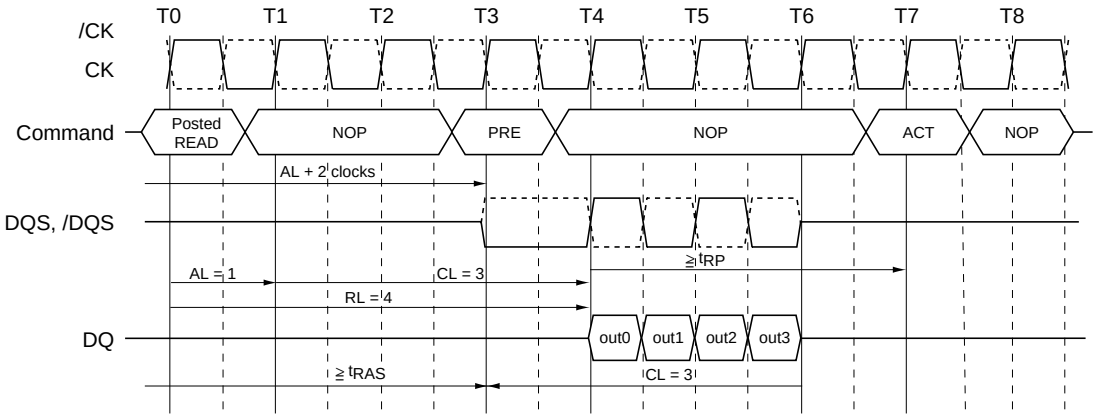
Remark: H: VIH, L: VIL, ×: VIH or VIL

Burst Read Operation Followed by Precharge

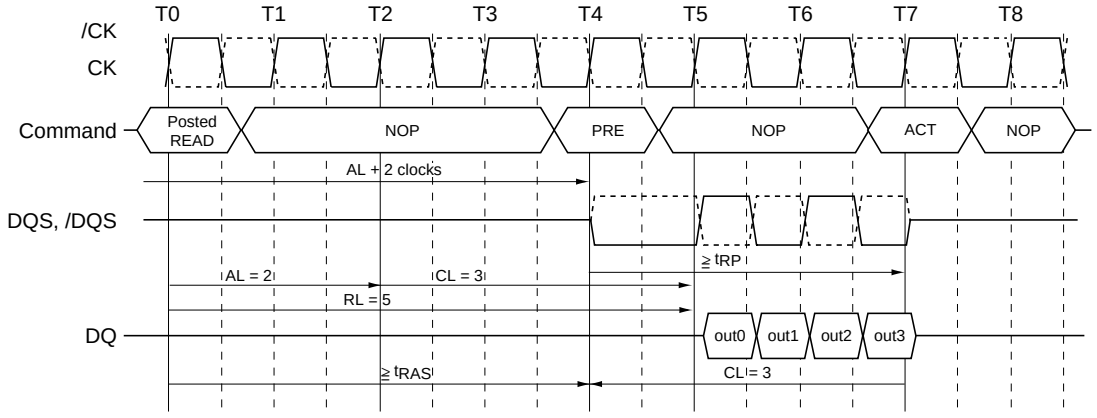
Minimum read to precharge command spacing to the same bank = AL + BL/2 clocks

For the earliest possible precharge, the precharge command may be issued on the rising edge that is

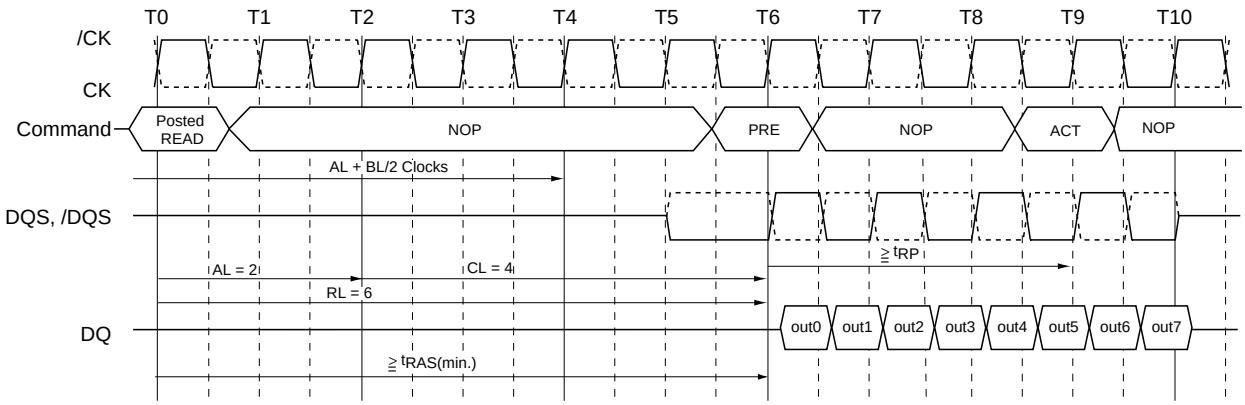
"Additive latency (AL) + BL/2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.



Burst Read Operation Followed by Precharge (RL = 4, BL = 4 (AL=1, CL=3))



Burst Read Operation Followed by Precharge (RL = 5, BL = 4 (AL=2, CL=3))

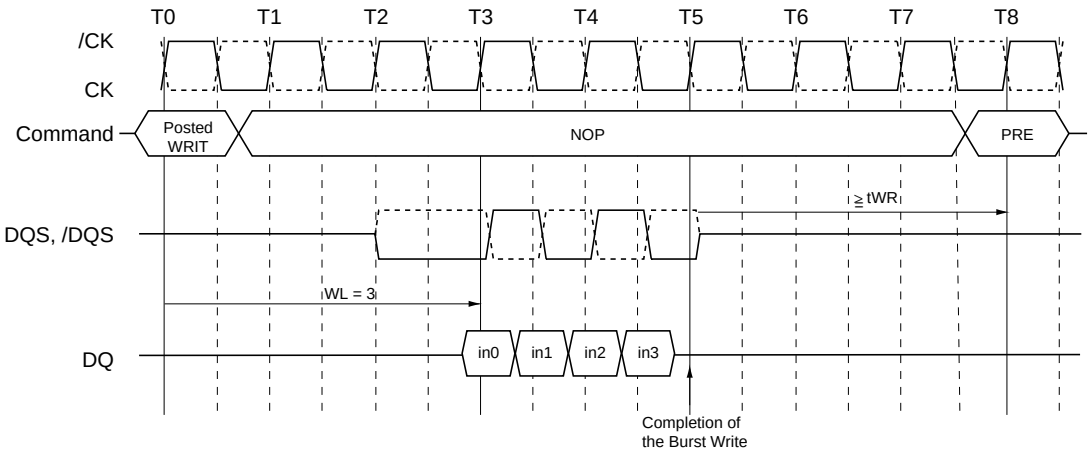


Burst Read Operation Followed by Precharge (RL = 6 (AL=2, CL=4, BL=8))

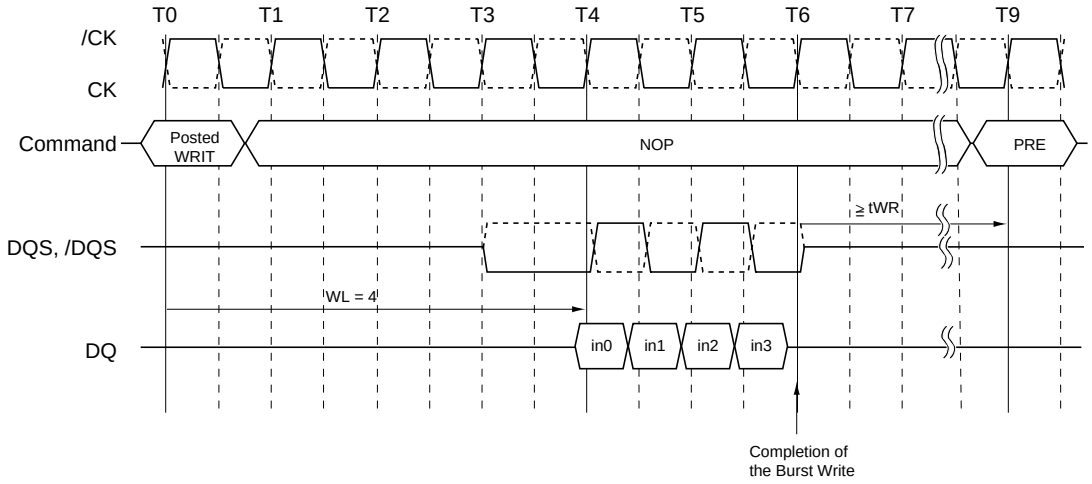
Burst Write followed by Precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clocks + tWR

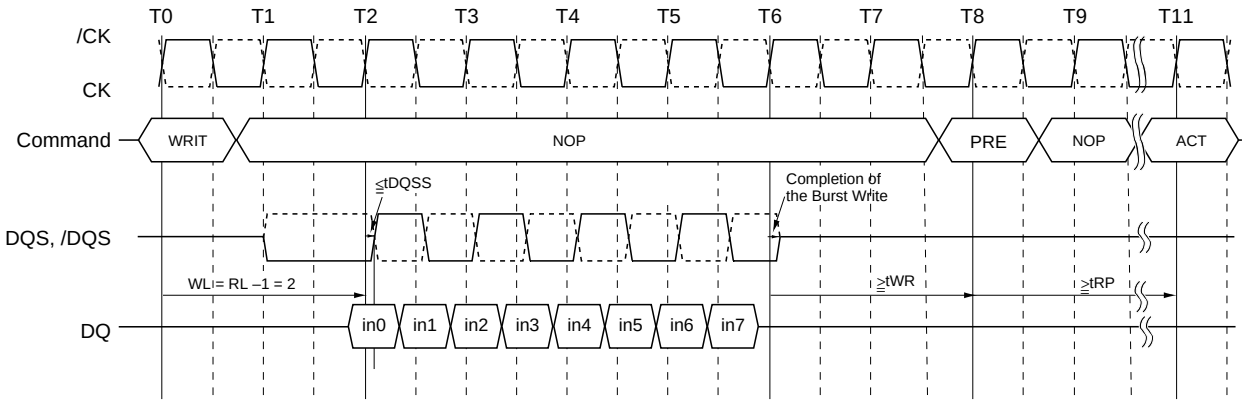
For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the precharge command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No precharge command should be issued prior to the tWR delay, as DDR-II SDRAM allows the burst interrupt operation only Read by Read or Write by Write at the boundary of burst 4.



Burst Write followed by Precharge (WL = (RL-1) =3)



Burst Write followed by Precharge (WL = (RL-1) = 4)



Burst Write followed by Precharge (WL = (RL-1) = 4,BL= 8)

Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the precharge command or the auto-precharge function. When a read or a write command is given to the DDR-II SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the read or write Command is issued, then normal read or write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a read Command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is /CAS latency (CL) clock cycles before the end of the read burst.

Auto-precharge can also be implemented during Write commands. The precharge operation engaged by the Auto precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

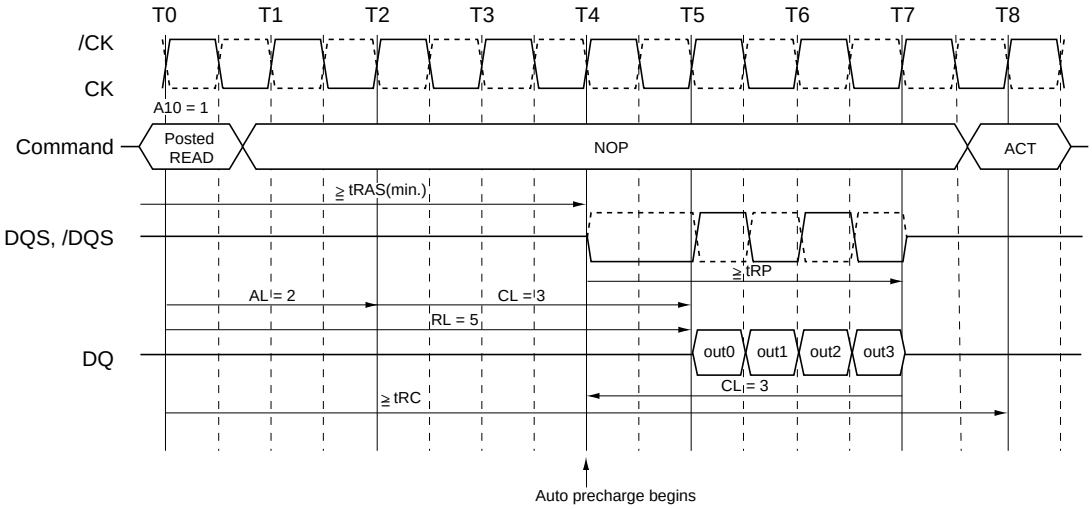
This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon /CAS latency) thus improving system performance for random data access. The /RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed so that the auto precharge command may be issued with any read or write command.

Burst Read with Auto Precharge [READA]

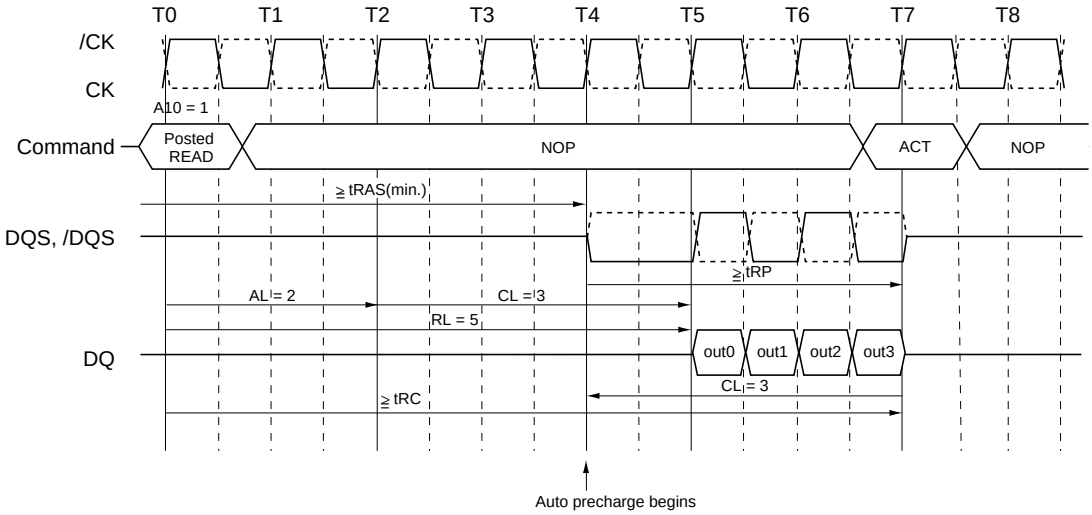
If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR-II SDRAM starts an auto Precharge operation on the rising edge which is (AL + BL/2) cycles later from the read with AP command when the condition that. When tRAS (min) is satisfied. If tRAS (min.) is not satisfied at the edge, the start point so auto-precharge operation will be delayed until tRAS (min.) is satisfied. A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously.

(1) The /RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.

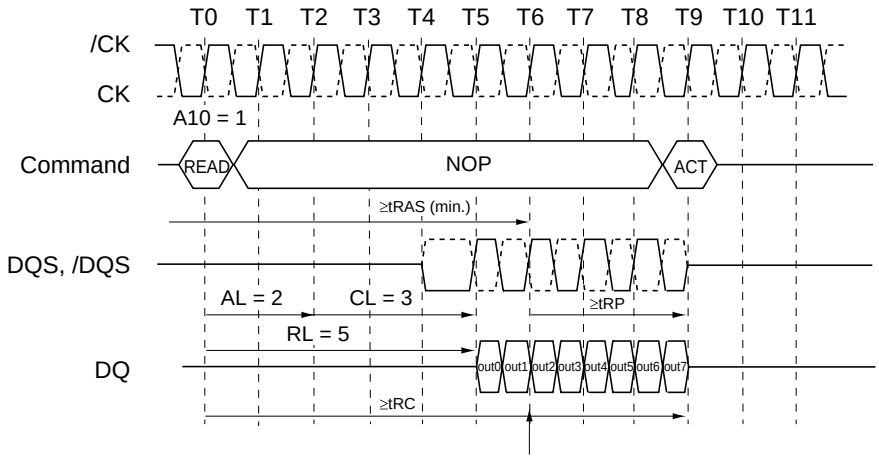
(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.



Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRC limit)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3))



Burst Read with Auto Precharge Followed by an Activation to the Same Bank (tRP limit)
(RL = 5, BL = 4 (AL = 2, CL = 3, internal tRCD = 3)



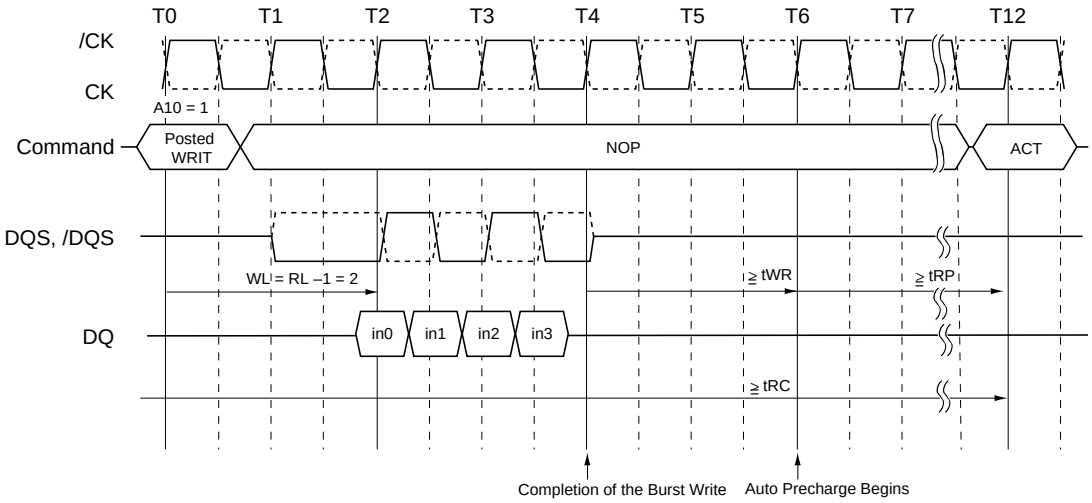
Burst Read with Auto Precharge Followed by an Activation to the Same Bank
(RL = 5, BL = 8 (AL = 2, CL = 3)

Burst Write with Auto-Precharge [WRITA]

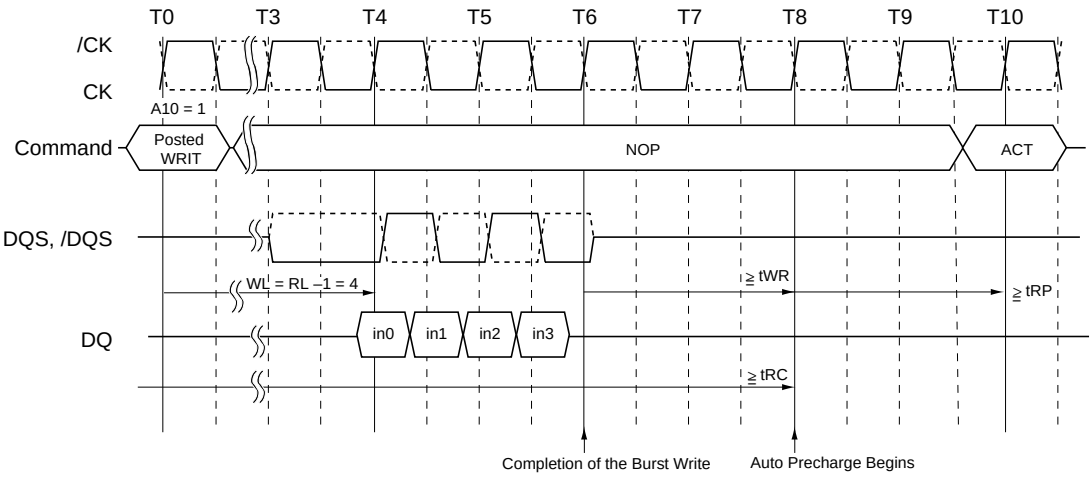
If A10 is high when a write command is issued, the Write with auto-precharge function is engaged. The DDR-II SDRAM automatically begins precharge operation after the completion of the burst writes plus write recovery time (tWR). The bank undergoing auto-precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

(1) The data-in to bank activate delay time (tWR + tRP) has been satisfied.

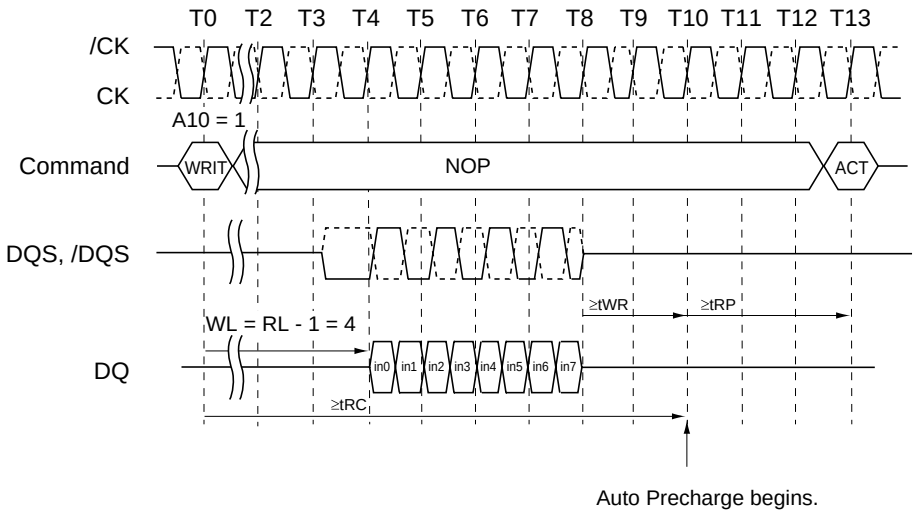
(2) The /RAS cycle time (tRC) from the previous bank activation has been satisfied.



Burst Write with Auto-Precharge (tRC Limit) (WL = 2, tWR =2, tRP=3)



Burst Write with Auto-Precharge (tWR + tRP) (WL = 4, tWR =2, tRP=3)



Burst Write with Auto Precharge Followed by an Activation to the Same Bank (WL = 4, BL = 8, tWR = 2, tRP = 3)

Refresh Requirements

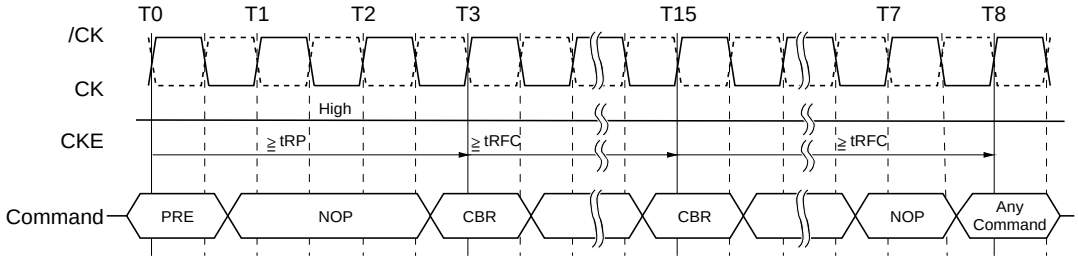
DDR-II SDRAM requires a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways: by an explicit Automatic Refresh command, or by an internally timed event in Self Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defines the average refresh interval, tREFI, which is a guideline to controllers for distributed refresh timing.

Automatic Refresh Command (/CAS Before /RAS Refresh) [REF]

When /CS, /RAS and /CAS are held low and /WE high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). All banks of the DDR-II SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Auto Refresh Command (CBR) can be applied. An address counter, internal to the device, supplies the bank address during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the DDR-II SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the Auto Refresh cycle time (tRFC).

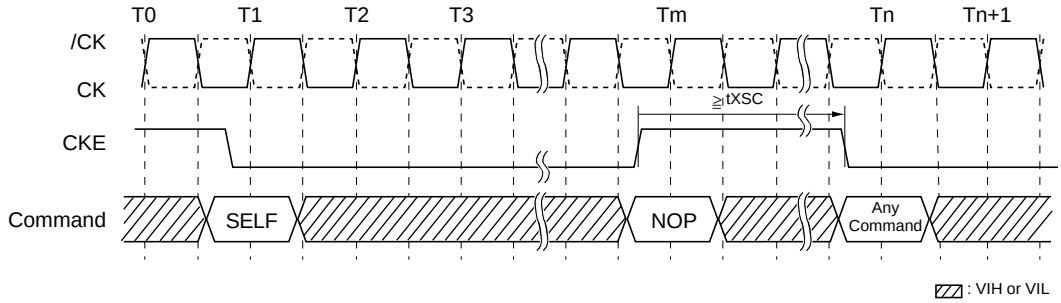
The DDR-II SDRAM requires Automatic Refresh cycles at an average periodic interval of tREFI (maximum). A maximum of eight Automatic Refresh commands can be posted to any given DDR-II SDRAM, and the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 8 × tREFI.



Automatic Refresh Command

Self Refresh Command [SELF]

The DDR-II SDRAM device has a built-in timer to accommodate Self Refresh operation. The self refresh command is defined by having /CS, /RAS, /CAS and CKE held low with /WE high at the rising edge of the clock. Once the Command is registered, CKE must be held low to keep the device in self refresh mode. When the SDRAM has entered self refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during self refresh operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit self refresh operation. Once the clock is cycling, the exit command will be registered asynchronously by bringing CKE high. After CKE is brought high, an internal timer is started to insure CKE is held high for approximately 10ns before registering the self refresh exit command. The purpose of this circuit is to filter out noise glitches on the CKE input that may cause the DDR-II SDRAM to erroneously exit self refresh operation. Once the self refresh command is registered, a delay equal or longer than the tXSC must be satisfied before any command can be issued to the device. CKE must remain high for the entire Self Refresh exit period (tXSC) and commands must be gated off with /CS held High. Alternatively, NOP commands may be registered on each positive clock edge during the self refresh exit interval. (Self Refresh Command)

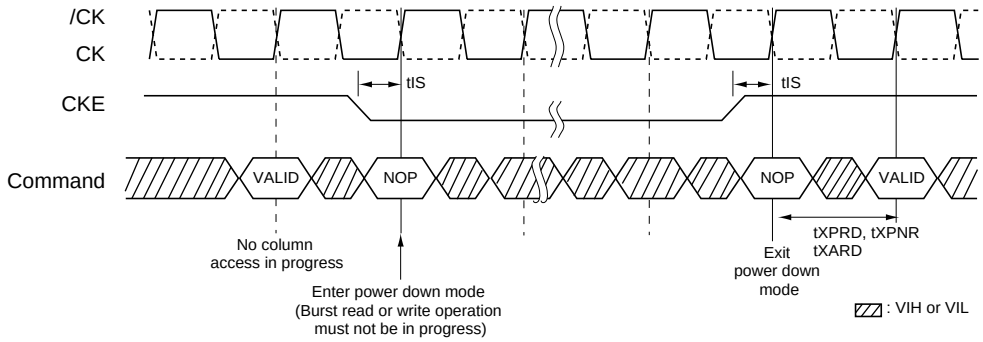


Self Refresh Command

Power-Down [PDEN]

Power-down is entered when CKE is registered (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK, /CK and CKE. In power down mode, CKE Low and a stable clock signal must be maintained at the inputs of the DDR-II SDRAM, and all other input signals are "VIH or VIL". Power-down duration is limited by the refresh requirements of the device.

The power-down state is synchronously exited when CKE is registered High (along with a NOP or DESL). A valid, executable command may be applied after satisfied tXPRD or tXARD for read command exiting form precharge power-down or active power-down respectively ,and after satisfied tXPNR for non-read command.



Power Down

Burst Interruption

Interruption of a burst read or write cycle is prohibited.

No Operation Command [NOP]

The no operation command should be used in cases when the DDR-II SDRAM is in an idle or a wait state. The purpose of the no operation command is to prevent the DDR-II SDRAM from registering any unwanted commands between operations. A no operation command is registered when /CS is low with /RAS, /CAS, and /WE held high at the rising edge of the clock. A no operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

Deselect Command [DESL]

The deselect command performs the same function as a no operation command. Deselect Command occurs when /CS is brought high at the rising edge of the clock, the /RAS, /CAS, and /WE signals become don't cares.

Package Drawing

64-ball FBGA(μBGA) (TBD)

Solder ball: Lead free (Sn-Ag-Cu)

80-ball FBGA(μBGA) (TBD)

Solder ball: Lead free (Sn-Ag-Cu)

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDE51XXGBSA.

Type of Surface Mount Device

EDE51XXGBSA: 64-ball μBGA, 80-ball μBGA < Lead free (Sn-Ag-Cu) >

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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