## DESCRIPTION

The Hynix HYM71V32D735HCT4 Series are 32Mx72bits ECC Synchronous DRAM Modules. The modules are composed of eighteen 32Mx4bits CMOS Synchronous DRAMs in 400mil 54pin TSOP-II package, one 2Kbit EEPROM in 8pin TSSOP package on a 200pin glass-epoxy printed circuit board. One 0.22uF and one 0.0022uF decoupling capacitors per each SDRAM are mounted on the PCB.

The Hynix HYM71V32D735HCT4 Series are Dual In-line Memory Modules suitable for easy interchange and addition of 256Mbytes memory. The Hynix HYM71V32D735HCT4 Series are fully synchronous operation referenced to the positive edge of the clock . All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

## FEATURES

- PC133MHz support
- 200pin SDRAM Registered DIMM
- Serial Presence Detect with EEPROM
- 1.75" (44.45mm) Height PCB with double sided components
- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- Data mask function by DQM
- SDRAM internal banks : four banks
- Module bank : one physical bank
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4 or 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{CAS}$ Latency ; 2, 3 Clocks

## ORDERING INFORMATION

| Part No. | Clock Frequency | Internal Bank | Ref. | Power | SDRAM Package | Plating |
|---|---|---|---|---|---|---|
| HYM71V32D735HCT4-K | 133MHz | 4 Banks | 4K | Normal | TSOP-II | Gold |
| HYM71V32D735HCT4-H | | | | | | |

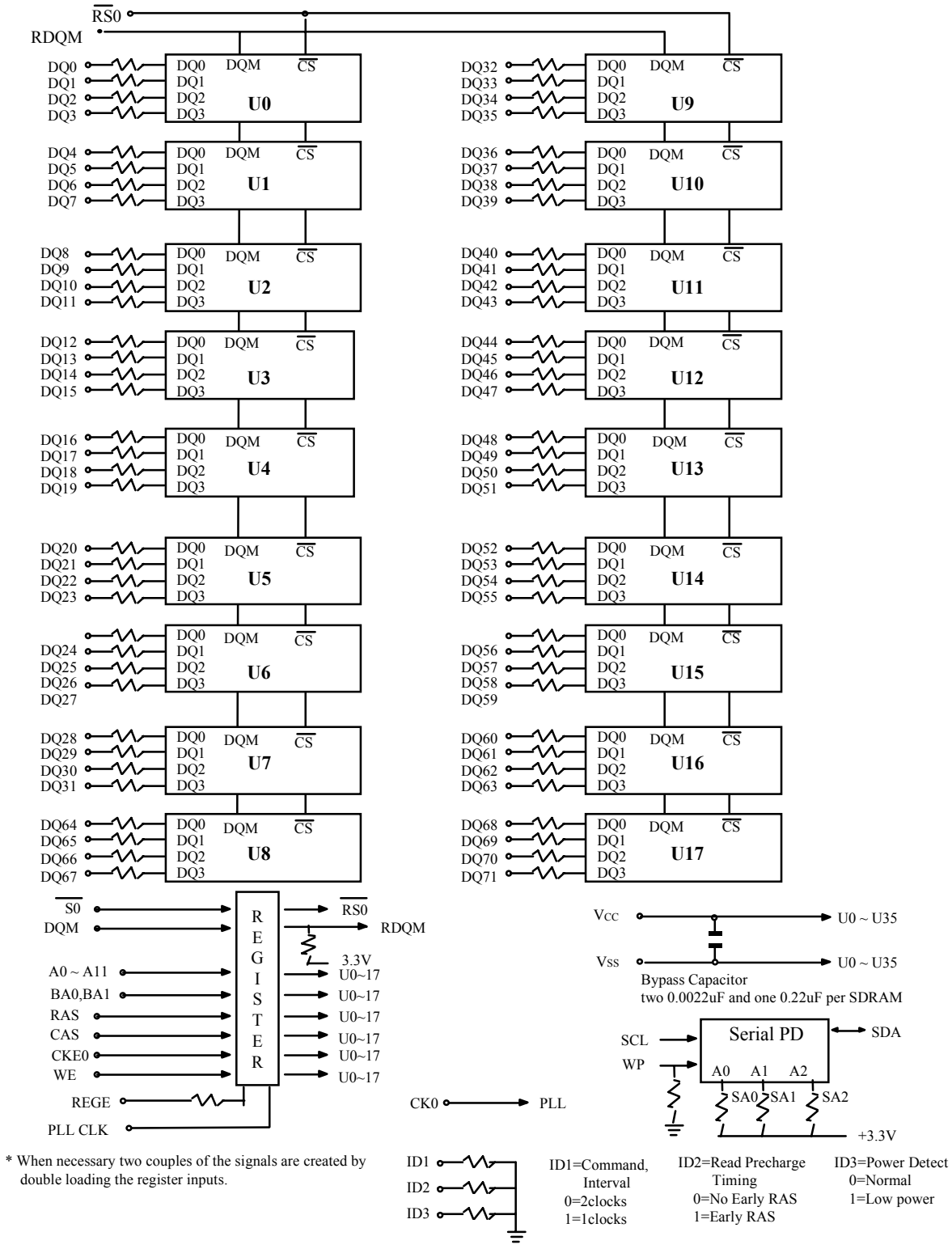
## PIN DESCRIPTION

| PIN | PIN NAME | DESCRIPTION |
|---|---|---|
| CK0 | Clock Inputs | The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK |
| CKE0 | Clock Enable | Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh |
| /S0 | Chip Select | Enables or disables all inputs except CK, CKE and DQM |
| BA0, BA1 | SDRAM Bank Address | Selects bank to be activated during /RAS activity<br>Selects bank to be read/written during /CAS activity |
| A0 ~ A11 | Address | Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA9, CA11<br>Auto-precharge flag : A10 |
| /RAS, /CAS, /WE | Row Address Strobe, Column Address Strobe, Write Enable | /RAS, /CAS and /WE define the operation<br>Refer function truth table for details |
| REGE | Register Enable | Register Enable pin which permits the DIMM to operateion in Buffered Mode when REGE input is Low, in Registered Mode when REGE input is High |
| DQM | Data Input/Output Mask | Controls output buffers in read mode and masks input data in write mode |
| DQ0 ~ DQ71 | Data Input/Output | Multiplexed data input / output pin |
| VCC | Power Supply (3.3V) | Power supply for internal circuits and input buffers |
| VSS | Ground | Ground |
| SCL | SPD Clock Input | Serial Presence Detect Clock input |
| SDA | SPD Data Input/Output | Serial Presence Detect Data input/output |
| SA0~2 | SPD Address Input | Serial Presence Detect Address Input |
| WP | Write Protect for SPD | Write Protect for Serial Presence Detect on DIMM |
| ID1~3 | Identification Detect | Commend Interval, Read Precharge Timing, Power Detect |
| NC | No Connection | No connection |

## PIN ASSIGNMENTS

| PIN NO. | NAME | PIN NO. | NAME | PIN NO. | NAME | PIN NO. | NAME |
|---|---|---|---|---|---|---|---|
| 1 | VDD | 51 | VSS | 101 | NC, VTT | 151 | CK0 |
| 2 | NC, VTT | 52 | RAS | 102 | NC, VTT | 152 | VSS |
| 3 | NC, VTT | 53 | VSS | 103 | VSS | 153 | NC |
| 4 | IN | 54 | NC | 104 | NC | 154 | S0 |
| 5 | OUT | 55 | A13 | 105 | RFU | 155 | VSS |
| 6 | ID1 | 56 | VDD | 106 | RFU | 156 | A12 |
| 7 | ID2 | 57 | A0 | 107 | ID3 | 157 | A10 |
| 8 | VSS | 58 | A1 | 108 | DQ71 | 158 | VDD |
| 9 | DQ67 | 59 | VSS | 109 | DQ70 | 159 | A2 |
| 10 | DQ66 | 60 | DQ35 | 110 | VSS | 160 | A3 |
| 11 | VDD | 61 | DQ34 | 111 | DQ69 | 161 | VSS |
| 12 | DQ65 | 62 | VDD | 112 | DQ68 | 162 | DQ31 |
| 13 | DQ64 | 63 | DQ33 | 113 | VDD | 163 | DQ30 |
| 14 | VSS | 64 | DQ32 | 114 | NC | 164 | VDD |
| 15 | DQ63 | 65 | VSS | 115 | VSS | 165 | DQ29 |
| 16 | DQ62 | 66 | DQ27 | 116 | NC | 166 | DQ28 |
| 17 | NC, VTT | 67 | DQ26 | 117 | DQ59 | 167 | VSS |
| 18 | DQ61 | 68 | VSS | 118 | DQ58 | 168 | DQ23 |
| 19 | DQ60 | 69 | DQ25 | 119 | VSS | 169 | DQ22 |
| 20 | VDD | 70 | DQ24 | 120 | DQ57 | 170 | VDD |
| 21 | NC | 71 | VSS | 121 | DQ56 | 171 | DQ21 |
| 22 | NC | 72 | DQ19 | 122 | VDD | 172 | DQ20 |
| 23 | VSS | 73 | DQ18 | 123 | DQ55 | 173 | VSS |
| 24 | NC | 74 | VDD | 124 | DQ54 | 174 | NC |
| 25 | NC | 75 | DQ17 | 125 | VSS | 175 | NC |
| 26 | VDD | 76 | DQ16 | 126 | DQ53 | 176 | VDD |
| 27 | DQ51 | 77 | VSS | 127 | DQ52 | 177 | NC |
| 28 | DQ50 | 78 | NC | 128 | VDD | 178 | VSS |
| 29 | VSS | 79 | NC, VTT | 129 | DQ47 | 179 | VSS |
| 30 | DQ49 | 80 | VDD | 130 | DQ46 | 180 | NC |
| 31 | DQ48 | 81 | DQ15 | 131 | VSS | 181 | NC |
| 32 | VDD | 82 | DQ14 | 132 | DQ45 | 182 | VDD |
| 33 | DQ43 | 83 | VSS | 133 | DQ44 | 183 | DQ11 |
| 34 | DQ42 | 84 | DQ13 | 134 | VDD | 184 | DQ10 |
| 35 | VSS | 85 | DQ12 | 135 | DQ39 | 185 | VSS |
| 36 | DQ41 | 86 | VDD | 136 | DQ38 | 186 | DQ9 |
| 37 | DQ40 | 87 | DQ7 | 137 | VSS | 187 | DQ8 |
| 38 | VDD | 88 | DQ6 | 138 | DQ37 | 188 | VDD |
| 39 | A4 | 89 | VSS | 139 | DQ36 | 189 | DQ3 |
| 40 | A5 | 90 | DQ5 | 140 | VDD | 190 | DQ2 |
| 41 | GND | 91 | DQ4 | 141 | A6 | 191 | VSS |
| 42 | A8 | 92 | VDD | 142 | A7 | 192 | DQ1 |
| 43 | A9 | 93 | PDE# | 143 | VSS | 193 | DQ0 |
| 44 | VDD | 94 | PD1 | 144 | A11 | 194 | SDA |
| 45 | NC | 95 | PD2 | 145 | NC | 195 | SA0 |
| 46 | CKE0 | 96 | PD3 | 146 | VDD | 196 | SA1 |
| 47 | VSS | 97 | PD4 | 147 | DQM | 197 | SA2 |
| 48 | CAS | 98 | SCL | 148 | WE | 198 | VDD |
| 49 | NC, VTT | 99 | NC | 149 | VSS | 199 | NC, VTT |
| 50 | VDD | 100 | VSS | 150 | NC | 200 | NC, VTT |

## BLOCK DIAGRAM




* When necessary two couples of the signals are created by double loading the register inputs.

## SERIAL PRESENCE DETECT

| BYTE NUMBER | FUNCTION DESCRIPTION | FUNCTION | | VALUE | | NOTE |
|---|---|---|---|---|---|---|
| | | -K | -H | -K | -H | |
| BYTE0 | # of Bytes Written into Serial Memory at Module Manufacturer | 128 Bytes | | 80h | | |
| BYTE1 | Total # of Bytes of SPD Memory Device | 256 Bytes | | 08h | | |
| BYTE2 | Fundamental Memory Type | SDRAM | | 04h | | |
| BYTE3 | # of Row Addresses on This Assembly | 12 | | 0Ch | | 1 |
| BYTE4 | # of Column Addresses on This Assembly | 11 | | 0Bh | | |
| BYTE5 | # of Module Banks on This Assembly | 1 Bank | | 01h | | |
| BYTE6 | Data Width of This Assembly | 72 Bits | | 48h | | |
| BYTE7 | Data Width of This Assembly (Continued) | - | | 00h | | |
| BYTE8 | Voltage Interface Standard of This Assembly | LVTTL | | 01h | | |
| BYTE9 | SDRAM Cycle Time @/CAS Latency=3 | 7.5ns | 7.5ns | 75h | 75h | |
| BYTE10 | Access Time from Clock @/CAS Latency=3 | 5.4ns | 5.4ns | 54h | 54h | |
| BYTE11 | DIMM Configuration Type | ECC | | 02h | | |
| BYTE12 | Refresh Rate/Type | 15.625us / Self Refresh Supported | | 80h | | |
| BYTE13 | Primary SDRAM Width | x4 | | 04h | | |
| BYTE14 | Error Checking SDRAM Width | x4 | | 04h | | |
| BYTE15 | Minimum Clock Delay Back to Back Random Column Address | tCCD = 1 CLK | | 01h | | |
| BYTE16 | Burst Lenth Supported | 1,2,4,8,Full Page | | 8Fh | | 2 |
| BYTE17 | # of Banks on Each SDRAM Device | 4 Banks | | 04h | | |
| BYTE18 | SDRAM Device Attributes, /CAS Lataency | /CAS Latency=2,3 | | 06h | | |
| BYTE19 | SDRAM Device Attributes, /CS Lataency | /CS Latency=0 | | 01h | | |
| BYTE20 | SDRAM Device Attributes, /WE Lataency | /WE Latency=0 | | 01h | | |
| BYTE21 | SDRAM Module Attributes | Registered/Buffered inputs, with PLL | | 1Fh | | |
| BYTE22 | SDRAM Device Attributes, General | +/- 10% voltage tolerence, Burst Read Single Bit Write, Precharge All, Auto Precharge, Early RAS Precharge | | 0Eh | | |
| BYTE23 | SDRAM Cycle Time @/CAS Latency=2 | 7.5ns | 10ns | 75h | A0h | |
| BYTE24 | Access Time from Clock @/CAS Latency=2 | 5.4ns | 6ns | 54h | 60h | |
| BYTE25 | SDRAM Cycle Time @/CAS Latency=1 | - | - | 00h | 00h | |
| BYTE26 | Access Time from Clock @/CAS Latency=1 | - | - | 00h | 00h | |
| BYTE27 | Minimum Row Precharge Time (tRP) | 15ns | 20ns | 0Fh | 14h | |
| BYTE28 | Minimum Row Active to Row Active Delay (tRRD) | 15ns | 15ns | 0Fh | 0Fh | |
| BYTE29 | Minimum /RAS to /CAS Delay (tRCD) | 15ns | 20ns | 0Fh | 14h | |
| BYTE30 | Minimum /RAS Pulse Width (tRAS) | 45ns | 45ns | 2Dh | 2Dh | |
| BYTE31 | Module Bank Density | 256MB | | 40h | | |
| BYTE32 | Command and Address Signal Input Setup Time | 1.5ns | 1.5ns | 15h | 15h | |
| BYTE33 | Command and Address Signal Input Hold Time | 0.8ns | 0.8ns | 08h | 08h | |
| BYTE34 | Data Signal Input Setup Time | 1.5ns | 1.5ns | 15h | 15h | |
| BYTE35 | Data Signal Input Hold Time | 0.8ns | 0.8ns | 08h | 08h | |
| BYTE36 ~61 | Superset Information (may be used in future) | - | | 00h | | |
| BYTE62 | SPD Revision | Intel SPD 1.2B | | 12h | | 3, 8 |
| BYTE63 | Checksum for Byte 0~62 | - | | B8h | F9h | |
| BYTE64 | Manufacturer JEDEC ID Code | Hynix JEDED ID | | ADh | | |
| BYTE65 ~71 | ....Manufacturer JEDEC ID Code | Unused | | FFh | | |
| BYTE72 | Manufacturing Location | HSI(Korea Area)<br>HSA (United States Area)<br>HSE (Europe Area)<br>HSJ (Japan Area)<br>HSS(Singapore)<br>Asia Area | | 0*h<br>1*h<br>2*h<br>3*h<br>4*h<br>5*h | | 9 |

*Continued*

| BYTE NUMBER | FUNCTION DESCRIPTION | FUNCTION | | VALUE | | NOTE |
|---|---|---|---|---|---|---|
| | | -K | -H | -K | -H | |
| BYTE73 | Manufacturer's Part Number (Component) | 7 (SDRAM) | | 37h | | 4, 5 |
| BYTE74 | Manufacturer's Part Number (128Mb based) | **1** | | 31h | | 4, 5 |
| BYTE75 | Manufacturer's Part Number (Voltage Interface) | V (3.3V, LVTTL) | | 56h | | 4, 5 |
| BYTE76 | Manufacturer's Part Number (Memory Width) | 3 | | 33h | | 4, 5 |
| BYTE77 | ....Manufacturer's Part Number (Memory Width) | 2 | | 32h | | 4, 5 |
| BYTE78 | Manufacturer's Part Number (Module Type) | D | | 44h | | 4, 5 |
| BYTE79 | Manufacturer's Part Number (Data Width) | 7 | | 37h | | 4, 5 |
| BYTE80 | ....Manufacturer's Part Number (Data Width) | 3 | | 33h | | 4, 5 |
| BYTE81 | Manufacturer's Part Number (Refresh, SDRAM Bank) | 5 (4K Refresh, 4Banks) | | 35h | | 4, 5 |
| BYTE82 | Manufacturer's Part Number (Generation) | H | | 48h | | 4, 5 |
| BYTE83 | Manufacturer's Part Number (Generation) | C | | 43h | | 4, 5 |
| BYTE84 | Manufacturer's Part Number (Package Type) | T | | 54h | | 4, 5 |
| BYTE85 | Manufacturer's Part Number (Component Configuration) | 4 (x4 based) | | 34h | | 4, 5 |
| BYTE86 | Manufacturer's Part Number (Hyphent) | - (Hyphen) | | 2Dh | | 4, 5 |
| BYTE87 | Manufacturer's Part Number (Min. Cycle Time) | K | H | 4Bh | 48h | 4, 5 |
| BYTE88 ~90 | Manufacturer's Part Number | Blanks | | 20h | | 4, 5 |
| BYTE91 | Revision Code (for Component) | Process Code | | - | | 4, 6 |
| BYTE92 | ....Revision Code (for PCB) | Process Code | | - | | 4, 6 |
| BYTE93 | Manufacturing Date | Year | | - | | 3, 6 |
| BYTE94 | ....Manufacturing Date | Work Week | | - | | 3, 6 |
| BYTE95 ~98 | Assembly Serial Number | Serial Number | | - | | 6 |
| BYTE99 ~125 | Manufacturer Specific Data (may be used in future) | None | | 00h | | |
| BYTE126 | System Frequency Support | 100MHz | | 64h | | 7, 8 |
| BYTE127 | Intel Specification Details for 100MHz Support | Refer to Note7 | | 8Fh | | 7, 8 |
| BYTE128 ~256 | Unused Storage Locations | - | | 00h | | |

Note :
1. The bank address is excluded
2. 1, 2, 4, 8 for Interleave Burst Type
3. BCD adopted
4. ASCII adopted
5. Basically Hynix writes Part No. except for 'HYM' in Byte 73~90 to use the limited 18 bytes from byte 73 to byte 90
6. Not fixed but dependent
7. CK0 connected to DIMM, TBD junction temp, CL2(3) support, Intel defined Concurrent Auto Precharge support
8. Refer to Intel SPD Specification 1.2B
9. Refer to HSI Web site.

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Ambient Temperature | TA | 0 ~ 70 | °C |
| Storage Temperature | TSTG | -55 ~ 125 | °C |
| Voltage on Any Pin relative to VSS | VIN, VOUT | -1.0 ~ 4.6 | V |
| Voltage on VDD relative to VSS | VDD, VDDQ | -1.0 ~ 4.6 | V |
| Short Circuit Output Current | IOS | 50 | mA |
| Power Dissipation | PD | 18 | W |
| Soldering Temperature · Time | TSOLDER | 260 · 10 | °C · Sec |

**Note :** Operation at above absolute maximum rating can adversely affect device reliability.

## DC OPERATING CONDITION (TA=0 to 70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VDD, VDDQ | 3.0 | 3.3 | 3.6 | V | 1 |
| Input High voltage | VIH | 2.0 | 3.0 | VDDQ + 0.3 | V | 1,2 |
| Input Low voltage | VIL | -0.3 | 0 | 0.8 | V | 1,3 |

**Note :**
1.All voltages are referenced to VSS = 0V
2.VIH(max) is acceptable 5.6V AC pulse width with <=3ns of duration.
3.VIL(min) is acceptable -2.0V AC pulse width with <=3ns of duration.

## AC OPERATING TEST CONDITION (TA=0 to 70°C, VDD=3.3±0.3V, VSS=0V)

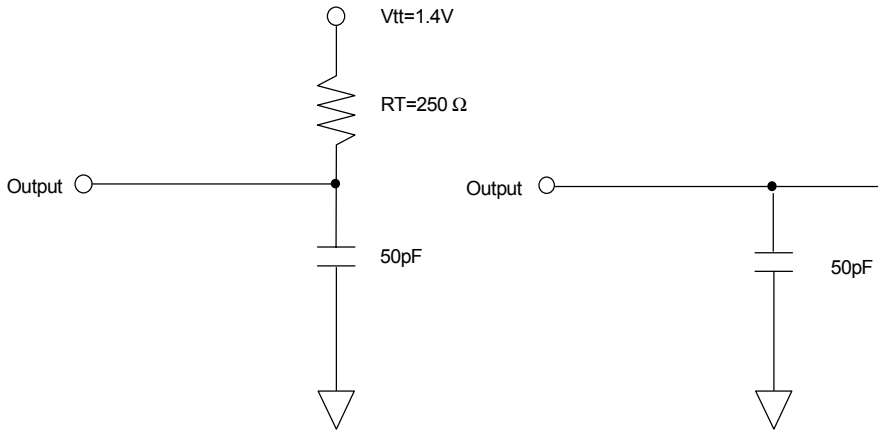
| Parameter | Symbol | Value | Unit | Note |
|---|---|---|---|---|
| AC Input High / Low Level Voltage | VIH / VIL | 2.4/0.4 | V | |
| Input Timing Measurement Reference Level Voltage | Vtrip | 1.4 | V | |
| Input Rise / Fall Time | tR / tF | 1 | ns | |
| Output Timing Measurement Reference Level Voltage | Voutref | 1.4 | V | |
| Output Load Capacitance for Access Time Measurement | CL | 50 | pF | 1 |

**Note :**
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (50pF). For details, refer to AC/DC output load circuit

## CAPACITANCE (TA=25°C, f=1MHz)

| Parameter | Pin | Symbol | -K/H | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Input Capacitance | CK0 | $C_{I1}$ | - | 44 | pF |
| | CKE0 | $C_{I2}$ | - | 20 | pF |
| | /S0, /S2 | $C_{I3}$ | - | 20 | pF |
| | A0~11, BA0, BA1 | $C_{I4}$ | - | 20 | pF |
| | /RAS, /CAS, /WE | $C_{I5}$ | - | 20 | pF |
| | DQM0~DQM7 | $C_{I6}$ | - | 20 | pF |
| Data Input / Output Capacitance | DQ0 ~ DQ63 | $C_{I/O}$ | - | 20 | pF |

## OUTPUT LOAD CIRCUIT




DC Output Load Circuit

AC Output Load Circuit

## DC CHARACTERISTICS I (TA=0 to 70°C, VDD=3.3±0.3V)

| Parameter | Symbol | Min. | Max | Unit | Note |
|---|---|---|---|---|---|
| Input Leakage Current | ILI | -10 | 10 | uA | 1 |
| Output Leakage Current | ILO | -1 | 1 | uA | 2 |
| Output High Voltage | VOH | 2.4 | - | V | IOH = -2mA |
| Output Low Voltage | VOL | - | 0.4 | V | IOL = +2mA |

**Note :**
1.VIN = 0 to 3.6V, All other pins are not tested under VIN =0V
2.DOUT is disabled, VOUT=0 to 3.6

## DC CHARACTERISTICS II

| Parameter | Symbol | Test Condition | | Speed | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | | -K | -H | | |
| Operating Current | IDD1 | Burst length=1, One bank active<br>tRC ≥ tRC(min), IOL=0mA | | **2400** | **2400** | mA | 1 |
| Precharge Standby Current in Power Down Mode | IDD2P | CKE ≤ VIL(max), tCK = 15ns | | 356 | | mA | |
| | IDD2PS | CKE ≤ VIL(max), tCK = ∞ | | 178 | | | |
| Precharge Standby Current in Non Power Down Mode | IDD2N | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 30ns. All other pins ≥ VDD-0.2V or ≤ 0.2V | | 570 | | mA | |
| | IDD2NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable. | | 570 | | | |
| Active Standby Current in Power Down Mode | IDD3P | CKE ≤ VIL(max), tCK = 15ns | | 320 | | mA | |
| | IDD3PS | CKE ≤ VIL(max), tCK = ∞ | | 155 | | | |
| Active Standby Current in Non Power Down Mode | IDD3N | CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 15ns<br>Input signals are changed one time during 30ns. All other pins ≥ VDD-0.2V or ≤ 0.2V | | 840 | | mA | |
| | IDD3NS | CKE ≥ VIH(min), tCK = ∞<br>Input signals are stable. | | 400 | | | |
| Burst Mode Operating Current | IDD4 | tCK ≥ tCK(min), IOL=0mA<br>All banks active | CL=3 | **3000** | **3000** | mA | 1 |
| | | | CL=2 | **3300** | **3300** | | |
| Auto Refresh Current | IDD5 | tRRC ≥ tRRC(min), All banks active | | **4900** | | mA | 2 |
| Self Refresh Current | IDD6 | CKE ≤ 0.2V | | 276 | | mA | |

**Note :**
1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2. Min. of tRRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II

## AAC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

| Parameter | | Symbol | -K | | -H | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| System Clock Cycle Time | $\overline{CAS}$ Latency = 3 | tCK3 | 7.5 | 1000 | 7.5 | 1000 | ns | 1 |
| | $\overline{CAS}$ Latency = 2 | tCK2 | 7.5 | | 10 | | | |
| Clock High Pulse Width | | tCHW | 2.5 | - | 2.5 | - | ns | 2 |
| Clock Low Pulse Width | | tCLW | 2.5 | - | 2.5 | - | ns | 2 |
| Access Time From Clock | $\overline{CAS}$ Latency = 3 | tAC3 | - | 5.4 | - | 5.4 | ns | 3 |
| | $\overline{CAS}$ Latency = 2 | tAC2 | - | 5.4 | - | 6 | ns | |
| Data-Out Hold Time | | tOH | 2.7 | - | 2.7 | - | ns | |
| Data-Input Setup Time | | tDS | 1.5 | - | 1.5 | - | ns | 2 |
| Data-Input Hold Time | | tDH | 0.8 | - | 0.8 | - | ns | 2 |
| Address Setup Time | | tAS | 1.5 | - | 1.5 | - | ns | 2 |
| Address Hold Time | | tAH | 0.8 | - | 0.8 | - | ns | 2 |
| CKE Setup Time | | tCKS | 1.5 | - | 1.5 | - | ns | 2 |
| CKE Hold Time | | tCKH | 0.8 | - | 0.8 | - | ns | 2 |
| Command Setup Time | | tCS | 1.5 | - | 1.5 | - | ns | 2 |
| Command Hold Time | | tCH | 0.8 | - | 0.8 | - | ns | 2 |
| CLK to Data Output in Low-Z Time | | tOLZ | 1 | - | 1 | - | ns | |
| CLK to Data Output in High-Z Time | $\overline{CAS}$ Latency = 3 | tOHZ3 | 2.7 | 5.4 | 2.7 | 5.4 | ns | |
| | $\overline{CAS}$ Latency = 2 | tOHZ2 | 2.7 | 5.4 | 3 | 6 | ns | |

**Note :**

1. In Registered DIMM, data is delayed an additional clock cycle due to the register (this is, Device CL + 1 = DIMM CL)
2. Assume tR / tF (input rise and fall time ) is 1ns, If tR & tF > 1ns, then [(tR+tF)/2-1]ns should be added to the parameter
3. Access times to be measured with input signals of 1v/ns edge rate, from 0.8v to 2.0v
   If tR > 1ns, then (tR/2-0.5)ns should be added to the parameter

## AC CHARACTERISTICS II

| Parameter | | Symbol | -K | | -H | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | | |
| $\overline{RAS}$ Cycle Time | Operation | tRC | 60 | - | 65 | - | ns | |
| | Auto Refresh | tRRC | 60 | - | 65 | - | ns | |
| $\overline{RAS}$ to $\overline{CAS}$ Delay | | tRCD | 15 | - | 20 | - | ns | |
| $\overline{RAS}$ Active Time | | tRAS | 45 | 100K | 45 | 100K | ns | |
| $\overline{RAS}$ Precharge Time | | tRP | 15 | - | 20 | - | ns | |
| $\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay | | tRRD | 15 | - | 15 | - | ns | |
| $\overline{CAS}$ to $\overline{CAS}$ Delay | | tCCD | 1 | - | 1 | - | CLK | |
| Write Command to Data-In Delay | | tWTL | 0 | - | 0 | - | CLK | 1 |
| Data-In to Precharge Command | | tDPL | 1 | - | 1 | - | CLK | 1 |
| Data-In to Active Command | | tDAL | 4 | - | 5 | - | CLK | 1 |
| DQM to Data-Out Hi-Z | | tDQZ | 2 | - | 2 | - | CLK | 1 |
| DQM to Data-In Mask | | tDQM | 0 | - | 0 | - | CLK | |
| MRS to New Command | | tMRD | 2 | - | 2 | - | CLK | |
| Precharge to Data Output Hi-Z | $\overline{CAS}$ Latency = 3 | tPROZ3 | 4 | - | 4 | - | CLK | 1 |
| | $\overline{CAS}$ Latency = 2 | tPROZ2 | 3 | - | 3 | - | | |
| Power Down Exit Time | | tPDE | 1 | - | 1 | - | CLK | |
| Self Refresh Exit Time | | tSRE | 1 | - | 1 | - | CLK | 2 |
| Refresh Time | | tREF | - | 64 | - | 64 | ms | |

**Note :**
1. Timing delay due to the register is considered in a registered DIMM
2. A new command can be given tRRC after self refresh exit

## DEVICE OPERATING OPTION TABLE

### HYM71V32D735HCT4-K

| | $\overline{\text{CAS}}$ Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| **133MHz(7.5ns)** | 2CLKs | 2CLKs | 6CLKs | 8CLKs | 2CLKs | 5.4ns | 2.7ns |
| **125MHz(8ns)** | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |
| **100MHz(10ns)** | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |

### HYM71V32D735HCT4-H

| | $\overline{\text{CAS}}$ Latency | tRCD | tRAS | tRC | tRP | tAC | tOH |
|---|---|---|---|---|---|---|---|
| **133MHz(7.5ns)** | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 5.4ns | 2.7ns |
| **125MHz(8ns)** | 3CLKs | 3CLKs | 6CLKs | 9CLKs | 3CLKs | 6ns | 3ns |
| **100MHz(10ns)** | 2CLKs | 2CLKs | 5CLKs | 7CLKs | 2CLKs | 6ns | 3ns |

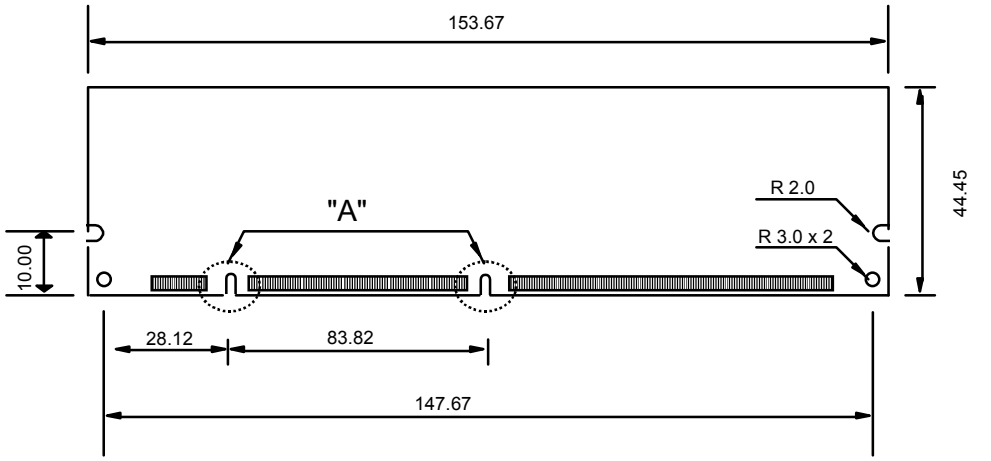
## COMMAND TRUTH TABLE

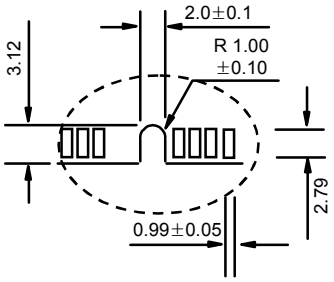
| Command | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | DQM | ADDR | A10/ AP | BA | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | | H | X | L | L | L | L | X | OP code | | | |
| No Operation | | H | X | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| Bank Active | | H | X | L | L | H | H | X | RA | | V | |
| Read | | H | X | L | H | L | H | X | CA | L | V | |
| Read with Autoprecharge | | | | | | | | | | H | | |
| Write | | H | X | L | H | L | L | X | CA | L | V | |
| Write with Autoprecharge | | | | | | | | | | H | | |
| Precharge All Banks | | H | X | L | L | H | L | X | X | H | X | |
| Precharge selected Bank | | | | | | | | | | L | V | |
| Burst Stop | | H | X | L | H | H | L | X | X | | | |
| DQM | | H | X | | | | | V | X | | | |
| Auto Refresh | | H | H | L | L | L | H | X | X | | | |
| Burst-Read-Single-WRITE | | H | X | L | L | L | L | X | A9 Pin High (Other Pins OP code) | | | MRS Mode |
| Self Refresh[1] | Entry | H | L | L | L | L | H | X | X | | | |
| | Exit | L | H | H | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | |
| Precharge power down | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | H | H | H | | | | | |
| | Exit | L | H | H | X | X | X | X | | | | |
| | | | | L | H | H | H | | | | | |
| Clock Suspend | Entry | H | L | H | X | X | X | X | X | | | |
| | | | | L | V | V | V | | | | | |
| | Exit | L | H | X | | | | X | | | | |

**Note :**
1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don't care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation
3. The burst read sigle write mode is entered by programming the Write burst mode bit (A9) in the mode register to a logic 1.

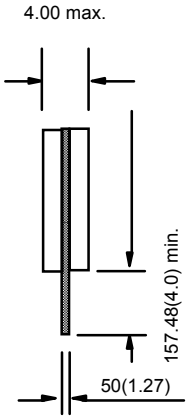
## PACKAGE DEMENSION

Unit: mm




DETAIL "A"




NOTES :
1. ALL DIMENSIONS ARE IN MILIMETERS
2. TOLERANCES ON ALL DIMMENSIONS ±0.127 UNLESS OTHERWISE.