Integrated Device Technology, Inc.

CMOS FLASH A/D CONVERTER

IDT75C48

FEATURES:

- 8-bit resolution
- 30 MSPS conversion rate
- Guaranteed no missing codes
- Pin- and function-compatible with TRW 1048
- Low power consumption: 500mW
- Extended analog input range
- On-chip EDC (Error Detection and Correction)
- Improved output logic HIGH drive, no pull-up needed
- No sample and hold required
- Differential Phase < 1 Degree
- Differential Gain < 2%
- Selectable output formats
- TTL-compatible
- Available in 28-pin CERDIP and LCC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88743 is listed for this function

DESCRIPTION:

The IDT75C48 is a 30 MegaSample per Second (MSPS), fully parallel, 8-bit Flash Analog to Digital Converter. The wide input analog bandwidth of 10MHz permits the conversion of analog input signals with full-power frequency components up to this limit with no input sample and hold. Low power consumption due to CEMOS™ processing, virtually eliminates thermal considerations. The IDT75C48 is available in 28-pin plastic and hermetic DIPs and a 28-pin LCC.

The IDT75C48 consists of a reference voltage generator, 255 comparators, encoding and EDC (Error Detection and Correction) logic and an output data register. A single clock starts the conversion process and controls all internal operations. Two control inputs allow the output coding format to be programmed for straight binary or offset two's complement in either the true or inverted form.

The IDT75C48 military Flash A/D Converters are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

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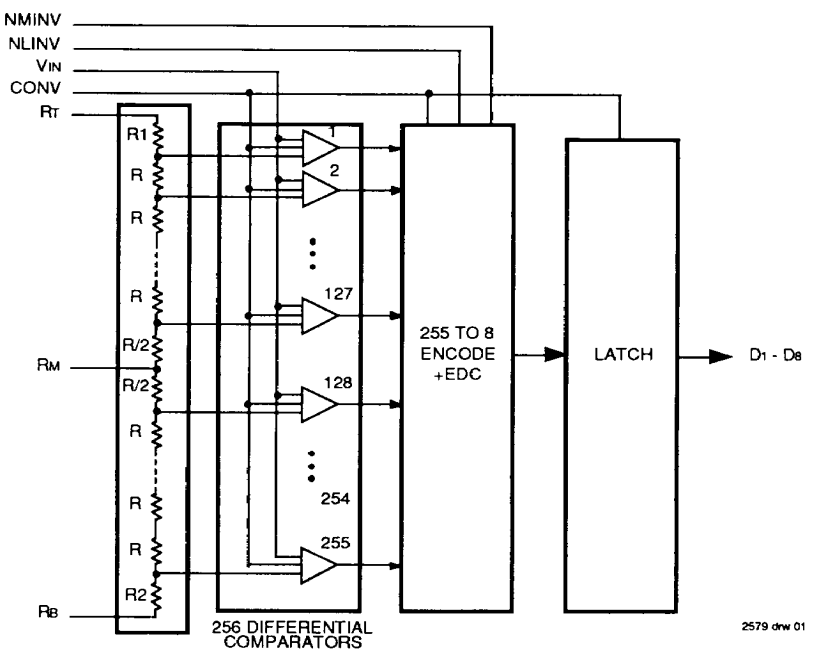
FUNCTIONAL BLOCK DIAGRAM



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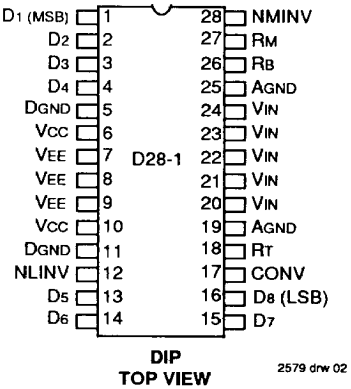
PIN CONFIGURATIONS



DIP
TOP VIEW

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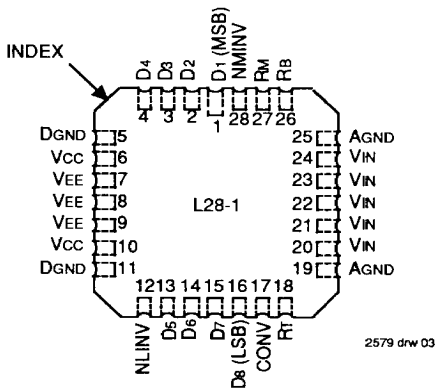

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LCC
TOP VIEW

GENERAL INFORMATION

The IDT75C48 has four functional sections: a comparator array, a reference voltage generator, encoding logic with EDC and output logic. The comparator array compares the input signal with 255 reference voltages to produce an N - of - 255 code. This is sometimes called a "Thermometer" code because all of the comparators with their reference voltage less than the input signal will be "on" while those with their reference above the input will be "off".

The reference voltage generator consists of a string of precisely matched resistors which generate the 255 voltages needed by the comparators. The voltages at the ends of the resistor string set the maximum and minimum conversion range and are typically 0V and −2V, respectively.

The encoding logic converts the "Thermometer" code into binary or offset two's complement numbers and can invert either code. Included in the encoding function is Error Detection and Correction logic which ensures that a corrupted Thermometer code is correctly encoded.

The output logic latches and holds the data constant between samples. The output timing is designed for an easy interface to external latches or memories using the same clock as the ADC.

POWER

The IDT75C48 requires two power supply voltages, V_{CC} and V_{EE}. Typically, V_{EE} = −5.2V and V_{CC} = +5.0V. Two separate grounds are provided, AGND and DGND, the analog and digital grounds. The difference between AGND and DGND must not exceed ± 0.1V and all power and ground pins must be connected.

REFERENCE

The IDT75C48 converts analog input signals that are within the range of the reference ($V_{RB} \leq V_{IN} \leq V_{RT}$) into digital form. V_{RB} (Reference Bottom) and V_{RT} (Reference Top) are applied across the reference resistor chain and both must be within the range of +2.1V to −2.1V. In addition, the voltage applied across the reference resistor chain (V_{RT}–V_{RB}) must be between 1.8V and 2.2V, with V_{RT} more positive than V_{RB}. Nominally, V_{RT} = 0.0V and V_{RB} = −2.0V.

The IDT75C48 provides a midpoint tap, RM, which allows the converter to be adjusted for optimum linearity or a non-linear transfer function. Adjustment of RM is not necessary to meet the linearity specification. Figure 5 shows a circuit which will provide approximately 1/2 LSB adjustment of the midpoint. The characteristic impedance of RM is about 170Ω and this node should be driven from a low impedance source. Any noise introduced at this point will couple directly into the resistor chain, seriously affecting performance.

Due to the unavoidable coupling with the clock and the input signal, R_T and R_B should provide low AC impedance to ground. For applications with a fixed reference, a bypass capacitor is recommend.

CONTROL

The IDT75C48 provides two function control pins, NMINV and NLINV. These controls are for steady state use and are usually tied to the appropriate voltages. They control the output coding format in either straight binary or offset two's complement. In addition, both formats may be either true or inverted. These pins are active low and perform the functions shown in Figure 1.

CONVERT

The IDT75C48 begins a conversion with every rising edge of the convert signal, CONV. The analog input signal is sampled on the rising edge of CONV, while the outputs of the comparators are encoded on the falling edge. The next rising edge latches the encoder output which is presented on the output pins.

The input sample is taken within 15ns of the rising edge of CONV. This is called t_{STO} or the Sampling Time Offset. This delay varies by a few nanoseconds from part to part and as a

function of temperature, but the short term uncertainty or jitter is less than 60ps.

If the maximum CONV pulse width HIGH time (tPWH) is exceeded, the accuracy of the input sample may be impaired. The maximum CONV pulse width LOW time (tPWL) may be exceeded, but the digital output data for the sample taken by the previous rising edge of CONV will be meaningless. It is recommended that CONV be held LOW during longer periods of inactivity.

The digital output data is presented at tD, the Digital Output Delay Time, after the next rising edge of CONV. Previous output data is held for the tHO (Output Hold Time) after the rising edge of CONV to allow for non-critical timing in the external circuitry. This means that the data for samples N is acquired while the converter is taking sample N + 2.

ANALOG INPUT

The IDT75C48 uses strobed, auto-zeroing, latching comparators. All five analog input pins must be connected together as close to the package as possible.

If the analog input signal is within the reference voltage range, the output will be a binary number between 0 and 255. An input signal above VRT will yield a full-scale positive output while an input below VRB will cause a full-scale negative output.

Step	Range		Binary		Offset Two's	
	–2.0000V FS 7.8431mV/Step	–2.0480V FS 8.000mV/Step	*NMINV=1 NLINV=1	NMINV=0 NLINV=0	NMINV=0 NLINV=1	NMINV=1 NLINV=0
000	0.0000V	0.0000V	00000000	11111111	10000000	01111111
001	–0.0078V	–0.0080V	00000001	11111110	10000001	01111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	–0.9961V	–0.0160V	01111111	10000000	11111111	00000000
128	–1.0039V	–1.0240V	10000000	01111111	00000000	11111111
129	–1.0118V	–1.0320V	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
254	–1.9921V	–2.0320V	11111110	00000001	01111110	10000001
255	–2.0000V	–2.0400V	11111111	00000000	01111111	10000000

*When NMINV and NLINV are both high a 1KΩ series resistor must be inserted between NMINV and VCC.

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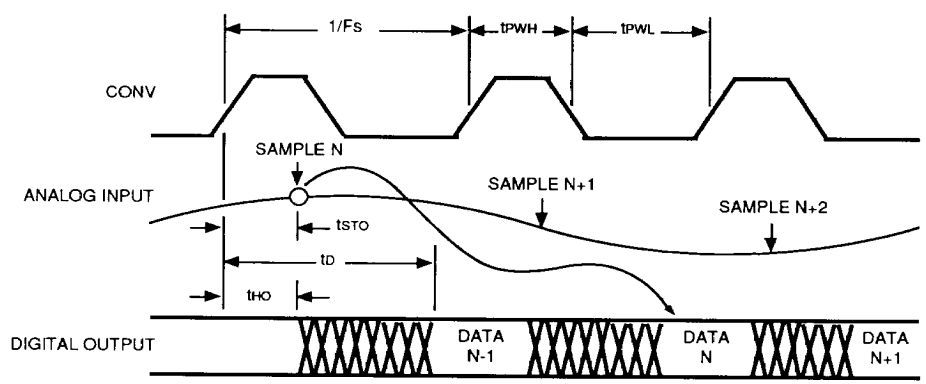

Figure 2. Timing Diagram

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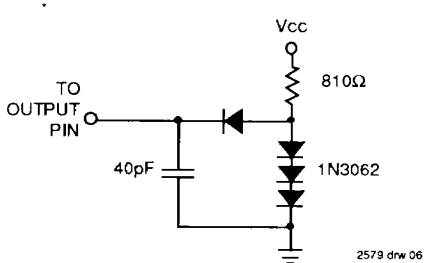

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Figure 3. Output Load 1

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
Power Supply			
V_{CC}	Measured to D_{GND}	−0.5 to +7.0	V
V_{EE}	Measured to A_{GND}	+0.5 to −7.0	V
A_{GND}	Measured to D_{GND}	−0.5 to +0.5	V
Input Voltage			
CONV, NMINV, NLINV	Measured to D_{GND}	−0.5 to V_{CC} +0.5	V
V_{IN}, V_{RT}, V_{RB}	Measured to A_{GND}	V_{CC} to V_{EE}	V
V_{RT}	Measured to V_{RB}	−4.0 to +4.0	V
Output			
Applied Voltage (2)	Measured to D_{GND}	−0.5 to V_{CC} +0.5	V
Applied Current (2, 3, 4)	Externally forced	−20.0 to +20.0	mA
Short Circuit Duration	Single output High to D_{GND}	1.0	S
Temperature			
Operating Ambient	Military	−55 to +125	°C
	Commercial	0 to +70	°C
Storage	Military	−65 to +150	°C
	Commercial	−55 to +125	°C

2579 tbl 01

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Absolute Maximum Ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current when flowing into the device.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Temperature Range						Unit
			Commercial			Military			
			Min.	Nom.	Max.	Min.	Nom.	Max.	
Power Supply									
V_{CC}	Positive Power Supply		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Power Supply		–4.9	–5.2	–5.5	–4.9	–5.2	–5.5	V
V_{AGND}	Analog Ground Voltage (ref D_{GND})		–0.1	0	+0.1	–0.1	0	+0.1	V
I_{CC}	Positive Supply Current	V_{CC} = Max., Static[1]	—	50	70	—	60	80	mA
I_{EE}	Negative Supply Current	V_{EE} = Max., Static[1]	—	–25	–35	—	–25	–35	mA
Digital Inputs (CONV, NMINV, NLINV)									
V_{IL}	Input Voltage, Logic LOW[4]		–0.5	—	0.8	–0.5	—	0.8	V
V_{IH}	Input Voltage, Logic HIGH[4]		2.0	—	V_{CC} +.1	2.0	—	V_{CC} +.1	V
I_{IL}	Input Current, Logic LOW	V_{CC} = Max., V_{IL} = 0.5V	—	—	±10	—	—	±10	µA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max., V_{IH} = 2.4V	—	—	±10	—	—	±10	µA
I_I	Input Current, Max. Input Voltage	V_{CC} = Max., V_I = V_{CC}	—	—	50	—	—	50	µA
C_I	Digital Input Capacitance[4]	T_A = +25°C, F = 1MHz	—	—	15	—	—	15	pF
Digital Outputs									
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min., I_{OL} = 4.0mA	—	—	0.5	—	—	0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min., I_{OH} = 4.0mA	2.4	—	—	2.4	—	—	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max.[2]	—	—	–50	—	—	–50	mA
Reference									
V_{RT}	Most Positive Reference Voltage[3]		–0.1	0	+0.1	–0.1	0	+0.1	V
V_{RB}	Most Negative Reference Voltage[3]		–1.9	–2.0	–2.1	–1.9	–2.0	–2.1	V
V_{RT}–V_{RB}	Reference Voltage Range		1.8	2.0	2.2	1.8	2.0	2.2	V
I_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	—	5	9	—	6	10	mA
R_{REF}	Reference Current (R_T to R_B)	V_{RT}, V_{RB} = Nom.	250	400	—	200	330	—	Ohm
Analog Input									
V_{IN}	Input Voltage Range		V_{RB}	—	V_{RT}	V_{RB}	—	V_{RT}	V
R_{IN}	Equiv. Input Resistance[4]	V_{RT}, V_{RB}= Nom., V_{IN} = V_{RB}	100	—	—	100	—	—	KOhm
C_{IN}	Equiv. Input Capacitance[4]	V_{RT}, V_{RB}= Nom., V_{IN} = V_{RB}	—	—	50	—	—	50	pF
I_{CB}	Input Const. Bias Current	V_{EE} = Max.	—	—	10	—	—	10	µA
T_A	Ambient Temperature, Still Air		0	—	70	—	—	—	°C
T_C	Case Temperature		—	—	—	–55	—	+125	°C

NOTES:
2579 tbl 02

1. Worst case, all digital inputs and outputs LOW.
2. Output HIGH, one pin to ground, one second duration.
3. V_{RT} must be more positive than V_{RB} and the voltage reference must be within the specified range. Although the device is specified and tested with the reference equal to 0V and –2V, the part will operate with V_{RT} up to +2.1V. Likewise, the reference range may vary from 1.2V to 2.6V.
4. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C48SX20 (20MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

Symbol	Parameter	Test Conditions	Temperature Range						Unit
			Commercial			Military			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
F_S	Conversion Rate	V_{CC} = Min., V_{EE} = Min.	20	30	—	20	30	—	MSPS
t_{PWL}	CONV, Pulse Width LOW[3]		18	—	100,000	18	—	100,000	ns
t_{PWH}	CONV, Pulse Width HIGH[3]		22	—	20,000	22	—	20,000	ns
t_{STO}	Sampling Time Offset	V_{CC} = Min., V_{EE} = Min.	0	—	10	0	—	15	ns
E_{AP}	Aperture Error[4]		—	—	60	—	—	60	ps
t_D	Digital Output Delay	V_{CC} = Min., V_{EE} = Min., Load 1	—	—	30	—	—	35	ns
t_{HO}	Digital Output Hold Time	V_{CC} = Min., V_{EE} = Min., Load 1	5	—	—	5	—	—	ns
E_{LI}	Linearity Error, Integral	V_{RT}, 1/2 LSB[2]	—	—	0.2	—	—	0.2	%FS
		V_{RB} = Nom. 3/4 LSB[2]	—	—	0.3	—	—	0.3	%FS
E_{LD}	Linearity Error, Differential	V_{RT}, V_{RB} = Nom.	—	—	0.2	—	—	0.2	%FS
CS	Code Size[1]		25	100	175	25	100	175	%Nom
E_{OT}	Offset Error, Top	V_{IN} = midpoint code 0	—	10	45	—	10	45	mV
E_{OB}	Offset Error, Bottom	V_{IN} = midpoint code 255	—	−10	−30	—	−10	−30	mV
T_{CO}	Offset Error, Temperature Coefficient[4]	V_{IN} = V_{RB}	—	—	±20	—	—	±20	µV/°C
BW	Bandwidth, Full Power Input		7	12	—	5	10	—	MHz
T_{TR}	Transient Response, Full Scale[5]		—	—	20	—	—	20	nS
SNR	Signal to Noise Ratio	20 MSPS Conversion Rate, 10 MHz Bandwidth							
	Peak Signal/RMS Noise	1.248 MHz Input	54	56	—	53	55	—	dB
		2.438 MHz Input	53	56	—	52	55	—	dB
	RMS Signal/RMS Noise	1.248 MHz Input	45	47	—	44	46	—	dB
		2.438 MHz Input	44	47	—	43	46	—	dB
NPR	Noise Power Ratio	DC to 8 MHz White Noise Bandwidth 4 Sigma Loading 1.248 MHz Slot 20 MSPS Conversion Rate	36.5	39	—	36.5	39	—	dB
DP	Differential Phase Error	F_S = 4 x NTSC	—	.5	1	—	.5	1	Degree
DG	Differential Gain Error	F_S = 4 x NTSC	—	1	2	—	1	2	%

2579 tbl 03

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
3. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
4. This parameter is guaranteed but not tested in production.

AC ELECTRICAL CHARACTERISTICS FOR IDT75C48SX30 (30MHz Version)

Specifications over the DC Electrical range unless otherwise stated.

Symbol	Parameter	Test Conditions	Temperature Range						Unit
			Commercial			Military			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FS	Conversion Rate	VCC = Min., VEE = Min.	30	40	—	30	40	—	MSPS
tPWL	CONV, Pulse Width LOW		14	—	100,000	14	—	100,000	ns
tPWH	CONV, Pulse Width HIGH		14	—	20,000	14	—	20,000	ns
tSTO	Sampling Time Offset	VCC = Min., VEE = Min.	0	—	10	0	—	15	ns
EAP	Aperture Error[4]		—	—	60	—	—	60	ps
tD	Digital Output Delay	VCC = Min., VEE = Min., Load 1	—	—	25	—	—	28	ns
tHO	Digital Output Hold Time	VCC = Min., VEE = Min., Load 1	5	—	—	5	—	—	ns
ELI	Linearity Error, Integral	VRT, 3/4 LSB[2]	—	—	0.3	—	—	0.3	%FS
		VRB = Nom. 1 LSB[2]	—	—	0.4	—	—	0.4	%FS
ELD	Linearity Error, Differential	VRT, VRB = Nom.	—	—	0.2	—	—	0.2	%FS
CS	Code Size[1]		25	100	175	25	100	175	%Nom
EOT	Offset Error, Top	VIN = midpoint code 0	—	10	45	—	10	45	mV
EOB	Offset Error, Bottom	VIN = midpoint code 255	—	–10	–30	—	–10	–30	mV
TCO	Offset Error, Temperature Coefficient[4]	VIN = VRB	—	—	±20	—	—	±20	µV/°C
BW	Bandwidth, Full Power Input		10	13	—	8	10	—	MHz
TTR	Transient Response, Full Scale[4]		—	—	20	—	—	20	nS
SNR	Signal to Noise Ratio	30 MSPS Conversion Rate, 15 MHz Bandwidth							
	Peak Signal/RMS Noise	5 MHz Input	44	48	—	44	48	—	dB
		10 MHz Input	44	48	—	44	48	—	dB
	RMS Signal/RMS Noise	5 MHz Input	35	39	—	35	39	—	dB
		10 MHz Input	35	39	—	35	39	—	dB
NPR	Noise Power Ratio	DC to 15 MHz White Noise Bandwidth 4 Sigma Loading 5 MHz Slot 30 MSPS Conversion Rate	—	—	—	—	—	—	dB
DP	Differential Phase Error	Fs = 4 x NTSC	—	.5	1	—	.5	1	Degree
DG	Differential Gain Error	Fs = 4 x NTSC	—	1	2	—	1	2	%

NOTES:

1. Guarantees no missing codes.
2. See the ordering information section regarding the part number designation.
4. No damage to the part will occur if the Max. times are exceeded. See the Convert section for more information about the Conv Max. time limitations.
5. This parameter is guaranteed but not tested in production.

2579 tbl 04

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CALIBRATION

The calibration of the IDT75C58 involves the setting of the 1st and 255th comparator thresholds to the desired voltages. This is done be varying the top and bottom voltages on the reference resistor chain, V_{RT} and V_{RB}, to compensate for any internal offsets. Assuming a nominal 0V to –2V reference range, apply –0.0039V (1/2 LSB from 0V) to the analog input, continuously strobe the device and adjust V_{RT} until the OVFL output toggles between 0 and 1. To adjust the first comparator, apply –1.996V (1/2 LSB from –2V) to the analog input and adjust V_{RB} until the converter output toggles between the codes 0 and 1.

The offset errors are caused by the parasitic resistance between the package pins and the actual resistor chain on-chip and are shown as R1 and R2 in the Functional Block Diagram. The offset errors, E_{OT} and E_{OB}, are specified in the AC Electrical Characteristics and indicate the degree of adjustment needed.

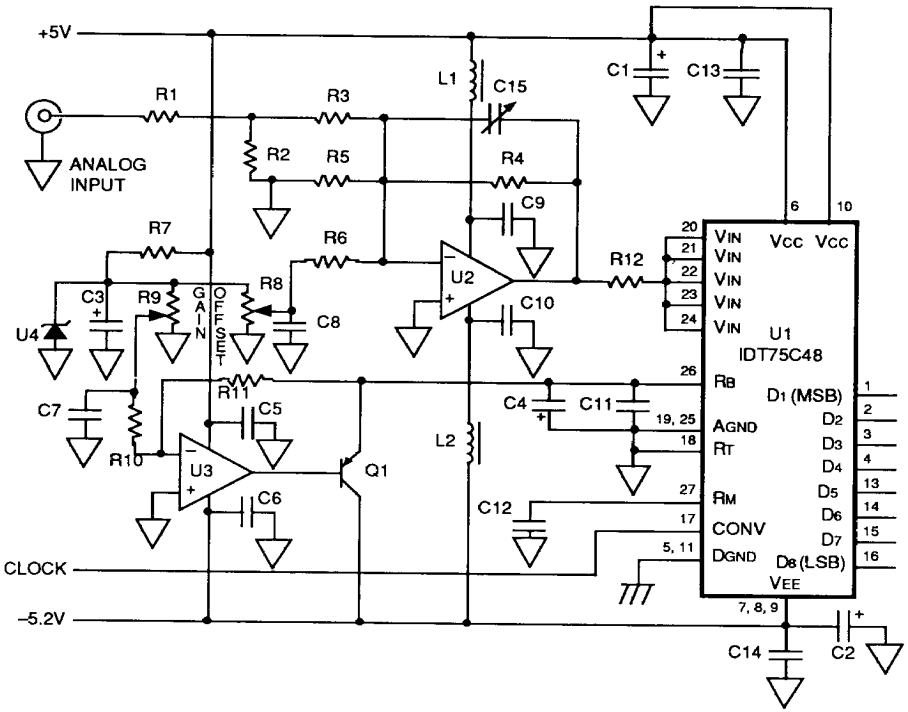
The previously described calibration scheme requires that both ends of the reference resistor chain be adjustable, i.e. be driven by operational amplifiers. A simpler method is to connect the top of the resistor chain, R_T, to analog ground or 0V and to adjust this end of the range with the input buffer offset control. The offset error at the bottom of the resistor chain results in a slight gain error which can be compensated for by varying the voltage applied to R_B. This is a preferred method for gain adjustment since it is not the input signal path. See Figure 5 for a detailed circuit diagram of this method.

TYPICAL INTERFACE

Figure 5 shows a typical application example for the IDT75C58. The analog input amplifier is a bipolar wideband operational amplifier whose low impedance output directly drives the A/D Converter. The input buffer amplifier is configured with a gain of minus two which will convert a standard video input signal (1V p–p) to the recommended 2V converter input range. Both V_{IN} pins are connected together as close to the package as possible and the input buffer feedback loop is closed at this point. Bipolar inputs, as well as the calibration of the reference top, are accomplished using the offset control. A band-gap reference is used to provide a stable voltage for both the offset and gain control. A variable capacitor in the input buffer feedback loop allows optimization of either the step or the frequency response and may be replaced by a fixed value in the final version of the printed circuit board.

To ensure operation to the rated specifications, proper decoupling is needed. The bypass capacitors should be located close to the chip with the shortest lead lengths possible. Massive ground planes are recommended. If separate digital and ground planes are used, they should be connected together at one point close to the IDT75C58.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier buffered by a PNP transistor. The transistor provides a low impedance source and is necessary to provide the current flowing through the resistor chain. The bottom reference voltage may be adjusted to cancel the gain error introduced by the offset voltage, E_{OB}, as discussed in the calibration section.



PARTS LIST

R1	0.0Ω
R2	80.7Ω
R3	1KΩ
R4	2KΩ
R5	220Ω
R6	2KΩ
R7	1KΩ
R8	2KΩ
R9	2KΩ
R10	10KΩ
R11	20KΩ
R12	27Ω
C1-C4	10µF
C5-C14	0.1µF
C15	1-6pF Variable
U1	IDT75C48
U2	HA-2539-5
U3	uA741C
U4	LM313
Q1	2N2907
L1, L2	Ferrite Bead

Figure 4. Application Example

2579 drw 07

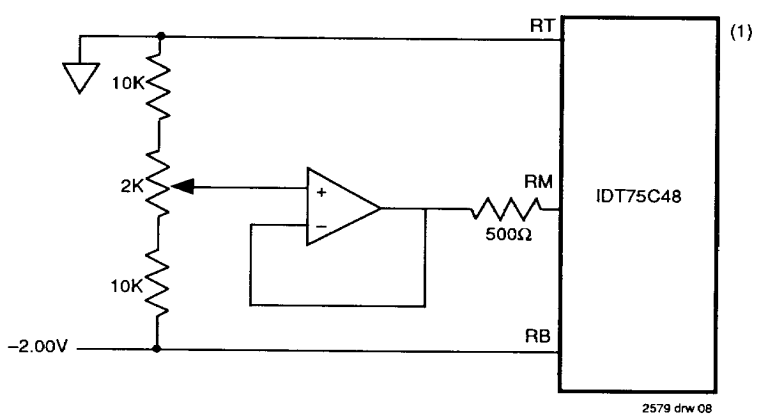


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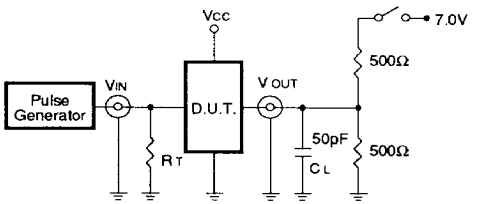
Figure 5. Mid-Point Adjust

NOTE:
1. When NMINV and NLINV are both HIGH a 1KΩ series register must be inserted between NMINV and VCC.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



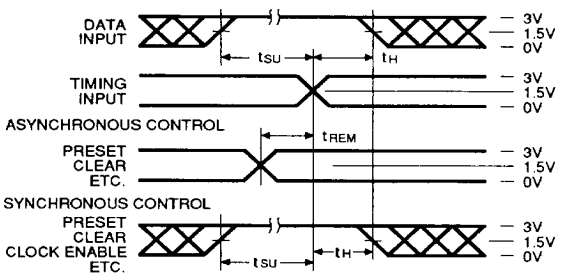
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

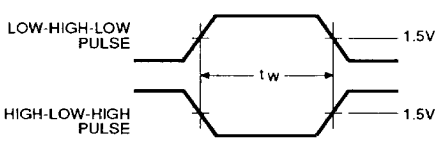
DEFINITIONS: 2578 tbl 6

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

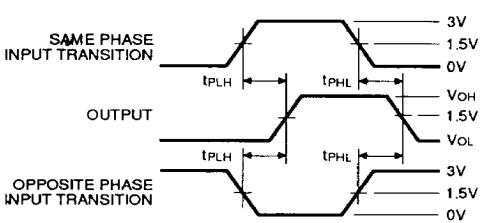
SET-UP, HOLD AND RELEASE TIMES



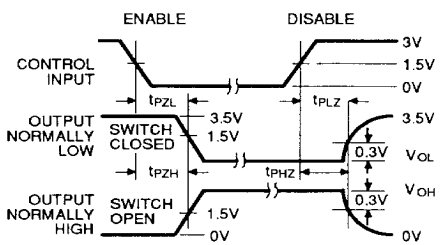
PULSE WIDTH



PROPAGATION DELAY



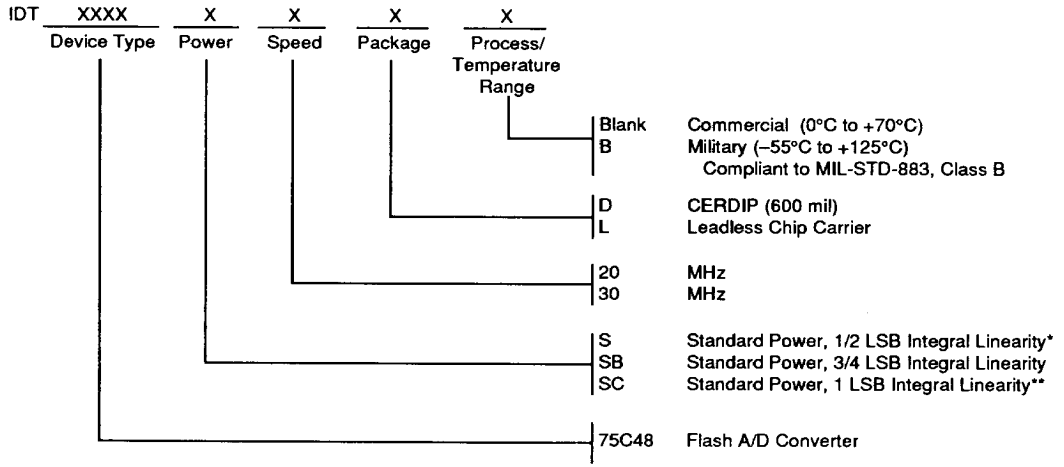
ENABLE AND DISABLE TIMES



NOTES 2578 drw 12

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Zo ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



2579 drw 09

* 20 MHz Version only
** 30 MHz Version only

5