L64815
Memory Management, Cache Control and Cache Tags Unit (MCT)
Preliminary

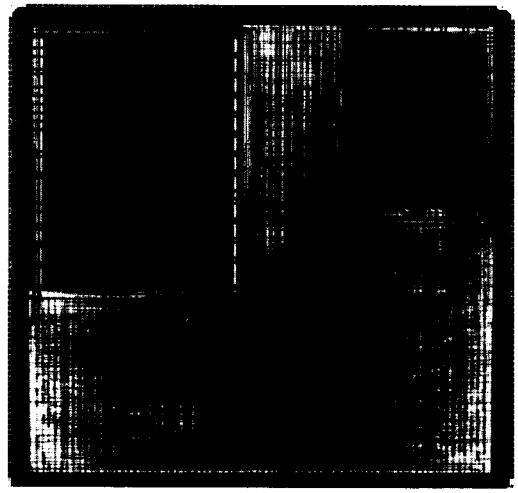
LSI LOGIC

Description

The L64815 Memory Management, Cache Control, and Cache Tags Unit (MCT) provides two essential functions for SPARC (Scalable Processor ARChitecture) CPU Cores – memory management and cache control. The MCT's memory management function implements the SPARC Reference Memory Management Unit (MMU). The Cache Controller manages a direct-mapped, combined instruction and data cache. In addition, the MCT provides an interface between the 32-bit Local Bus and the 64-bit Mbus.

The L64815 MCT is made by LSI Logic using 0.7-micron channel length, silicon gate HCMOS technology.

The MCT is a member of LSI Logic's L64811 Chip Family which implements and supports SPARC-based system development of SPARC) chips.



L64815 Die

Features

The memory management unit of the L64815:

- Incorporates a 64-entry, fully associative Translation Lookaside Buffer (TLB)
- Uses Least Recently Used (LRU) replacement algorithm for the TLB
- Uses fixed 4096-byte page size
- Supports three-level page mapping
- Supports sparse address spaces
- Supports large linear mappings
- Supports 256 contexts
- Provides page-level protection
- Performs 32-bit virtual to 36-bit physical address translation

The write-through, no-allocate cache controller of the L64815:

- Provides 2048 virtual address cache tags
- Provides 32-byte block size
- Provides hardware-miss processing
- Includes 32-byte Line Buffer
- Supports cache sizes of 32, 64, 128, and 256 Kbytes
- Supports line-by-line cache freezing

In addition, the L64815:

- Supports 25-, 33-, and 40-MHz operation
- Uses 64-bit Mbus as its main memory interface
- Is available in 223-pin ceramic pin grid array
- Provides Block Fill capability
- Provides Block Copy capability

The MCT in the SPARC CPU Core

The MCT is part of a high-performance, general-purpose, reprogrammable computer based on Sun Microsystems's SPARC. Such a computer requires three main components: a CPU Core, main memory, and an input/output (I/O) subsystem. A SPARC CPU Core consists of the following elements: a SPARC-compatible Integer Unit (IU), a Floating-Point Unit (FPU), a Memory Management Unit (MMU), and a cache. These elements provide data, integer, and floating-point arithmetic processing power and the flexible, fast memory management required to support multiple processes running simultaneously from a large physical memory.

Figure 1. shows the simple primary interface between the IU, FPU, and MCT– the elements of the CPU Core. Note that no intervening logic is required to connect these components.

The MCT in the SPARC CPU Core (Continued)

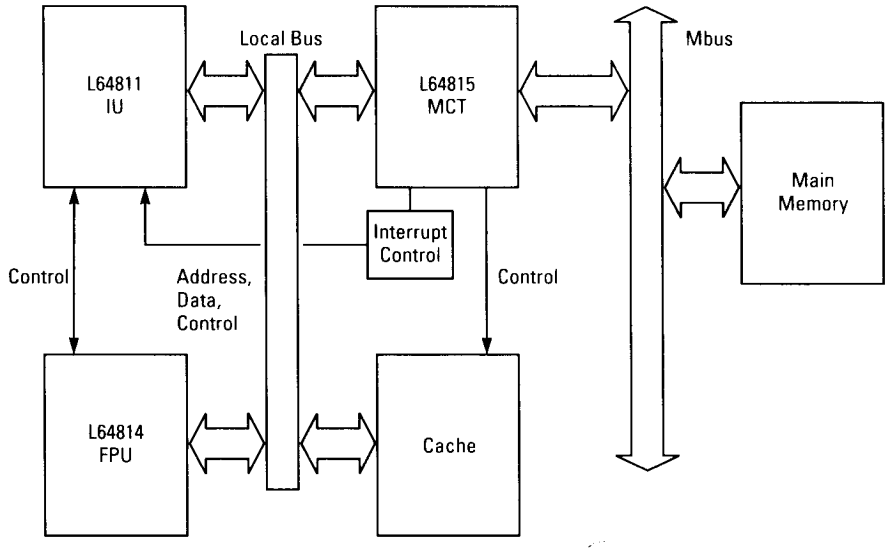


Figure 1. SPARC Standard Architecture Block Diagram

MCT Function

A high-performance, SPARC-based computer requires an efficient memory-management scheme to manage the large physical memories demanded by multitasking operating systems. To feed the IU with one instruction per processor cycle, the CPU Core requires a fast cache memory based on static RAM.

The L64815 MCT provides the logic required to implement both a memory-management scheme and a cache memory.

The MCT – and by extension, the CPU Core – connects to main memory via the Mbus. This multiplexed, 64-bit wide bus connects the CPU Core to the computer's main memory, I/O controllers, and graphic display engine. The Mbus supports multiple masters and provides burst mode data transfers of up to 128 bytes.

The sum of these elements is a balanced, high-performance CPU Core constructed with only three integrated circuits plus static RAM for the cache memory, resulting in a compact and straightforward CPU implementation.

To efficiently support a large number of processes running a wide variety of applications, the MMU portion of the MCT provides three essential services:

- Rapid virtual-to-physical address translation
- Memory access protection
- Page fault indication

The MMU provides **rapid address translation** because it caches translation table entries in a 64-entry, fully associative Translation Lookaside Buffer (TLB). Since translation values are cached and address translation is done in hardware, the physical address is usually transmitted on the main memory bus (Mbus) in the next cycle after the effective address. Once configured, the MMU manages the TLB autonomously, fetching translation entries from tables in main memory whenever an entry required for a particular address translation is not in the TLB.

The MCT also **stores memory access protection masks** in the TLB. If a process attempts to read from or write to a page in memory to which it does not have access, the MMU initiates a memory exception.

If a page is not resident in main memory, the MMU initiates a **page fault exception** to cause the computer's operating system software to determine whether the page is allocated to the process, not mapped, or simply not resident.

MCT Function (Continued)

The L64815's Cache Controller provides the control logic necessary for a high-speed cache memory. The Cache Controller supports static RAM cache memories of 32, 64, 128, or 256 Kbytes. This combined data and instruction cache is able to supply data or instructions to the IU in the same clock cycle as the access – a requirement to maintain the one-instruction-per-cycle pace of the IU. The Cache Controller also supports multitasking efficiently by allowing up to 256 contexts to own lines in the cache.

The Cache Controller's basic function is to keep the cache filled with valid data. The Cache Controller tracks the validity of data in the cache using 2048 cache tags, which are located on the MCT. The cache tags allow the MCT to validate for data for virtual address, context, and access protection. If the Cache Controller finds that the data in cache is invalid for a particular request, it refills the invalid portion of the cache with appropriate data from main memory. The refill process is transparent to the SPARC Integer Unit (IU). The Cache Controller fills the cache in 32-byte increments. This 32-byte line size allows the MCT to use the Mbus burst mode, to provide a high hit rate, and to maximize bus utilization.

The MCT's cache memory is directly mapped to the IU's virtual address space. The MCT uses direct mapping to meet the single-cycle cache memory access time required by the SPARC IU. To allow the MCT to fill the cache without IU help, the Cache Controller uses the MMU to translate virtual to physical addresses for cache fill operations. Clearly, having both the MMU and Cache Control functions on the same chip is a significant benefit.

The Cache Controller uses a write-through, no-allocate technique for managing store operations. To allow store operations to complete as quickly as possible, the MCT updates the cache with the new value, and then writes the data to main memory via the Mbus. Once the MCT has latched the store data, the IU can execute other instructions.

Block Diagram

Figure 2. shows the major functional blocks of the MCT, including the ancillary logic blocks that support the MMU and Cache Controller. The following paragraphs describe each block.

The MMU translates virtual addresses generated by the IU into physical addresses on the Mbus. The MMU has three basic components: the Table-Walking Logic, the Translation Lookaside Buffer (TLB), and the TLB Control Logic.

Table Walking Logic – This block manages the retrieval of translation entries from tables in physical memory, and it performs the actual translation of virtual to physical addresses for Mbus accesses. The Table Walking Logic "walks" a series of linked tables in physical memory to fetch the value needed to translate a particular virtual address into a physical address. Then it completes the address translation by combining the translation value with part of the virtual address.

Translation Lookaside Buffer (TLB) – To speed address translation for subsequent accesses of the same page in main memory, the MMU caches address-translation values in the TLB. The TLB can store and retrieve 64 address-translation values. An address-translation value is tagged with the most significant 20 bits of its virtual address and its context number. For any access of main memory, the fully associative TLB checks the effective memory address against these tags. If the TLB finds a match, the translation entry is delivered to the Table Walking Logic where the physical address is composed. If there is no match, then the Table Walking Logic fetches the required translation value from a set of tables in main memory. The Table Walking Logic uses the retrieved value to generate the physical address for the access, and the TLB replaces the least-recently-used value in the TLB with the new one.

TLB Control – This block contains the diagnostic mechanisms for the TLB, and it controls the TLB Flush and Probe operations.

Block Diagram
(Continued)

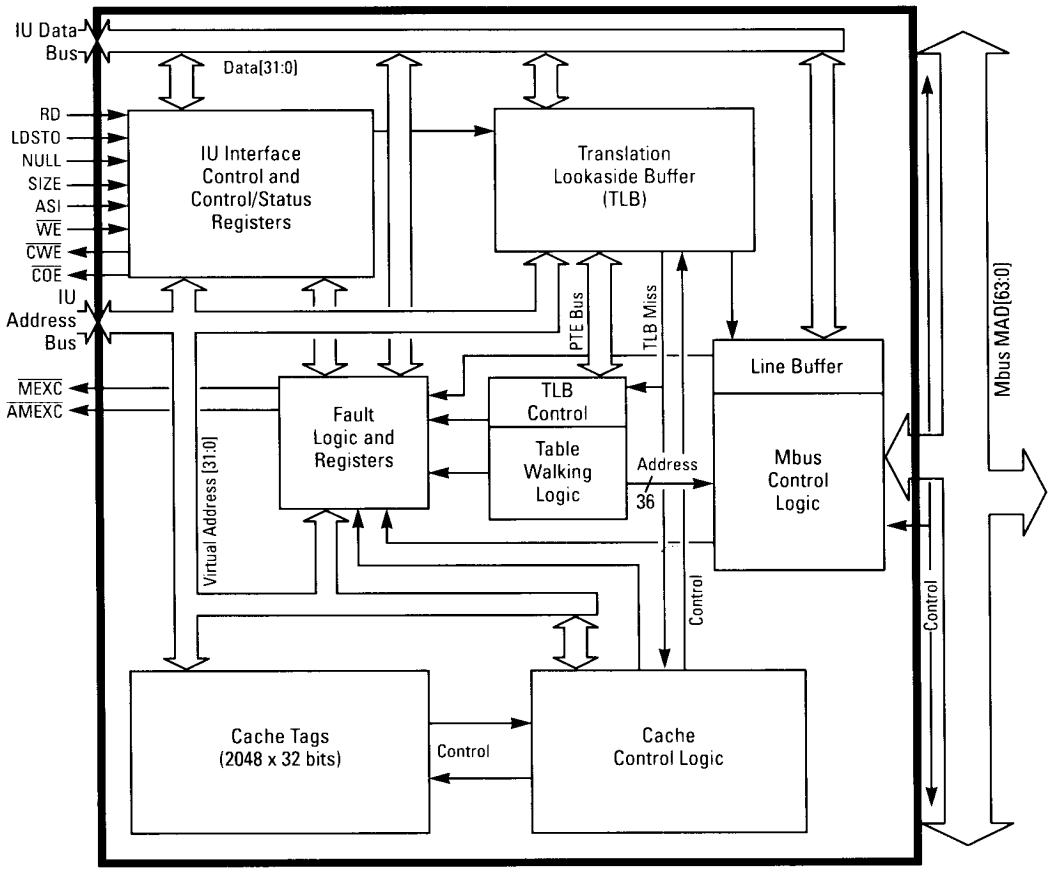


Figure 2. MCT Block Diagram

The **Cache Control** block, comprised of the Cache Tags and the Cache Control Logic, keeps the cache RAM filled with valid data.

Cache Tags – The 2048 Cache Tags store the data that the MCT uses to validate the contents of the 2048-line cache memory. This data includes a valid bit, the 7 to 4 (depending on cache size) most-significant bits of the virtual address, the context number, and access protection codes. The tags are directly indexed by the virtual address associated with an access.

Cache Control Logic – This block contains the compare logic that determines whether the data or instruction required by a particular access is in the cache memory. When the data in the cache is not valid for a particular access (a miss), the IU Interface Control block fills the appropriate cache line with data copied from main memory. During flush operations, the Cache Control Logic also invalidates the cache lines specified by memory management software.

The **IU Interface Control**, the **Fault Logic**, and the **Mbus Control Logic** (including the **Line Buffer**) coordinate and support the MMU and Cache Control blocks. Together, these blocks are called the ancillary logic.

IU Interface Control – This logic block performs two basic functions – it controls the MCT's interface to the IU, and it provides overall MCT control.

As the MCT's IU interface, it decodes Address Space Identifiers (ASIs) and MCT register addresses. The IU Interface Control block contains the Control Register, the Context Table Pointer Register, the Context Register, and the Reset Register, and it controls access to the fault registers located in the **Fault Logic** block.

As the MCT's overall controller, the IU Interface Control block uses the **Line Buffer** to manage write-through operations. It also manages cache fill operations and controls reset sequencing.

Block Diagram (Continued)

Mbus Control Logic – This block manages Mbus transactions for the MCT by sequencing bus control signals and by converting data from the 64-bit Mbus format to the 32-bit datapath formats in the MCT. The MCT can serve only as an Mbus master, not as a slave.

An important part of the Mbus Control Logic is the 32-byte **Line Buffer**, which buffers data for both write and read operations. During writes, the Buffer acts as two independent buffers so that the MCT can fill one buffer while the Mbus Control Logic uses the other as the source for a write transaction on the Mbus. When used for writes, the Buffer can store two doublewords and their associated addresses. During read operations, the Line Buffer buffers data from the high bandwidth Mbus into the MCT's narrower internal bus. This feature is especially important for cache-fill operations because it allows an entire 32-byte cache line to be transferred on the Mbus in a single burst.

Fault Logic –This block monitors faults reported to the MCT by Mbus slaves. It reports faults to the IU by asserting the appropriate memory exception signal and by setting status bits in the fault status registers. It records fault addresses in the fault address registers.

Signal Descriptions: Local Bus Interface

The Local Bus interface connects the MCT with the IU, the FPU, and the static RAM of the cache memory. The 82 Local Bus signals are described in the following paragraphs.

A[31:0]
IU Address [31:0] — A[31:0] comprise the address portion of the bidirectional Local Bus. During store and load operations, the bus master uses these signals to specify the virtual addresses of instructions or data for memory accesses. When the MCT is filling the cache, it uses A[17:0] to specify cache addresses.

ASI[5:0]
Address Space Identifier [5:0] — The IU uses the six ASI bits to specify the address space for an instruction fetch or a data access to memory.

D[31:0]
IU Data Bus [31:0] — D[31:0] comprise the data portion of the bidirectional Local Bus. The MCT samples the bus when the IU or some other entity writes data to the MCT. The MCT drives the bus when loading cache memory.

FNULL
FPU Null — The FPU asserts FNULL to nullify the memory address currently latched by the MCT.

$\overline{\text{IOE}}$
IU Output Enable — The MCT uses $\overline{\text{IOE}}$ to enable and disable the IU's bus drivers.

INULL
IU Null — INULL causes the MCT to ignore the address on A[31:0].

LDSTO
Load/Store Operation — The IU asserts LDSTO during the data cycles of atomic load-store operations to indicate that the current operation is indivisible. The MCT latches this signal at the rising edge of CLK.

$\overline{\text{MDS}}$
Memory Data Strobe — When the MCT has been forced to hold the IU because of a cache miss or access to slow memory, the MCT asserts $\overline{\text{MDS}}$ to indicate that data or instruction is available on D[31:0].

$\overline{\text{AMEXC}}$
Asynchronous Memory Exception — The MCT asserts $\overline{\text{AMEXC}}$ to indicate that it has detected an asynchronous memory exception. By connecting $\overline{\text{AMEXC}}$ to interrupt logic, system designers can use this signal to interrupt the IU.

$\overline{\text{MEXC}}$
Synchronous Memory Exception — The MCT asserts $\overline{\text{MEXC}}$ to initiate a synchronous instruction or data exception trap.

$\overline{\text{MHOLD}}$
Memory Hold — The MCT uses $\overline{\text{MHOLD}}$ to freeze the pipelines of both the IU and FPU during a cache miss (for systems with cache) or during a slow-memory access.

RD
Read — The IU asserts RD to classify the current memory access as a read operation.

SIZE[1:0]
Size [1:0] — These bits comprise the size portion of the Local Bus. The IU uses these two bits to specify to the MCT the size of the current data transfer or instruction fetch.

$\overline{\text{WE}}$
Write Enable — The IU asserts $\overline{\text{WE}}$ to classify the current memory access as a write operation.

Signal Descriptions: Mbus Interface

The Mbus connects the MCT to main memory, expansion bus controllers, and other devices. The MCT is a bus master, never a bus slave.

The MCT's interface to the Mbus consists of 72 signals, which are defined in the following paragraphs.

MAD[63:0]
Memory Address and Data — During the Mbus address phase, MAD contains the physical address, size, type, and other control bits. During the Mbus data phase, MAD contains eight bytes of data.

$\overline{\text{MAS}}$
Memory Address Strobe — The MCT asserts $\overline{\text{MAS}}$ during the first cycle of a bus transaction to identify the cycle as the "address cycle" or "address phase" of the transaction.

$\overline{\text{MBB}}$
Mbus Busy — The current bus master asserts $\overline{\text{MBB}}$ from the beginning to the end of a bus transaction.

$\overline{\text{MBG}}$
Mbus Grant — The Mbus arbiter asserts $\overline{\text{MBG}}$ to grant Mbus mastership to the MCT.

$\overline{\text{MBR}}$
Mbus Request — The MCT asserts $\overline{\text{MBR}}$ to request Mbus ownership.

$\overline{\text{MERR}}$
Mbus Error — The bus slave asserts $\overline{\text{MERR}}$ to indicate that a bus error has occurred.

$\overline{\text{MRDY}}$
Mbus Ready — The bus slave asserts $\overline{\text{MRDY}}$ to indicate that the slave has received or transmitted valid data. When combined with two other signals, $\overline{\text{MRTY}}$ and $\overline{\text{MERR}}$, $\overline{\text{MRDY}}$ conveys additional transaction status.

$\overline{\text{MRTY}}$
Mbus Retry — The bus slave asserts $\overline{\text{MRTY}}$ to indicate that the slave wants the bus master to abort and retry the current transaction.

$\overline{\text{MRST}}$
Mbus Reset — The MCT asserts $\overline{\text{MRST}}$ to initialize all devices residing on the Mbus to a defined state.

Signal Descriptions: Cache Memory Control

Five of the MCT's signals are devoted to managing the static RAMs comprising the cache memory. They are defined below.

$\overline{\text{COE}}$
Cache Output Enable — The MCT asserts this signal to enable data from the cache onto the Local Bus.

$\overline{\text{CWE}}$[3:0]
Cache Write Enable [3:0] — During cache write operations, the MCT asserts one or more of these four signals to strobe data into the appropriate cache segment.

Signal Description: Miscellaneous

The MCT uses the signals described below to control external events or to receive input from external events.

CLK
Clock — This clock signal synchronizes all system operations, including the IU, MCT, FPU, and transactions on the Mbus.

$\overline{\text{ERROR}}$
Error — When the IU asserts $\overline{\text{ERROR}}$, the MCT sets the WD bit in the Reset Register to one and then resets the IU by asserting $\overline{\text{IRST}}$.

The IU asserts $\overline{\text{ERROR}}$ when a trap is encountered while traps are disabled (software disables traps via the ET bit in the PSR). In this situation, the IU saves the PC and nPC registers, sets the TT value in the TBR, enters into an error state, asserts the $\overline{\text{IRST}}$ signal, and halts.

$\overline{\text{IRST}}$
IU Reset — The MCT asserts $\overline{\text{IRST}}$ to reset the IU.

$\overline{\text{PARA}}$
Parametric Test — The $\overline{\text{PARA}}$ output signal is used for factory test only.

$\overline{\text{POR}}$
Power On Reset — External logic asserts $\overline{\text{POR}}$ to indicate a power-on reset condition. $\overline{\text{POR}}$ freezes all of the MCT's logic as long as it is asserted. $\overline{\text{POR}}$ is propagated to the IU as $\overline{\text{IRST}}$.

TEST
Test — When asserted by external logic, the TEST signal reduces the reset periods of the MCT signals $\overline{\text{MRST}}$ and $\overline{\text{IRST}}$ from 1024 to 16 clock cycles.

$\overline{\text{TN}}$
Test 3-State — When asserted, $\overline{\text{TN}}$ causes the impedance of all 3-state pins to become high. This input signal is used for factory test only, and it must be biased high for normal MCT operation.

Electrical Requirements

This section specifies the electrical requirements for the L64815 MCT. Five tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 1.)
- Recommended Operating Conditions (Table 2.)
- Capacitance (Table 3.)
- DC Characteristics (Table 4.)
- Pin Description Summary (Table 5.)

Table 1. Absolute Maximum Ratings

Symbol	Parameter	Limits[1]	Unit
VDD	DC Supply	-0.3 to +7	V
VIN	Input Voltage	-0.3 to VDD +0.3	V
IIN	DC Input Current	±10	mA
TSTG	Storage Temperature Range (Plastic)	-40 to +125	°C

Note:
1. Referenced to VSS

Table 2. Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
VDD	DC Supply	+3 to +6	V
TA	Ambient Temperature	-0 to +70	°C

Table 3. Capacitance

Symbol	Parameter	Condition	Min	Typ	Max	Units
CIN	Input Capacitance	VIN = 5.0 V, TA = 25°C, f = 1 MHz			10	pF
COUT	Output Capacitance	VIN = 5.0 V, TA = 25°C, f = 1 MHz			12	pF
CIO	I/O Bus Capacitance	VIN = 5.0 V, TA = 25°C, f = 1 MHz			15	pF

Electrical Requirements (Continued)

Table 4. DC Characteristics

Symbol	Parameter	Condition[1]	Min	Typ	Max	Units
VIL	Voltage Input LOW				0.8	V
VIH	Voltage Input HIGH		2.0			V
VOH	Voltage Output HIGH	IOH = -4.0 mA	2.4	4.5		V
VOL	Voltage Output LOW	IOL = 4.0 mA		0.2	0.4	V
IIH	Current Input HIGH	VIN = VDD or VSS			10	µA
IIL	Current Input LOW	VIN = VDD or VSS			-10	µA
IOH	Current Output HIGH	VOH = 2.4 V	-2.0			mA
IOL	Current Output LOW	VOL = 0.4 V	8.0			mA
IOZ	Current 3-State Output Leakage	VOH = VDD or VSS	-10	±1	10	µA
IOS	Current Open Short Circuit	VDD = Max, VOH = VDD VDD = Max, VOL = VDD	15 -5	50 -25	130 -100	mA mA
IDD	Quiescent Supply Current	VIN = VDD or VSS			5	mA
ICC	Supply Current	VIN = Max, f = 25 MHz VIN = Max, f = 33 MHz VIN = Max, f = 40 MHz			1.8 2.8 4.5	W W W

Note:
1. Specified at VDD equals 5V ± 5%; ambient temperature over the specified range

Table 5. Pin Description Summary

Mnemonic	Description	Input/Output	Active
A[31:0]	Local Bus Address	3-State bidirectional	
ASI[5:0]	Address Space Identifier	3-State input	
D[31:0]	Local Bus Data	3-State bidirectional	
SIZE[1:0]	Local Bus Size	3-State input	
$\overline{\text{MHOLD}}$	Memory Hold	Output	LOW
$\overline{\text{MDS}}$	Memory Data Strobe	Output	LOW
$\overline{\text{MEXC}}$	Memory Exception	Output	LOW
$\overline{\text{IOE}}$	IU Output Enable	Output	LOW
RD	Read	Input	HIGH
$\overline{\text{WE}}$	Write Enable	Input	LOW
INULL	IU Null	Input	LOW
FNULL	Floating-Point Null	Input	LOW
$\overline{\text{LDSTO}}$	Load/Store	Input	HIGH
MAD[63:0]	Mbus Address and Data	3-State bidirectional	
$\overline{\text{MAS}}$	Mbus Address Strobe	3-State	LOW
$\overline{\text{MRDY}}$	Mbus Ready	3-State	LOW
$\overline{\text{MRTY}}$	Mbus Retry	3-State	LOW
$\overline{\text{MERR}}$	Mbus Error	3-State	LOW
$\overline{\text{MBR}}$	Mbus Request	Output	LOW
$\overline{\text{MBG}}$	Mbus Grant	Input	LOW
$\overline{\text{MBB}}$	Mbus Busy	3-State	LOW
$\overline{\text{MRST}}$	Mbus Reset	3-State	LOW
$\overline{\text{COE}}$	Cache Output Enable	Output	LOW
$\overline{\text{CWE}}$[3:0]	Cache Write Enable [3:0]	Output	LOW
$\overline{\text{IRST}}$	IU Reset	Output	LOW
$\overline{\text{POR}}$	Power On Reset	Input	LOW
$\overline{\text{ERROR}}$	Error	Input	LOW
CLK	Clock	Input	
$\overline{\text{PARA}}$	Parametric Test	Output	LOW
$\overline{\text{TN}}$	Factory Test	Input	LOW
TEST	Test	Input	HIGH

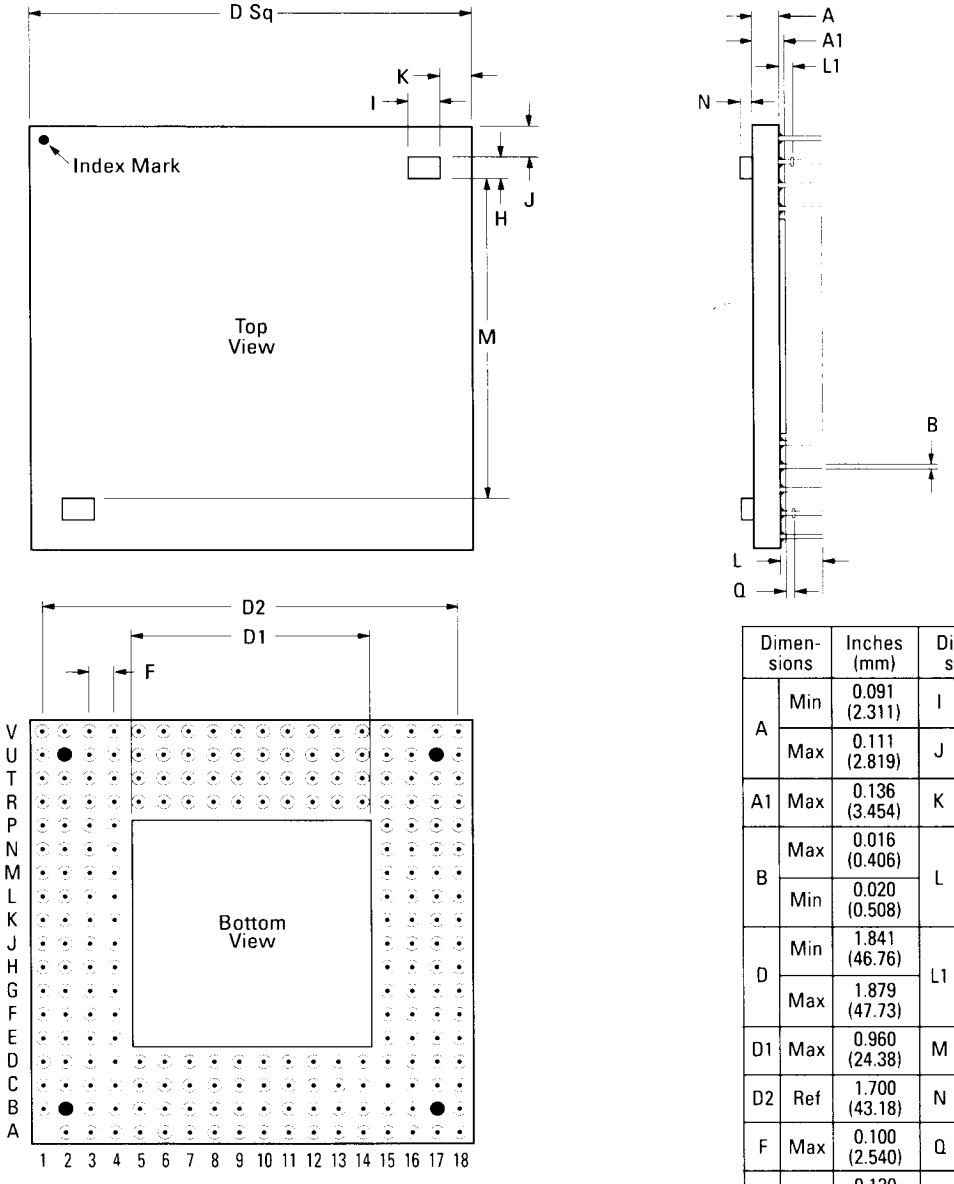
Pinout, Package and Ordering Information

The L64815 is available in a 223-pin Ceramic Pin Grid Array (CPGA) in three speed versions: 25, 33, and 40 MHz.

Table 6 lists the L64815 order numbers by clock frequency. Figures 3 and 4 show the package dimensions and list the pinouts of the 223-pin CPGA.

Table 6. L64815 Order Numbers

Order Number	Clock Frequency	Package Type	Operating Range
L64815GC-25	25 MHz	223 CPGA	Commercial
L64815GC-33	33 MHz	223 CPGA	Commercial
L64815GC-40	40 MHz	223 CPGA	Commercial



Dimensions		Inches (mm)	Dimensions		Inches (mm)
A	Min	0.091 (2.311)	I	Max	0.175 (4.445)
	Max	0.111 (2.819)	J	Ref	0.188 (4.775)
A1	Max	0.136 (3.454)	K	Ref	0.215 (5.461)
B	Max	0.016 (0.406)	L	Min	0.185 (4.699)
	Min	0.020 (0.508)		Max	0.195 (4.953)
D	Min	1.841 (46.76)	L1	Min	0.065 (1.651)
	Max	1.879 (47.73)		Max	0.075 (1.905)
D1	Max	0.960 (24.38)	M	Ref	1.225 (31.12)
D2	Ref	1.700 (43.18)	N	Ref	0.080 (2.032)
F	Max	0.100 (2.540)	Q	Ref	0.040 (1.016)
H	Max	0.130 (3.302)			

Figure 3. 223-pin Pin Grid Array Mechanical Drawing

Pinout, Package and Ordering Information (Continued)

A		VDD	ASI2	POR	WE	IRST	MDS	VSS	VDD	VSS	MRST	MERR	MBB	MAD1	MAD6	MAD10	VDD	VSS
B	VDD	VSS	ASI1	ASI5	SIZE1	FNULL	IOE	AMEXC	CLK	MAS	MBR	MRTY	MAD0	MAD3	MAD7	MAD11	VSS	VDD
C	A2	A1	ASI0	ASI4	ERROR	RD	LDSTO	MHOLD	VSS	MBG	MRDY	VSS	MAD2	MAD4	MAD9	MAD13	MAD14	MAD15
D	A6	A5	A4	A0	ASI3	SIZE0	INULL	VSS	MEXC	VDD	VSS	VSS	MAD5	MAD8	MAD12	MAD17	MAD18	MAD19
E	A11	A9	A8	A3											MAD16	MAD21	MAD23	MAD24
F	VDD	A13	A10	A7											MAD20	VSS	MAD25	MAD27
G	A17	A15	VSS	A12											MAD22	VSS	MAD28	MAD30
H	VSS	A19	A16	A14											VDD	MAD26	MAD31	MAD32
J	VDD	A20	VDD	A18											VDD	MAD29	MAD34	VDD
K	VSS	A21	A23	A25					Top View						VSS	MAD33	MAD35	VSS
L	A22	A24	A27	VDD											MAD37	VDD	MAD36	VDD
M	A26	A28	A30	VSS											VSS	MAD39	VDD	MAD38
N	A29	A31	VSS	D2											MAD42	MAD41	VSS	MAD40
P	D0	D1	D3	D7											MAD48	MAD45	MAD44	MAD43
R	D4	D5	D6	D11	D14	D21	VSS	D26	D28	CWE0	VDD	MAD62	MAD60	MAD56	MAD52	MAD49	MAD47	MAD46
T	D8	D9	D10	D15	D18	VDD	D25	VDD	D30	CWE2	TEST	VSS	VSS	MAD61	MAD57	MAD53	MAD51	MAD50
U	VDD	VSS	D12	D16	D19	D22	D24	D27	VDD	D29	COE	CWE1	TN	MAD63	MAD58	MAD54	VDD	VSS
V	VSS	VDD	D13	D17	D20	D23	VSS	VSS	VDD	VSS	D31	CWE2	VDD	PARA	MAD59	MAD55	VSS	VDD

*Not Connected

MD90 56 rh

Figure 4. 223-pin CPGA Pinout – Top View

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