Chapter 5
Specifications

Functional modules in the L64855 SGC are implemented in 1.5-micron drawn gate length (0.9-micron effective channel length) Channel-Free Array. This chapter defines the electrical parameters of the SGC chip. The descriptions of DC electrical requirements and AC timing are intended for hardware designers who are interested in the compatibility of the SGC with other board level components. The packaging information is intended for printed circuit board designers who are incorporating the SGC in printed circuit board assemblies. The material is presented under three related headings.

- DC Electrical Requirements
- AC Timing Diagrams
- Pinouts and Mechanical

5.1 DC Electrical Requirements

This section specifies the DC electrical requirements for the L64855 SBus Graphics Controller. Four tables list electrical data in the following categories:

- Absolute Maximum Ratings (Table 5.1)
- Recommended Operating Conditions (Table 5.2)
- DC Characteristics (Table 5.3)

Table 5.1 Absolute Maximum Ratings

Symbol[1]	Parameter	Limits[1] Min	Typical	Max	Unit
V_{DD}	DC Supply	-0.3	5	7	V
V_{IN}	Input Voltage	0.3		V_{DD} + 0.3	V
I_{IN}	DC Input Current	-10		+10	mA
T_{STG}	Storage Temperature				
	Ceramic	-65°		+150°	C
	Plastic	-40°		+125°	C

1. Referenced to V_{SS}

Table 5.2 Recommended Operating Ranges

Symbol	Parameter	Range	Unit
V_{DD}	DC Supply	4.75 to 5.75	V
T_A	Ambient Temperature		
	Commercial	0° to +70°	C

The DC characteristics in Table 5.3 are specified at V_{DD} = 5V ± 5%, and ambient temperature over the commercial temperature range which is 0° C to 70° C.

Table 5.3
DC Characteristics

Symbol	*Parameter*	*Condition*	*Min*	*Typ*	*Max*	*Units*
V_{IL}	Voltage Input LOW				0.8	V
V_{IH}	Voltage Input HIGH		2.0			V
V_{OL}	Voltage Output LOW			0.2	0.4	V
V_{OH}	Voltage Output HIGH		2.4	4.5		V
I_{IN}	Input Leakage Current	V_{DD} = 5V, $V = V_{DD}$ or V_{SS}	-10	±1	10	µA
I_{OZ}	Current 3-State Output Leakage	V_{DD} = Max, $V_{out} = V_{DD}$ or V_{SS}	-10	±1	10	µA
I_{OSP1}	P-Channel, Output Short Circuit Current, 1 mA Output Buffer	V_{DD} = Max, V_{out} = 0V	-25		-1	mA
I_{OSP2}	P-Channel, Output Short Circuit Current, 2 mA Output Buffer	V_{DD} = Max, V_{out} = 0V	-50		-2.5	mA
I_{OSP4}	P-Channel, Output Short Circuit Current, 4 mA Output Buffer	V_{DD} = Max, V_{out} = 0V	-100		-5	mA
I_{OSP6}	P-Channel, Output Short Circuit Current, 6 mA Output Buffer	V_{DD} = Max, V_{out} = 0V	-150		-7.5	mA
I_{OSN1}	N-Channel, Output Short Circuit Current, 1 mA Output Buffer	V_{DD} = Max, $V_{out} = V_{DD}$	3.5		33	mA
I_{OSN2}	N-Channel, Output Short Circuit Current, 2 mA Output Buffer	V_{DD} = Max, $V_{out} = V_{DD}$	7.5		65	mA
I_{OSN4}	N-Channel, Output Short Circuit Current, 4 mA Output Buffer	V_{DD} = Max, $V_{out} = V_{DD}$	15		130	mA
I_{OSN6}	N-Channel, Output Short Circuit Current, 6 mA Output Buffer	V_{DD} = Max, $V_{out} = V_{DD}$	22.5		195	mA
C_{IN}	Input Capacitance	Any Input[1]		2		pF
C_{OUT}	Output Capacitance	Any Output[2]		4		pF
I_{DD}	Quiescent Supply Current	V_{DD} = Max, $V_{IN} = V_{DD}$ or V_{SS}			2	mA
I_{CC}	Dynamic Supply Current	V_{DD} = Max			250	mA

1. Not applicable to assigned bidirectional buffer (excluding package).
2. Output using single buffer structure (excluding package).

5.2 AC Timing

This section consists of AC timing diagrams derived from simulation of the L64855 SGC.Figure 5.1 shows test conditions used for AC timing characteristics.

Figure 5.1 AC Test Load and Resulting Waveform Characteristics

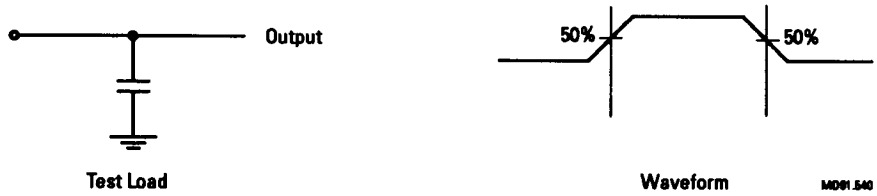


Table 5.4 Capacitive Loading

Signal Name	*Capacitive Load*
$\overline{VCAS}$, $\overline{VDTOE}$, VSC, $\overline{VWE}$, VMA[8:0]	112 pF (14 x 8pF)
$\overline{VAD}$	50 pF
$\overline{ACK}$[2:0], D[31:0], $\overline{IRQ5}$	120 pF
LOAD	32 pF
All other outputs	32 pF

Conventions used in the timing diagram figures include the following:

- Signals that are asserted active LOW are shown with an overbar ($\overline{AS}$).
- Shaded areas in the diagrams indicate an indeterminate state.
- Signals are asserted when they have reached 90% of their active value, whether that is LOW or HIGH. Signals are deasserted when they are within 10% of their unasserted value, whether LOW or HIGH.
- The mnemonic VAD/VDD[7:0] or VAD/VED[7:0] in a diagram denotes all pixel data bus signals: VAD[7:0], VBD[7:0], VCD[7:0], VDD[7:0], and VED[7:0].

Read and Write Timing

The first five timing diagrams are related to reads and writes in single word and burst mode. The timing for a read or a write is related to the SBus clock in terms of writing data from the SBus into VRAM. Once the data is in VRAM, however, it is governed by the video oscillator that generates the RAMDAC clock (DAC_CLKP), video shift clock (VSC) and RAMDAC load (DAC_LD) signals rather than by the SBus clock.

The video data transfer output enable ($\overline{VDTOE}$) signal interfaces between the SBus timing and the RAMDAC clock timing. The SAM is a 512 x 8-bit memory that supplies pixel data to the RAMDAC. The pixels sent to the RAMDAC are tracked by a counter that generates an

interrupt when all 512 have been transferred and the SAM is empty. The counter then generates an internal interrupt that takes priority over reads or writes to VRAM from the SBus side. With the SBus locked out of DRAM, $\overline{\text{VDTOE}}$ is asserted and data is transferred from DRAM to the SAM. DRAM and the SAM are connected only when $\overline{\text{VDTOE}}$ is asserted.

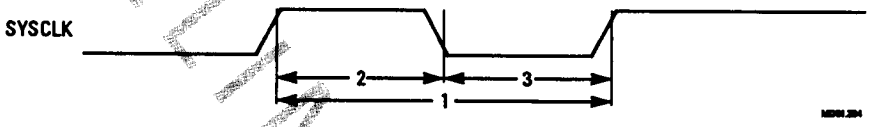
If the counter interrupts during an SBus write to DRAM, the write is allowed to complete before the $\overline{\text{VDTOE}}$ signal is asserted.

During a read or write, only one SBus signal goes to both the SGC and RAMDAC. The READ signal is connected to the SGC RD pin and the RAMDAC R/W pin. All other controller board signals are generated by the SGC from the oscillator or go through the SGC and are converted to control signals for other chips.

In the following timing diagrams, the upper half of the diagram correspond to SBus signals. The lower half correspond to signals generated by the SGC to move data out of VRAM to the RAMDAC.

The clock timing for all timing diagrams is shown in Figure 5.2.

Figure 5.2
CLK Cycle



The numbers in Figure 5.2 and all ensuing figures are defined in Table 5.4 following the last timing diagram.

Figure 5.3
Read Cycle
1152x900, 1024x768

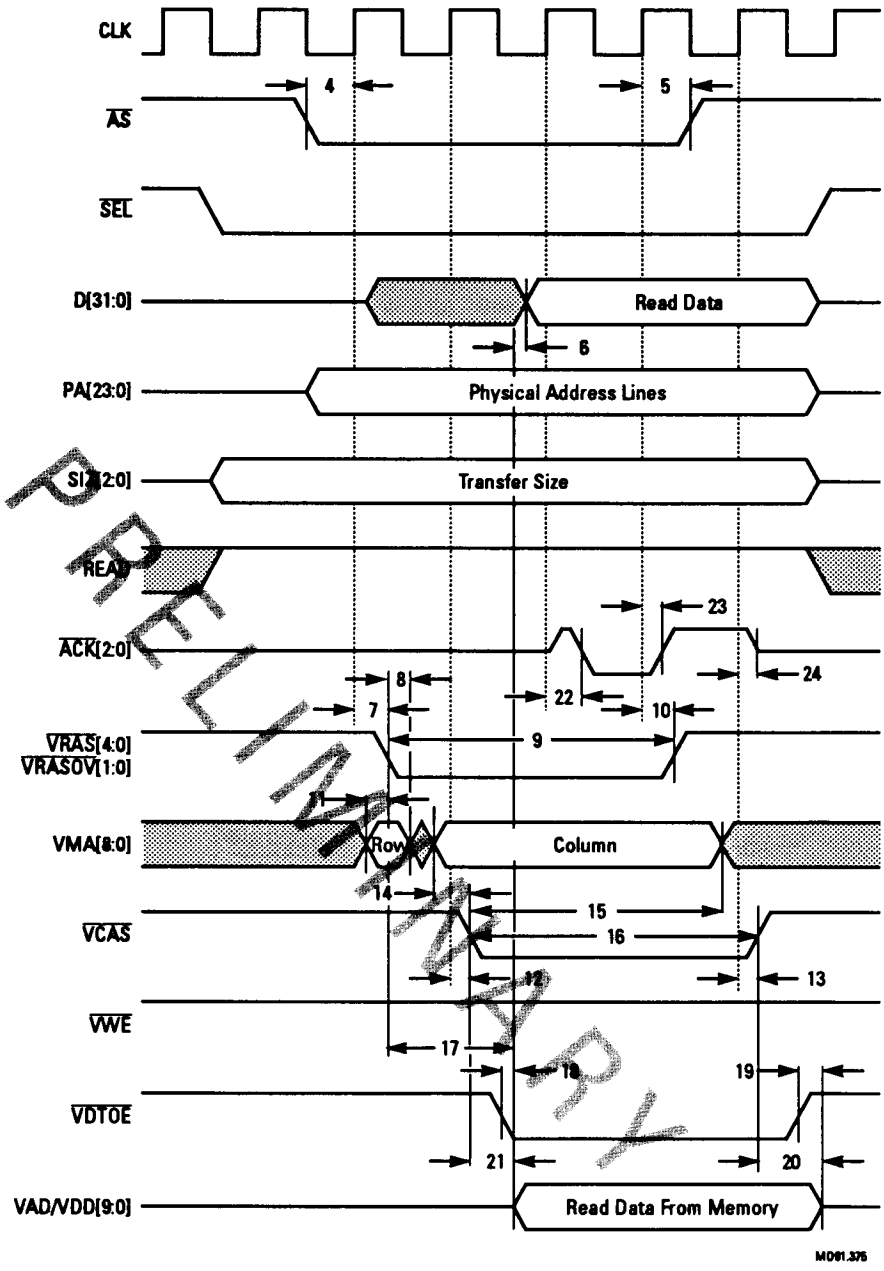


Figure 5.4
Read Cycle
1152x900 1024x768
Burst Mode
(Sheet 1 of 2)

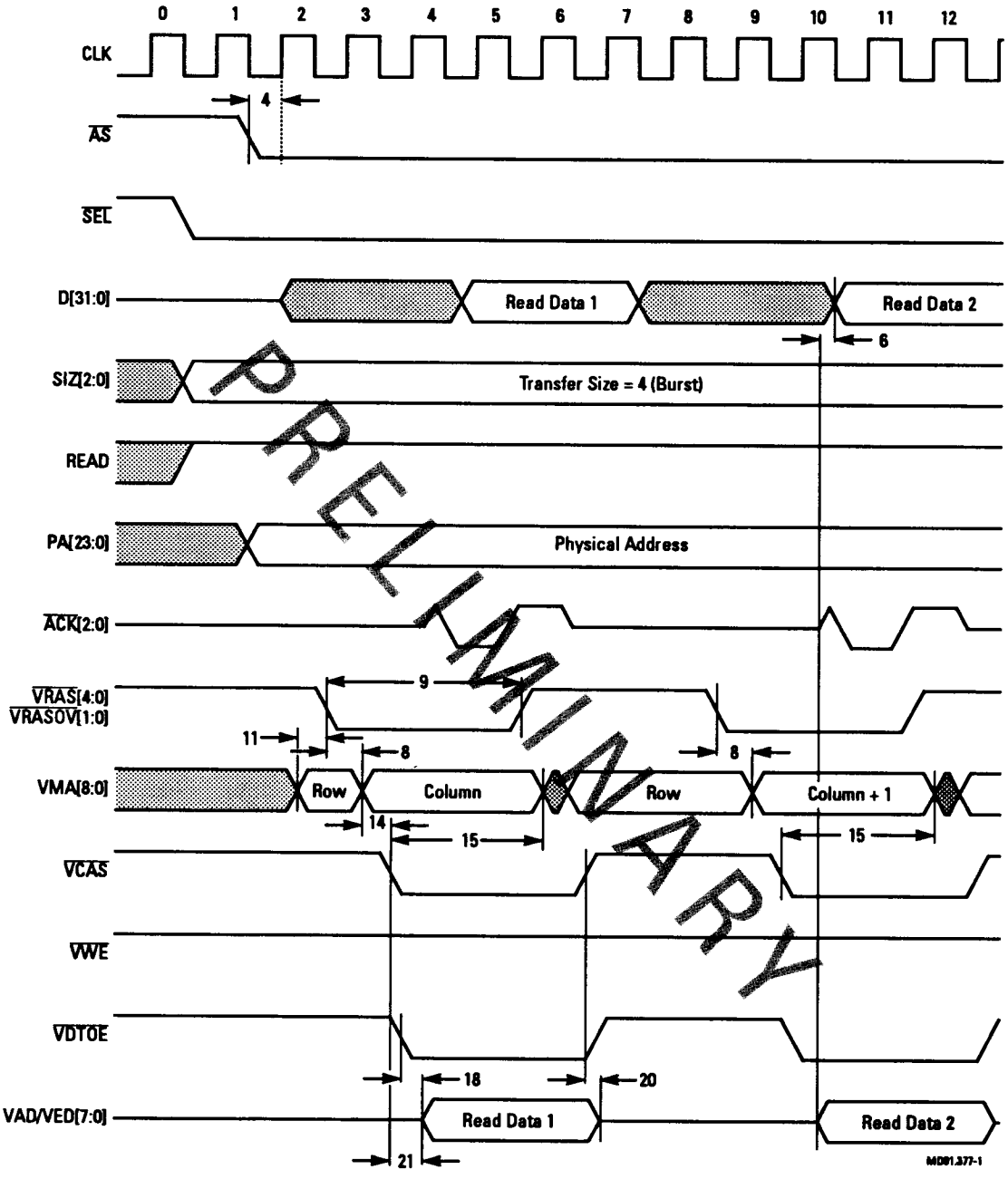


Figure 5.4
Read Cycle
1152x900 1024x768
Burst Mode
(Sheet 2 of 2)

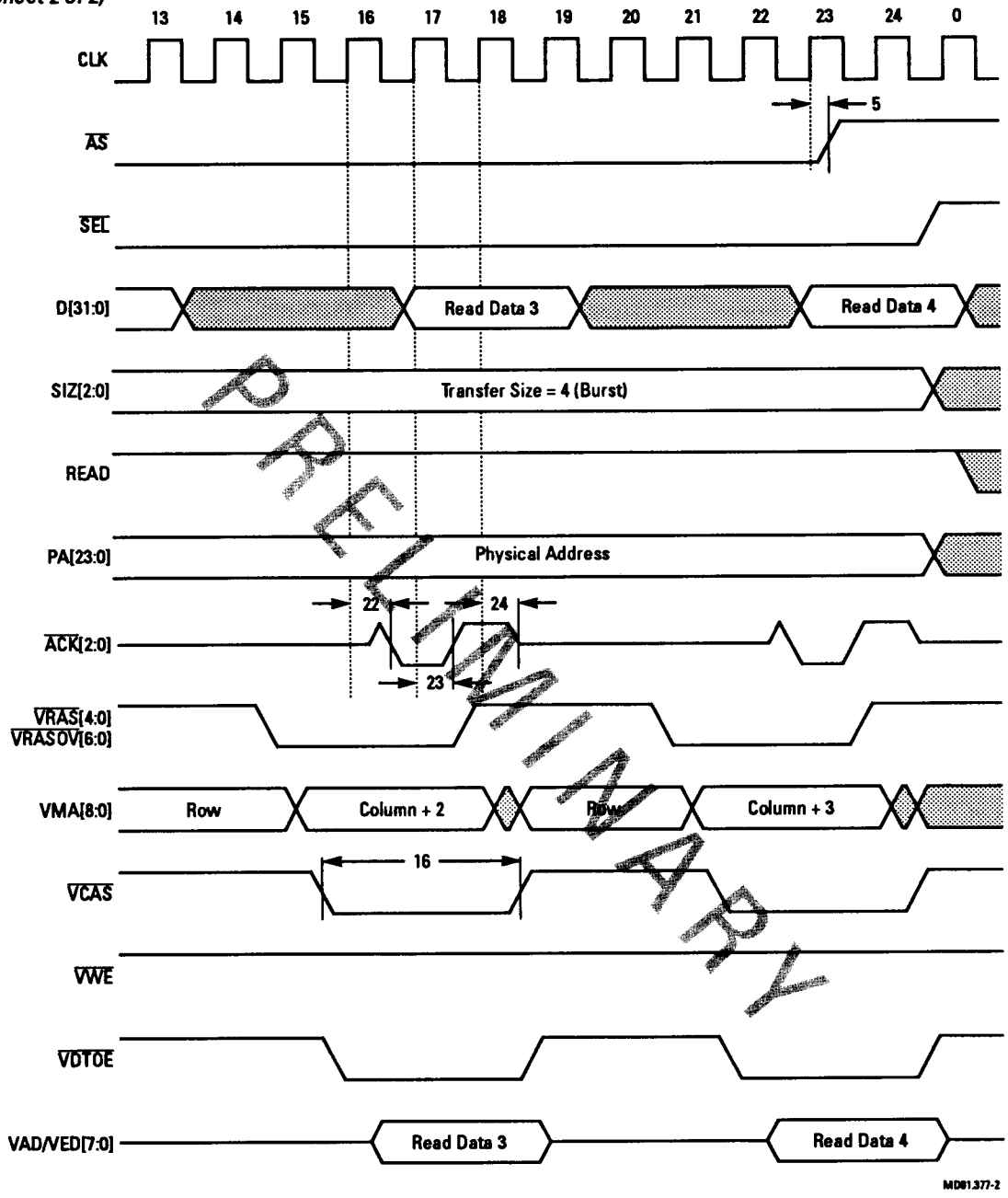


Figure 5.5
Write Cycle
1152x900 1024x768

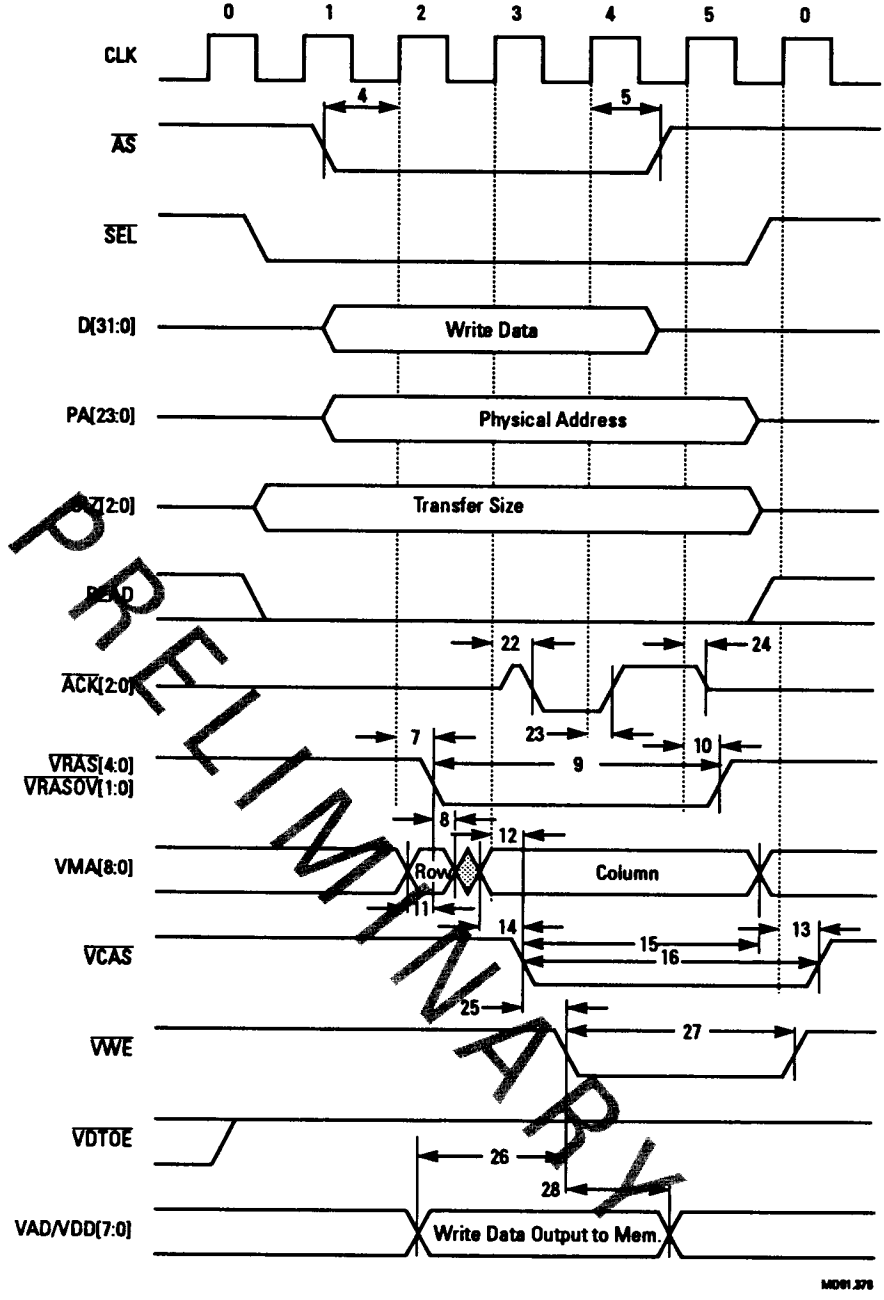


Figure 5.6
Write Cycle
1152x900 1024x768
Burst Mode
(Sheet 1 of 2)

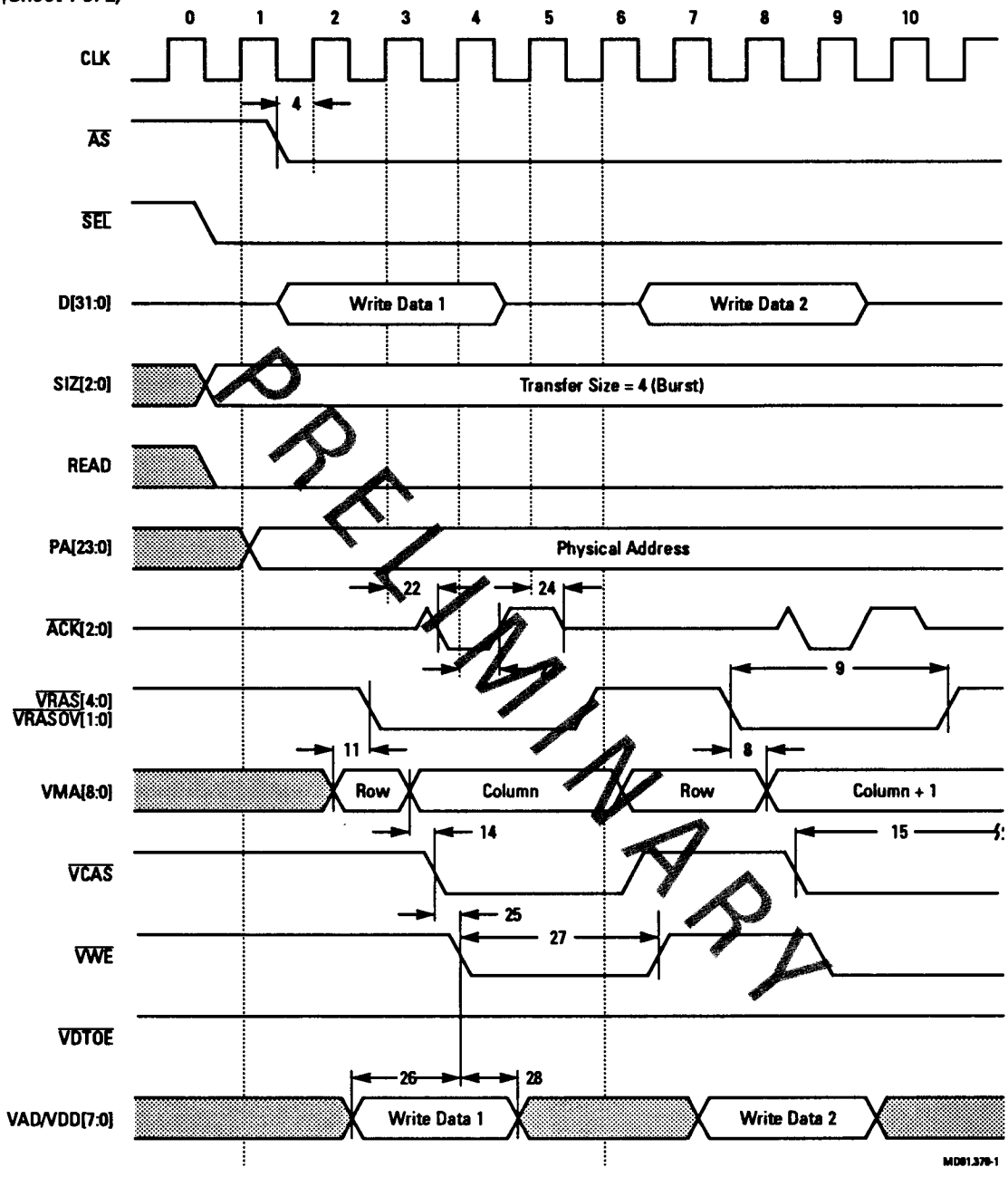


Figure 5.6
Write Cycle
1152x900 1024x768
(Sheet 2 of 2)

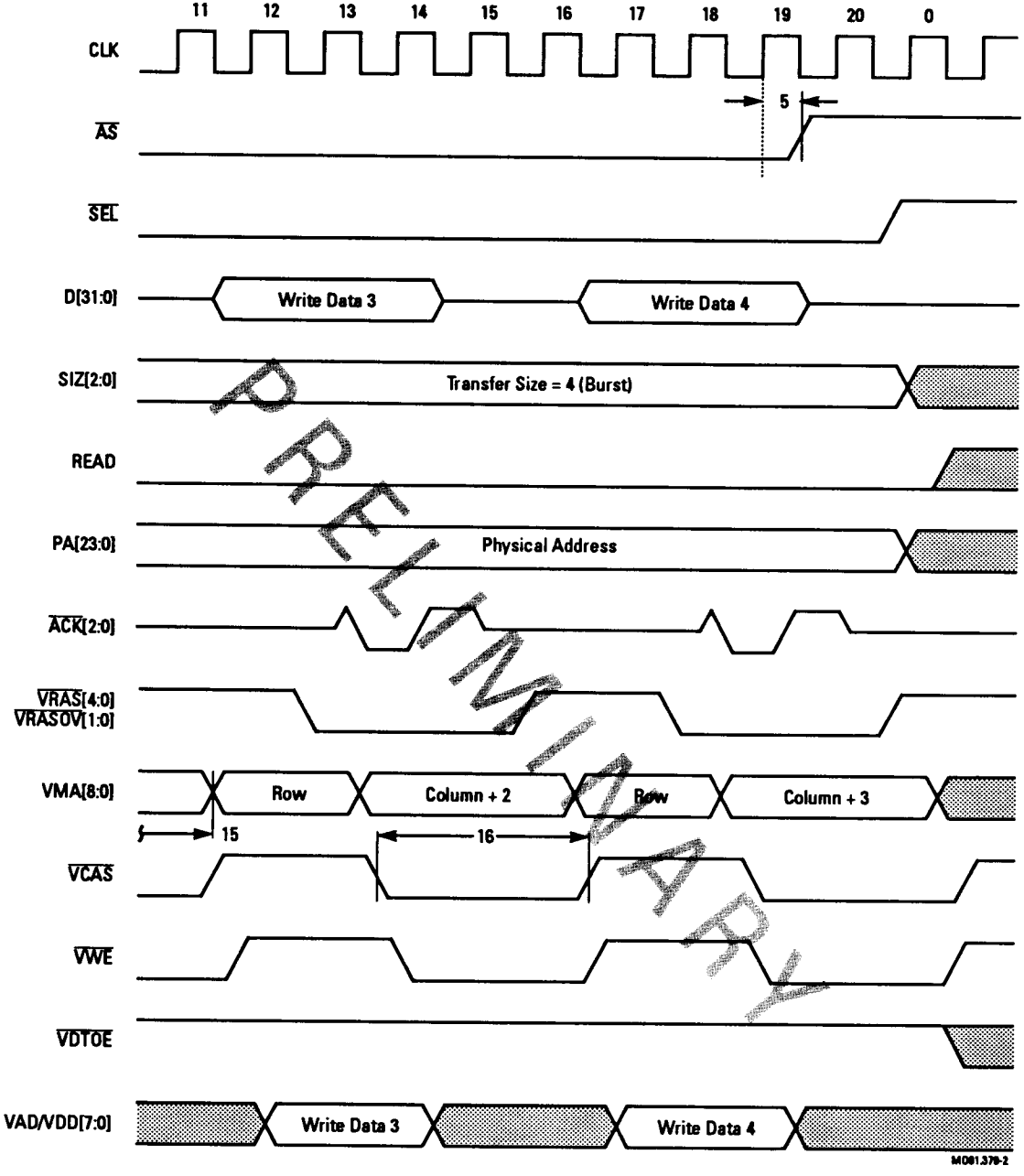
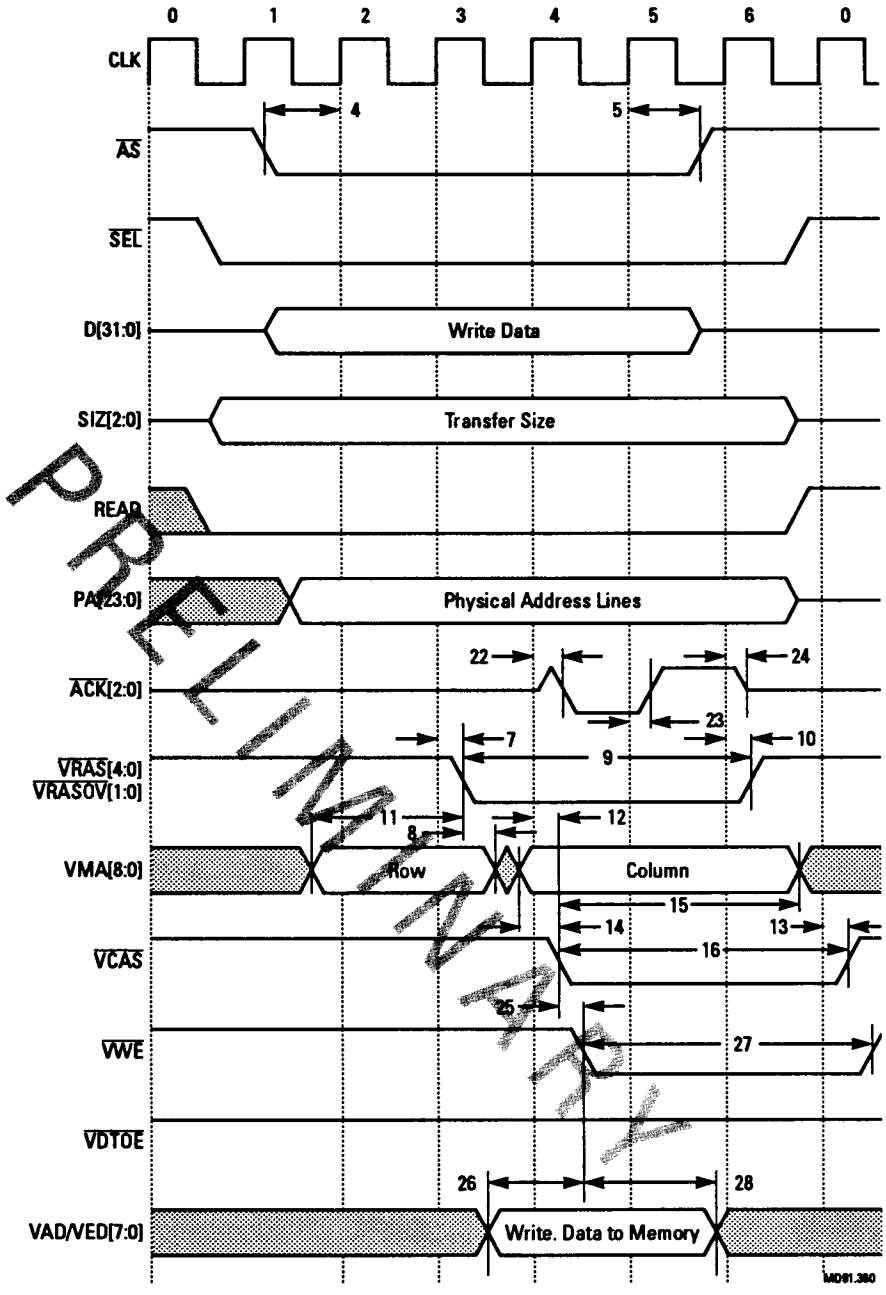


Figure 5.7
Write Cycle
1280x1024



Data Transfer Cycles

The following timing diagram illustrates the data transfer cycle. Unlike the previous read and write cycles, the transfer cycle is governed entirely by the video oscillator, which is converted to the DAC_CLKP signal in the SGC. The DAC_CLKP signal drives the clock input to the RAMDAC chip. By bringing the oscillator signal into the L64855 before using it to drive the RAMDAC both chips are internally synchronized.

Table 5.4 shows the timing values for the L64855 SBus Graphics Controller. The values were determined from simulation at 25MHz.

Figure 5.8
Data Transfer
1024x768 60Hz
(Sheet 1 of 2)

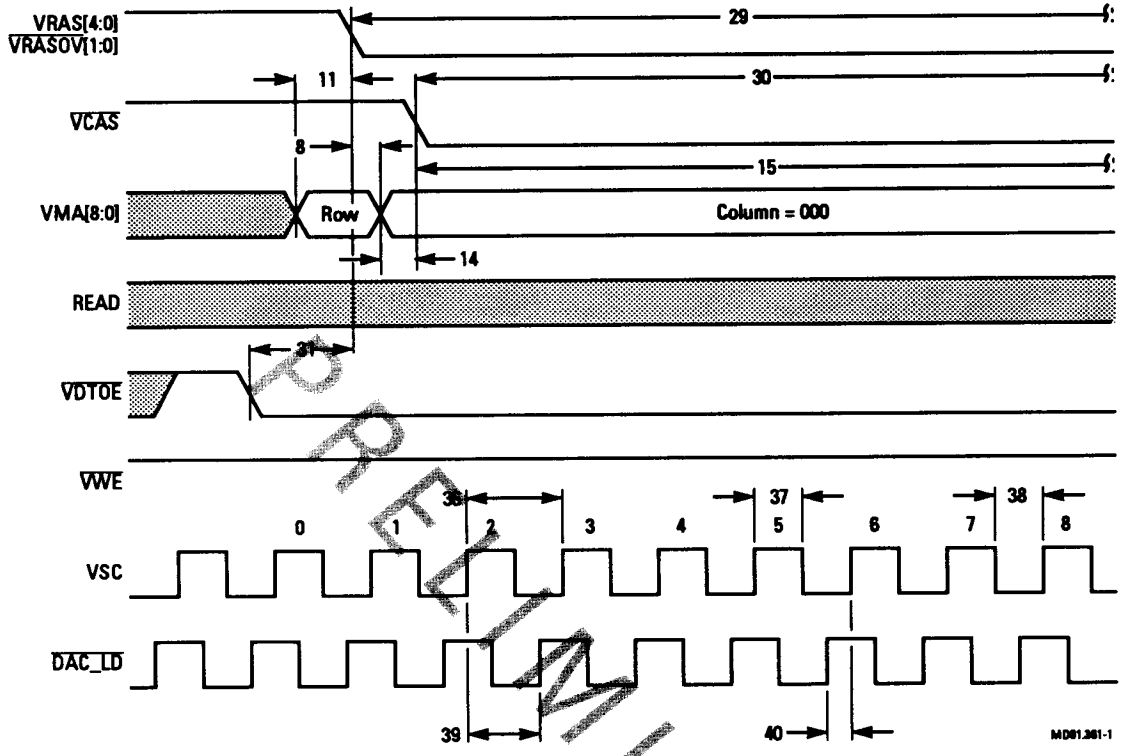


Figure 5.8
Data Transfer
1024x768 60Hz
(Sheet 2 of 2)

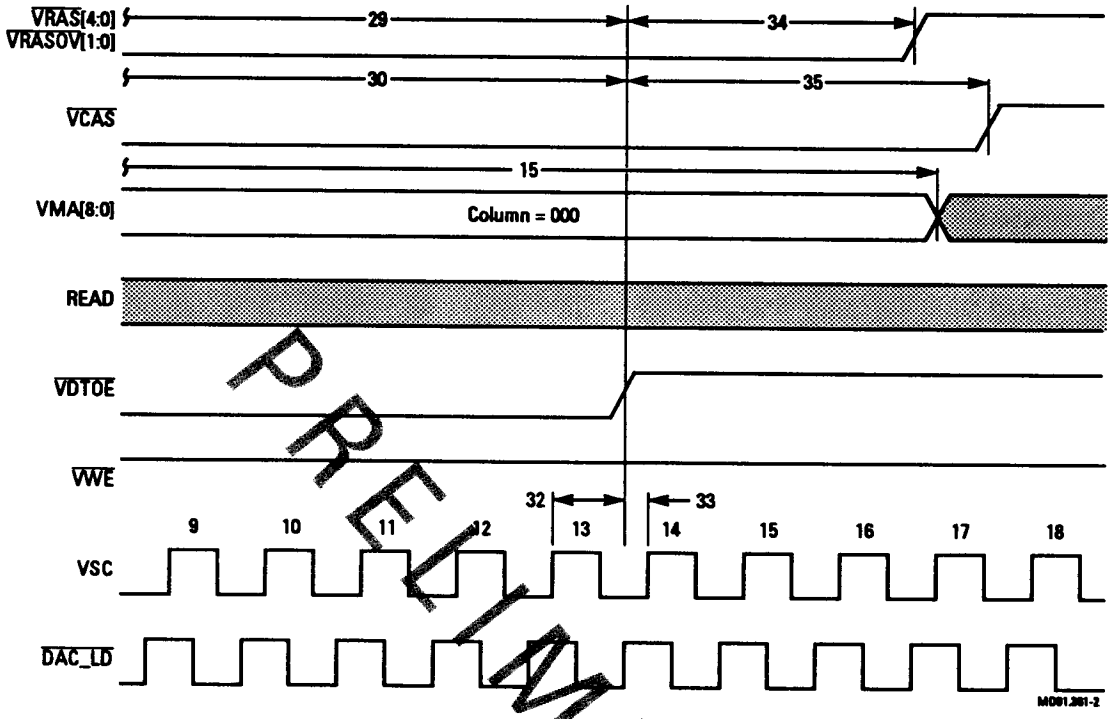


Figure 5.9
Data Transfer
1152x900 66Hz
(Sheet 1 of 2)

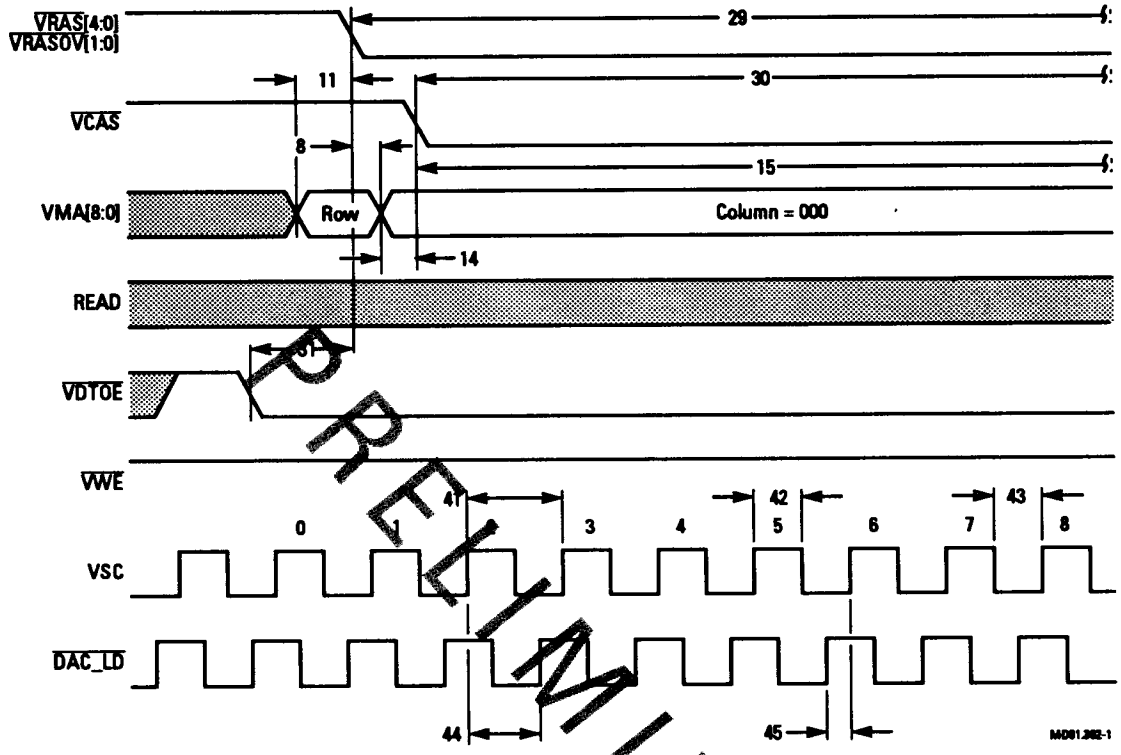


Figure 5.9
Data Transfer
1152x900 66Hz
(Sheet 2 of 2)

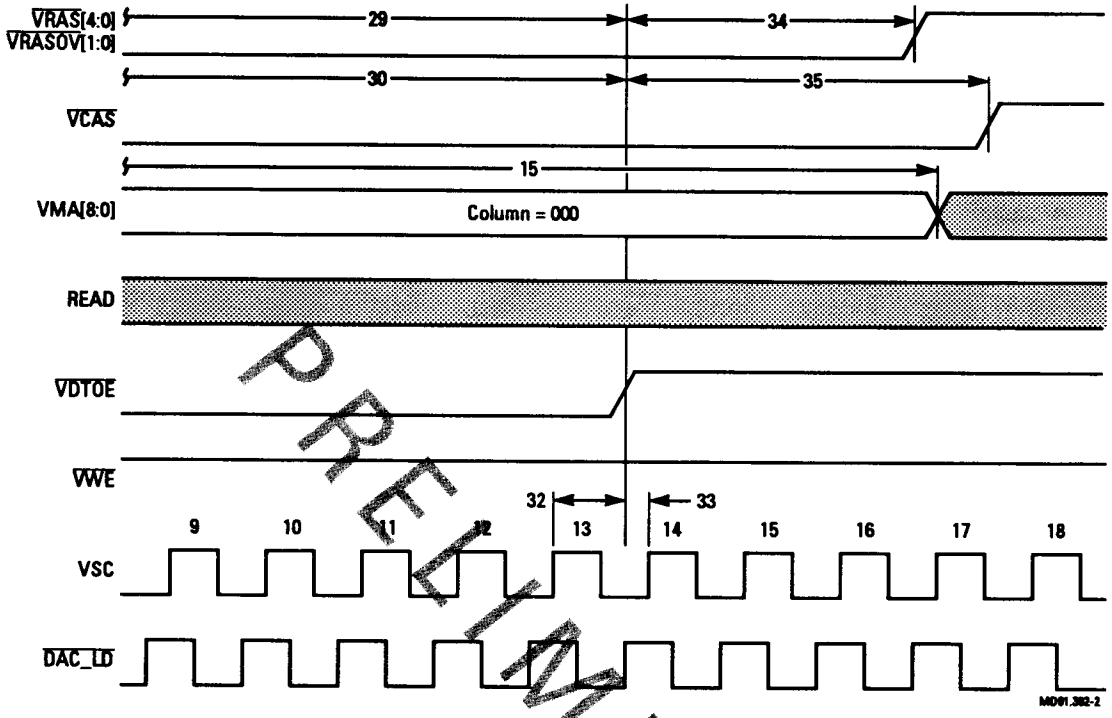


Figure 5.10
Data Transfer
11152x900 76Hz
(Sheet 1 of 2)

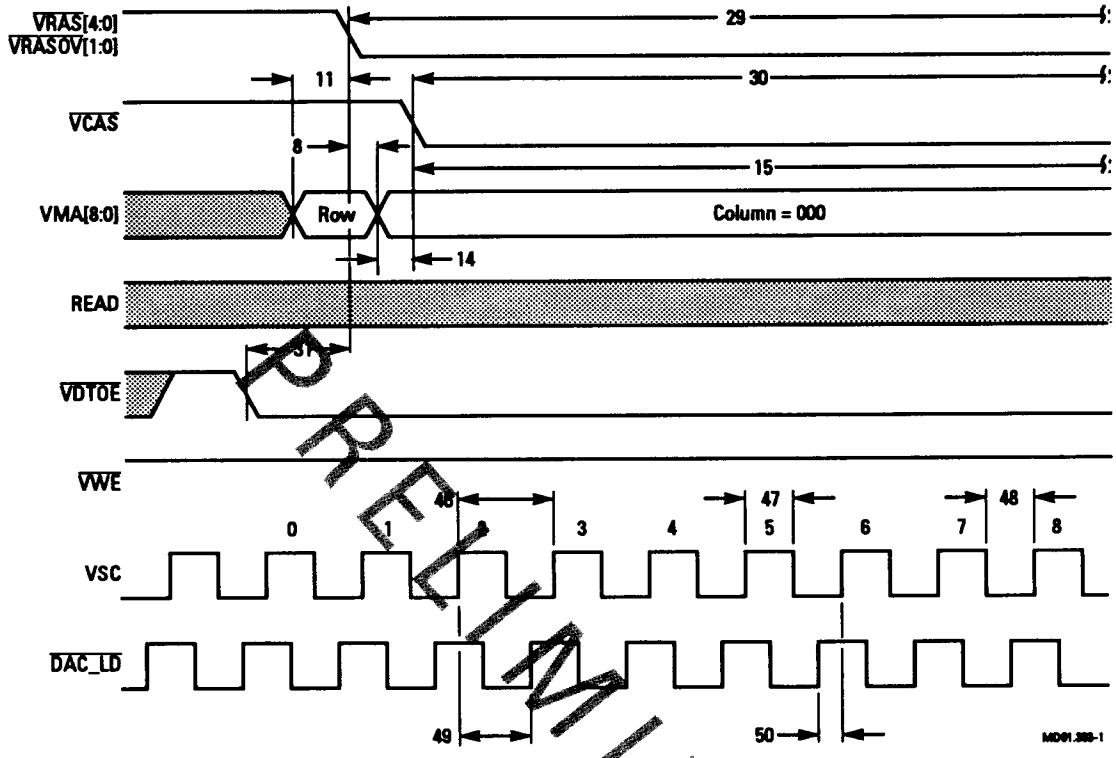


Figure 5.10
Data Transfer
1152 x 900 76Hz
(Sheet 2 of 2)

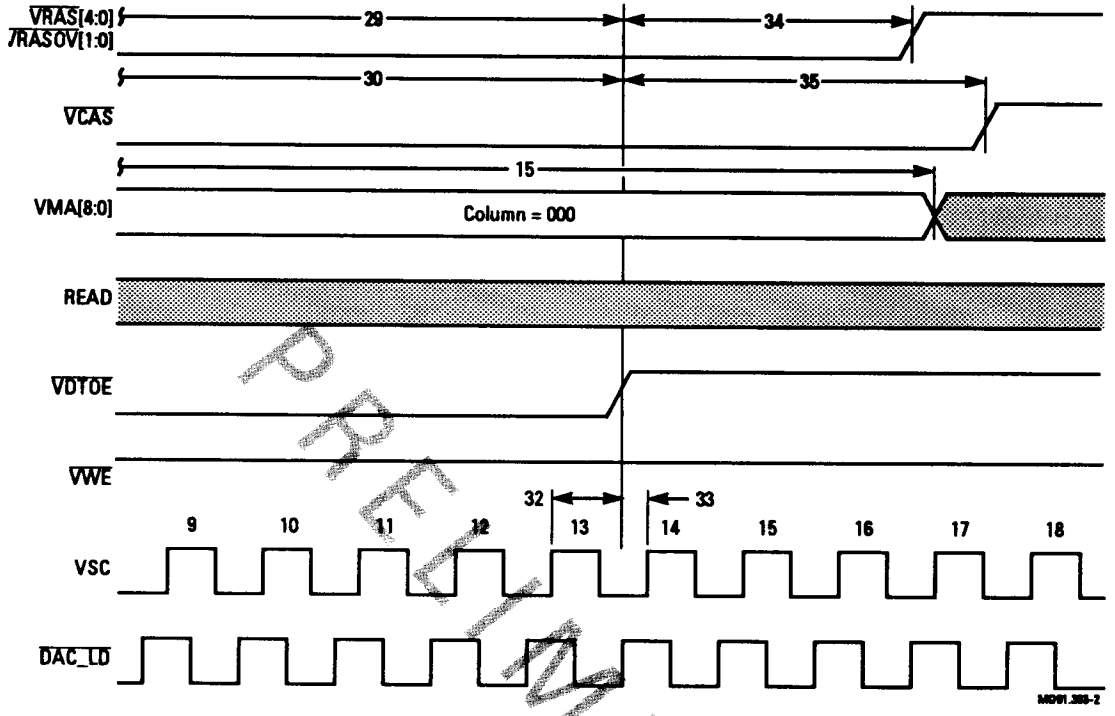


Figure 5.11
Data Transfer
1280x1024 60Hz
(Sheet 1 of 2)

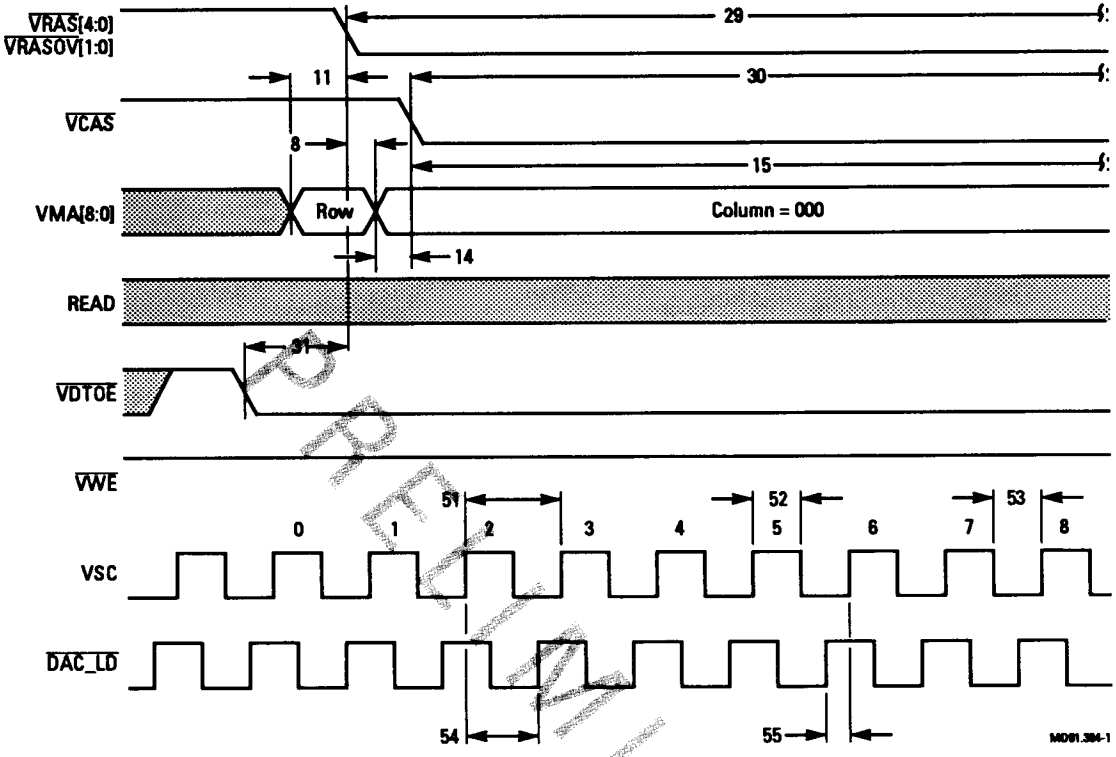


Figure 5.11
Data Transfer
1280x1024 60Hz
(Sheet 2 of 2)

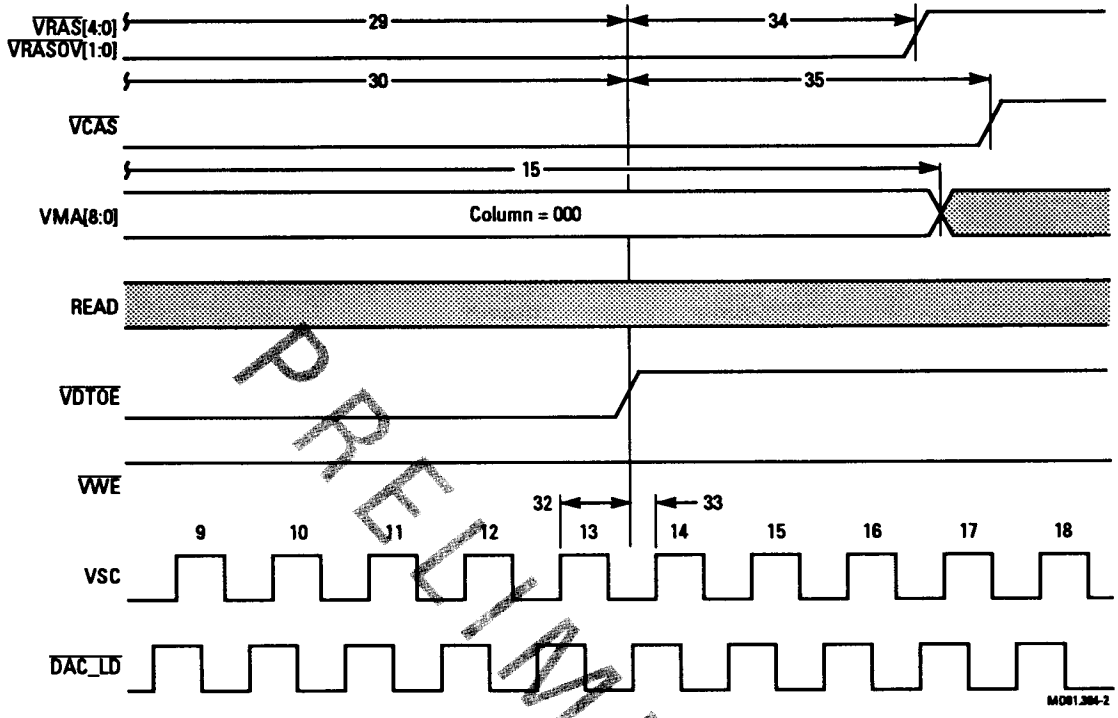


Figure 5.12
CAS Before Refresh Cycle

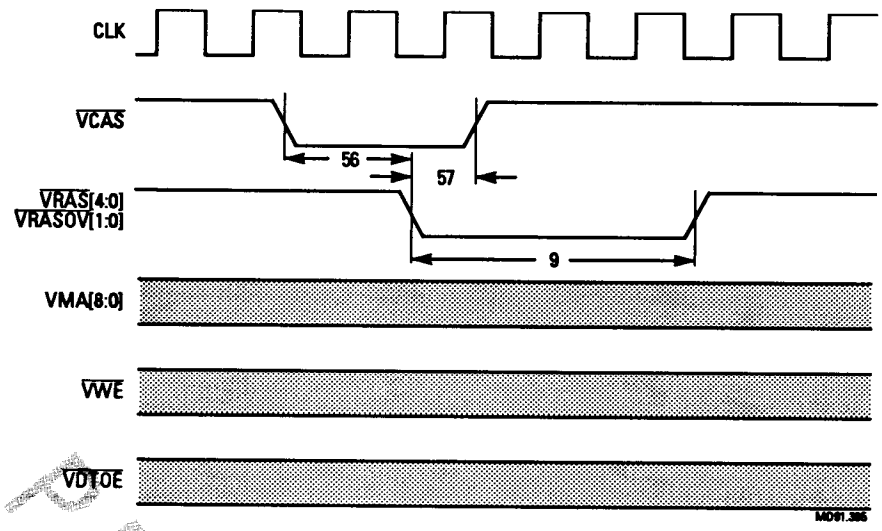


Figure 5.13
DAC_CLKP Cycle 1024x768 60Hz

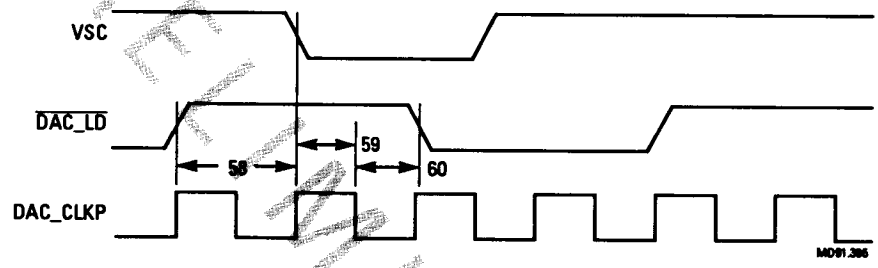


Figure 5.14
DAC_CLKP Cycle 1152x900 66Hz

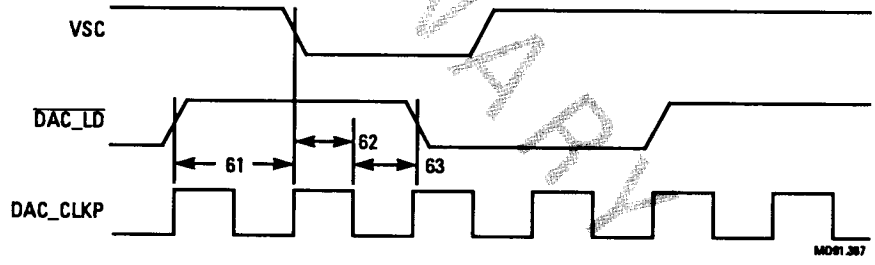


Figure 5.15
DAC_CLKP Cycle
1152x900 76Hz

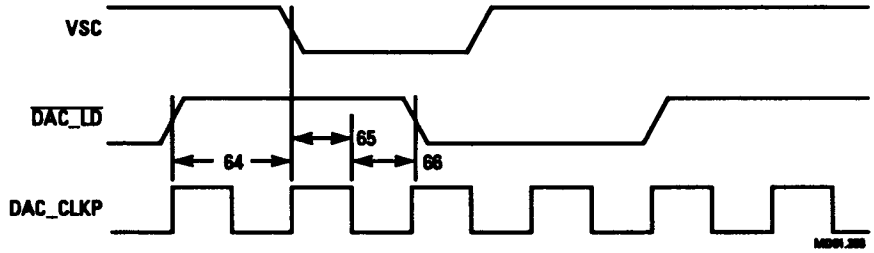


Figure 5.16
DAC_CLKP Cycle
1280x1024 60Hz

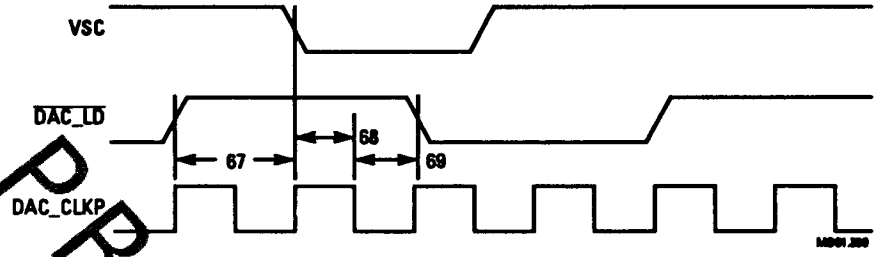


Table 5.5 AC Timing Parameters (Sheet 1 of 2)

Parameter	Description	Min	Max	Units
1.	CLK cycle	40	60	ns
2.	CLK HIGH	17		ns
3.	CLK LOW	17		ns
4.	$\overline{AS}$ input setup to CLK HIGH	15		ns
5.	From CLK HIGH to $\overline{AS}$ invalid input hold	0		ns
6.	VAD/VDD to read data delay	28		ns
7.	CLK HIGH to $\overline{VRAS}$ active	31.5	33	ns
8.	Row address hold time	18		ns
9.	From $\overline{VRAS}$ HIGH/LOW to $\overline{VRAS}$ LOW/HIGH	120	180	ns
10.	From CLK HIGH to $\overline{VRAS}$ inactive	9	33	ns
11.	Row address setup	3.8		ns
12.	From CLK HIGH to $\overline{VCAS}$ active	5	17	ns
13.	From CLK HIGH to $\overline{VCAS}$ inactive	6	20	ns
14.	Column address setup	5		ns
15.	Column address hold	120		ns
16.	From $\overline{VCAS}$ HIGH/LOW to $\overline{VCAS}$ LOW/HIGH	120	180	ns
17.	Access time from $\overline{VRAS}$	85		ns
18.	Access time from $\overline{VDTOE}$	17		ns
19.	Output disable time from $\overline{VDTOE}$ HIGH	0	20	ns
20.	Output disable time from $\overline{VCAS}$ HIGH	6	22	ns
21.	Access time falling edge of $\overline{VCAS}$	25		ns
22.	From CLK HIGH to $\overline{ACK}$ active output delay	22.5		ns
23.	From CLK HIGH to $\overline{ACK}$ inactive output delay	22.5		ns
24.	From CLK HIGH to $\overline{ACK}$ 3-state output delay	35		ns
25.	From $\overline{VCAS}$ LOW to $\overline{VWE}$ HIGH/LOW (write)	3.5		ns
26.	Write video data setup	28		ns
27.	$\overline{VWE}$ pulse width	122.5		ns
28.	Write video data hold	75		ns
29.	$\overline{VDTOE}$ LOW hold after $\overline{VRAS}$	436		ns
30.	$\overline{VDTOE}$ LOW hold after $\overline{VCAS}$	404		ns
31.	$\overline{VDTOE}$ LOW setup	42		ns
32.	From VSC HIGH to $\overline{VDTOE}$ HIGH delay	24		ns
33.	VSC LOW hold time after $\overline{VDTOE}$ HIGH	20		ns
34.	$\overline{VDTOE}$ HIGH to $\overline{VRAS}$ HIGH delay	128.5		ns

Table 5.5 AC Timing Parameters (Sheet 2 of 2)

Parameter	Description	Min	Max	Unit
35.	$\overline{\text{VDTOE}}$ HIGH to $\overline{\text{VCAS}}$ HIGH delay	159.9		ns
36.	VSC cycle (1024*768 60Hz)	62.4		ns
37.	VSC HIGH (1024*768 60Hz)	28		ns
38.	VSC LOW (1024*768 60Hz)	34.5		ns
39.	From VSC HIGH to $\overline{\text{DAC\_LD}}$ HIGH (1024*768 60Hz)	52		ns
40.	From $\overline{\text{DAC\_LD}}$ HIGH to VSC HIGH (1024*768 60Hz)	10.5		ns
41.	VSC cycle (1152*900 66Hz)	43		ns
42.	VSC HIGH (1152*900 66Hz)	18.5		ns
43.	VSC LOW (1152*900 66Hz)	25		ns
44.	VSC HIGH to $\overline{\text{DAC\_LD}}$ HIGH (1152*900 66Hz)	33		ns
45.	From $\overline{\text{DAC\_LD}}$ HIGH to VSC HIGH (1152*900 66Hz)	10.5		ns
46.	VSC cycle (1152*900 76Hz)	38		ns
47.	VSC HIGH (1152*900 76Hz)	15.5		ns
48.	VSC LOW (1152*900 76Hz)	22.5		ns
49.	From VSC HIGH to $\overline{\text{DAC\_LD}}$ HIGH (1152*900 76Hz)	27.5		ns
50.	From $\overline{\text{DAC\_LD}}$ HIGH to VSC HIGH (1152*900 76Hz)	10.5		ns
51.	VSC cycle (1280*1024 60Hz)	46		ns
52.	VSC HIGH (1280*1024 60Hz)	23.5		ns
53.	VSC LOW (1280*1024 60Hz)	22.5		ns
54.	From VSC HIGH to $\overline{\text{DAC\_LD}}$ HIGH (1280*1024 60Hz)	35.5		ns
55.	From $\overline{\text{DAC\_LD}}$ HIGH to VSC HIGH (1280*1024 60Hz)	10.5		ns
56.	$\overline{\text{VCAS}}$ before $\overline{\text{VRAS}}$ refresh setup	47.5		ns
57.	$\overline{\text{VCAS}}$ before $\overline{\text{VRAS}}$ refresh hold	36		ns
58.	DAC_CLKP cycle (1024*768 60Hz)	15.5		ns
59.	DAC_CLKP HIGH (1024*768 60Hz)	7		ns
60.	DAC_CLKP LOW (1024*768 60Hz)	9		ns
61.	DAC_CLKP cycle (1152*900 66Hz)	11		ns
62.	DAC_CLKP HIGH (1152*900 66Hz)	4.5		ns
63.	DAC_CLKP LOW (1152*900 66Hz)	6.5		ns
64.	DAC_CLKP cycle (1152*900 76Hz)	9.5		ns
65.	DAC_CLKP HIGH (1152*900 76Hz)	4		ns
66.	DAC_CLKP LOW (1152*900 76Hz)	6		ns
67.	DAC_CLKP cycle (1280*1024 60Hz)	9		ns
68.	DAC_CLKP HIGH (1280*1024 60Hz)	4.5		ns
69.	DAC_CLKP LOW (1280*1024 60Hz)	5.5		ns

Table 5.6
Pin Description Summary

Mnemonic	*Description*	*Drive (mA)*	*I/O*
CLK	SBus Clock		Input
$\overline{AS}$	SBus Address Strobe		Input
OSC1280	Oscillator		Input
OSC1152	Oscillator		Input
PA[23:0]	SBus Physical Address		Input
READ	SBus Read/Write		Input
$\overline{RESET}$	Power on Reset		Input
SIZ[2:0]	SBus Transfer Size		Input
$\overline{SEL}$	SBus Chip Select		Input
SNS[1:0]	Monitor Sense Line		Input
$\overline{ACK}$[2:0]	SBus Slave Acknowledge	4	Output
D[31:0]	SBus Data	4	Bidirectional
$\overline{DAC\_BLK}$	RAMDAC Blank	2	Output
$\overline{DAC\_CE}$	RAMDAC Chip Enable	2	Output
DAC_CLKP	RAMDAC Pixel Clock	8	Output
$\overline{DAC\_LD}$	Load Output to RAMDAC	2	Output
$\overline{FCPROM}$	FCode PROM Enable	1	Output
$\overline{IRQ}$	SBus Interrupt Request	4	3-State Output, Open Drain
LOAD	Clock for Ovrly and Mono	2	Output
SYNC	Composite Video Sync	1	Output
VAD[7:0]	VRAM Pixel Port A	2	3-State Bidirectional
VBD[7:0]	VRAM Pixel Port B	1	3-State Bidirectional
VCD[7:0]	VRAM Pixel Port C	1	3-State Bidirectional
VDD[7:0]	VRAM Pixel Port D	1	3-State Bidirectional
VED[7:0]	VRAM Pixel Port E	1	3-State Bidirectional
$\overline{VCAS}$	CAS Strobe	6	Output
$\overline{VDTOE}$	Data Transfer Enable	6	Output
VMA[8:0]	Multiplexed Address	4	Output
$\overline{VRAS}$[4:0]	RAS Strobe	1	Output
$\overline{VRASOV0}$	Overlay 0 RAS	1	Output
$\overline{VRASOV1}$	Overlay1 RAS	1	Output
VSC	VRAM Shift Clock	6	Output
$\overline{VWE}$	VRAM Write Enable	6	Output

Total signals = 160 (36 inputs, 31 outputs, 72 bidirectional, 6 power, 13 ground)

5.3 Pinouts and Mechanical

This section contains the mechanical drawings and pinouts for the 64855 Sbus Video Controller chip. Pinouts are shown in Figure 5.17. Mechanicals are shown in Figure 5.18. A pin list follows the figures.

Figure 5.17 160-pin PQFP Pinout

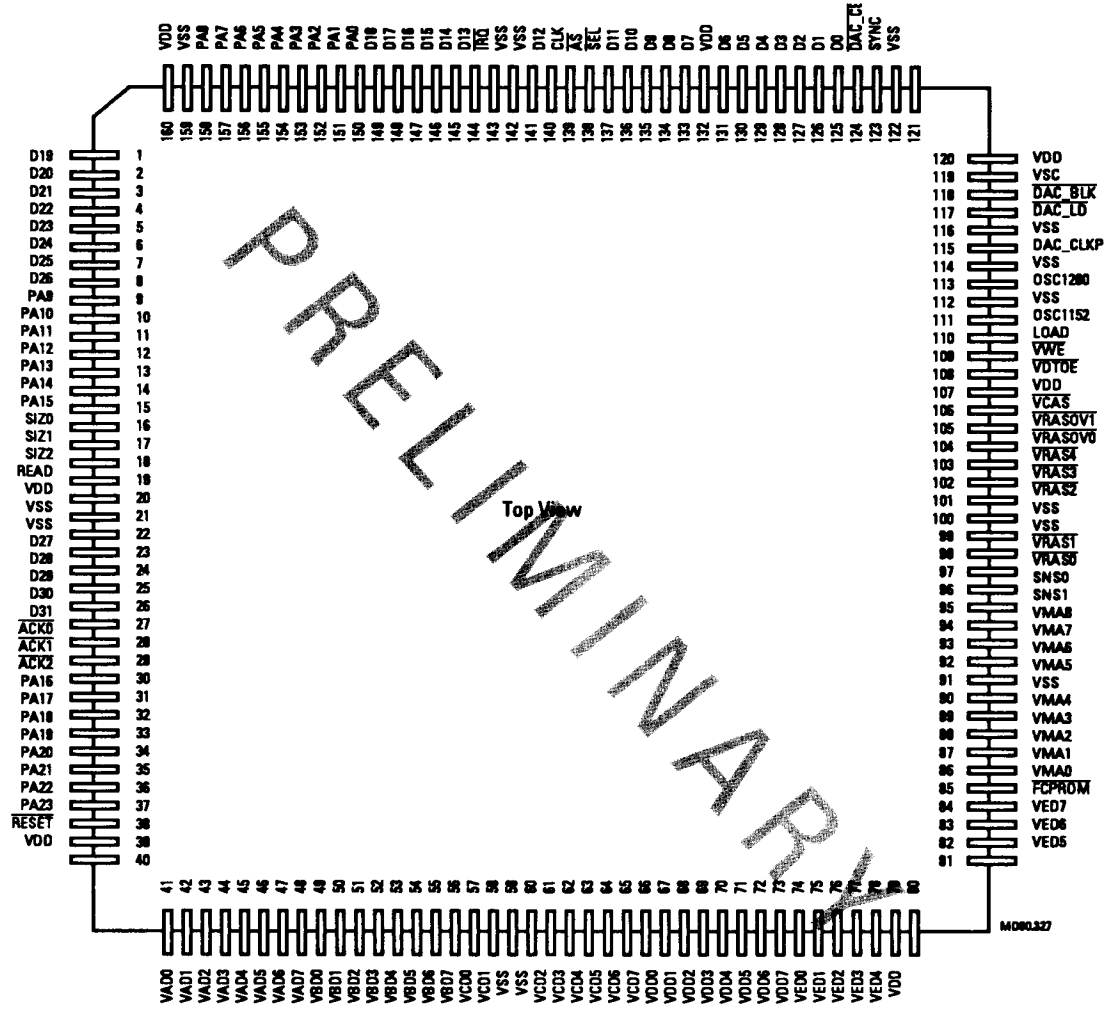
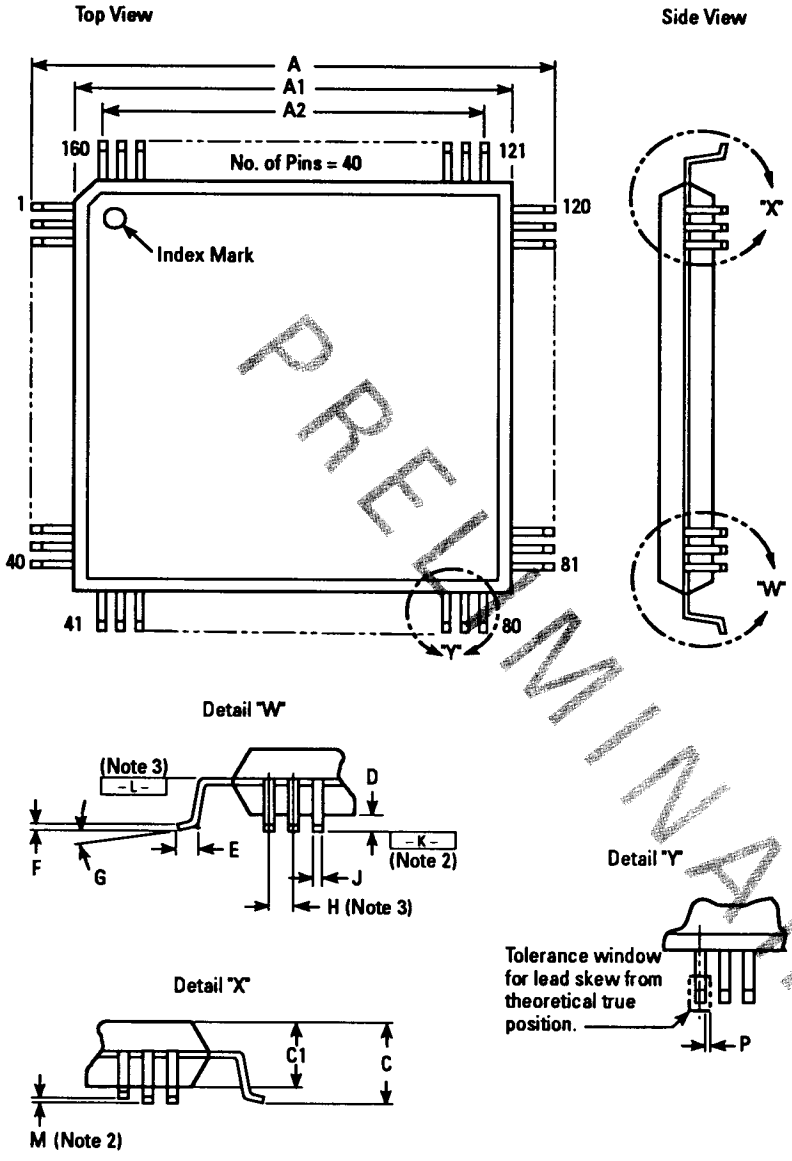


Figure 5.18
160-pin PQFP
Mechanical
Drawing



Dimension		Millimeters (Inches)
A	Min	31.60 Sq (1.244)
	Max	32.40 Sq (1.276)
A1	Min	27.90 Sq (1.098)
	Max	28.10 Sq (1.106)
A2	Ref	25.35 Sq (0.998)
C	Max	3.94 (0.155)
C1	Max	3.55 (0.140)
D	Max	0.030 (0.012)
E	Min	0.061 (0.024)
	Max	1.00 (0.039)
F	Min	0.10 (0.004)
	Max	0.25 (0.010)
G	Min	0 degrees
	Max	10 degrees
H	Nom	0.65 (0.026)
J	Min	0.25 (0.010)
	Max	0.35 (0.014)
M	Max	0.10 (0.004)
P	Max	0.05 (0.002)

Notes:
1. Controlling dimension – mm.
2. Coplanarity of all leads shall be within .010 mm (difference between the highest and lowest lead with seating plane –K– as reference).
3. Lead pitch determined at –L–.
4. Drawing is not to scale.

Table 5.7
L64855 Pin List

Pin Name	Number	Pin Name	Number	Pin Name	Number	Pin Name	Number	Pin Name	Number
$\overline{ACK0}$	28	D23	5	PA18	33	VCD0	57	VMA0	85
$\overline{ACK1}$	29	D24	6	PA19	34	VCD1	58	VMA1	86
$\overline{ACK2}$	30	D25	7	PA20	35	VCD2	61	VMA2	87
$\overline{AS}$	138	D26	8	PA21	36	VCD3	62	VMA3	88
CLK	139	D27	23	PA22	37	VCD4	63	VMA4	89
$\overline{DAC\_BLK}$	118	D28	24	PA23	38	VCD5	64	VMA5	91
$\overline{DAC\_CE}$	123	D29	25	READ	19	VCD6	65	VMA6	92
DAC_CLKP	115	D30	26	$\overline{RESET}$	39	VCD7	66	VMA7	93
$\overline{DAC\_LD}$	117	D31	27	SIZ0	16	VDD0	67	VMA8	94
D0	124	$\overline{FCPROM}$	84	SIZ1	17	VDD1	68	$\overline{VRAS0}$	97
D1	125	$\overline{IRQ}$	143	SIZ2	18	VDD2	69	$\overline{VRAS1}$	98
D2	126	LOAD	110	$\overline{SEL}$	137	VDD3	70	$\overline{VRAS2}$	101
D3	127	OSC1152	111	SNS0	136	VDD4	71	$\overline{VRAS3}$	102
D4	128	OSC1280	113	SNS1	135	VDD5	72	$\overline{VRAS4}$	103
D5	129	PA0	150	SYNC	122	VDD6	73	$\overline{VRASOV0}$	104
D6	130	PA1	151	VAD0	41	VDD7	74	$\overline{VRASOV1}$	105
D7	132	PA2	152	VAD1	42	VDD	20	VSC	119
D8	133	PA3	153	VAD2	43	VDD	40	VSS	21
D9	134	PA4	154	VAD3	44	VDD	80	VSS	22
D10	135	PA5	155	VAD4	45	VDD	107	VSS	59
D11	136	PA6	156	VAD5	46	VDD	120	VSS	60
D12	140	PA7	157	VAD6	47	VDD	131	VSS	90
D13	144	PA8	158	VAD7	48	VDD	160	VSS	99
D14	145	PA9	9	VBD0	49	$\overline{VDTOE}$	108	VSS	100
D15	146	PA10	10	VBD1	50	VED0	75	VSS	112
D16	147	PA11	11	VBD2	51	VED1	76	VSS	114
D17	148	PA12	12	VBD3	52	VED2	77	VSS	116
D18	149	PA13	13	VBD4	53	VED3	78	VSS	121
D19	1	PA14	14	VBD5	54	VED4	79	VSS	141
D20	2	PA15	15	VBD6	55	VED5	81	VSS	142
D21	3	PA16	31	VBD7	56	VED6	82	VSS	159
D22	4	PA17	342	$\overline{VCAS}$	106	VED7	83	VWE	109