



# LXT905

## *Universal 10BASE-T Transceiver with 3.3V Support*

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### Datasheet

The LXT905 Universal 10BASE-T Transceiver is designed for IEEE 802.3 physical layer applications. It provides, in a single CMOS device, all the active circuitry for interfacing most standard 802.3 controllers to 10BASE-T media.

LXT905 functions include Manchester encoding/decoding, receiver squelch and transmit pulse shaping, jabber, link integrity testing, and reversed polarity detection/correction. The LXT905 drives the 10BASE-T twisted-pair cable with only a simple isolation transformer using a single 3.3V or 5V power supply. Integrated filters simplify the design work required for FCC-compliant EMI performance.

## Applications

- Cable Modems
- Hub/Switched Dedicated LANs for 10BASE-T
- Desktop 10BASE-T LAN adapter boards
- USB to Ethernet Converters

## Product Features

- Transparent 3.3 V or 5 V operation
- Integrated filters – Simplifies FCC compliance
- Integrated Manchester encoder/decoder
- 10BASE-T compliant transceiver
- Automatic polarity correction
- SQE enable/disable
- Four LED drivers
- Full duplex capability
- Power-down mode with tristate
- Available in 28-pin PLCC and 32-pin LQFP packages
- Commercial Temperature Range ( 0 to +70°C)
- Extended Temperature Range (-40 to +85°C)



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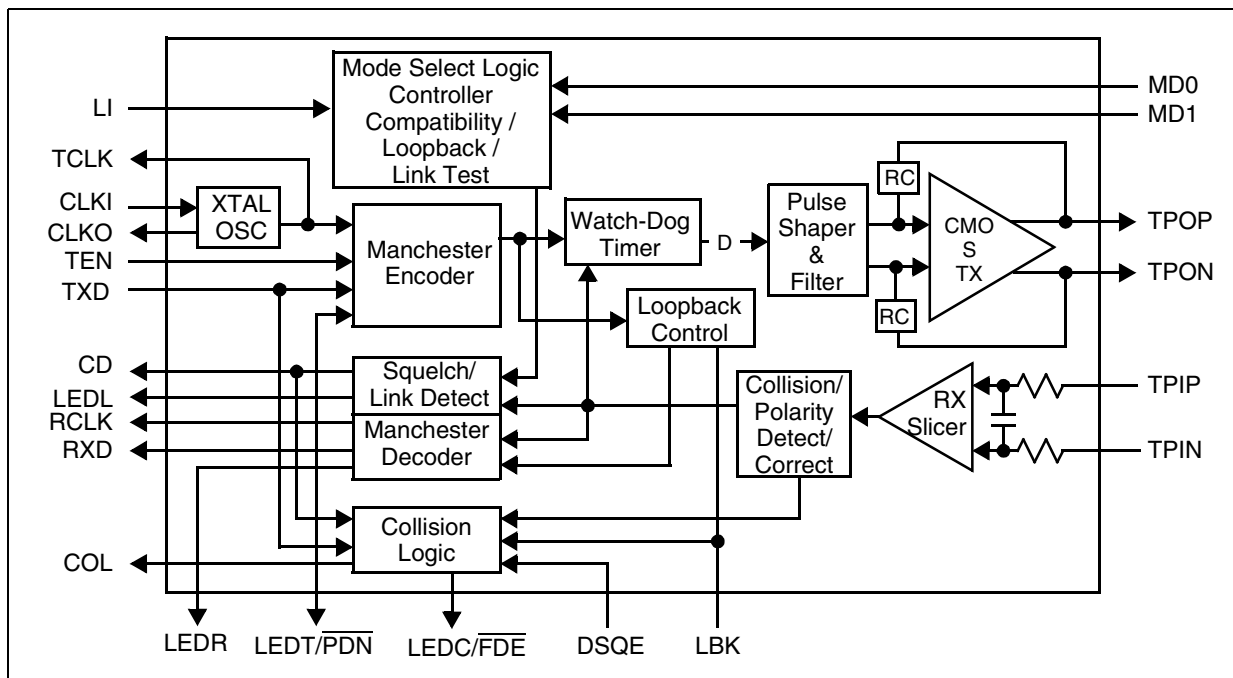
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## Revision History

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| Revision | Date  | Description                                     |
|----------|-------|-------------------------------------------------|
| 2.7      | 10/00 | Change resistor values for Figures 7, 8, and 9. |

Figure 1. LXT905 Block Diagram



## 1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT905 Pin Assignments

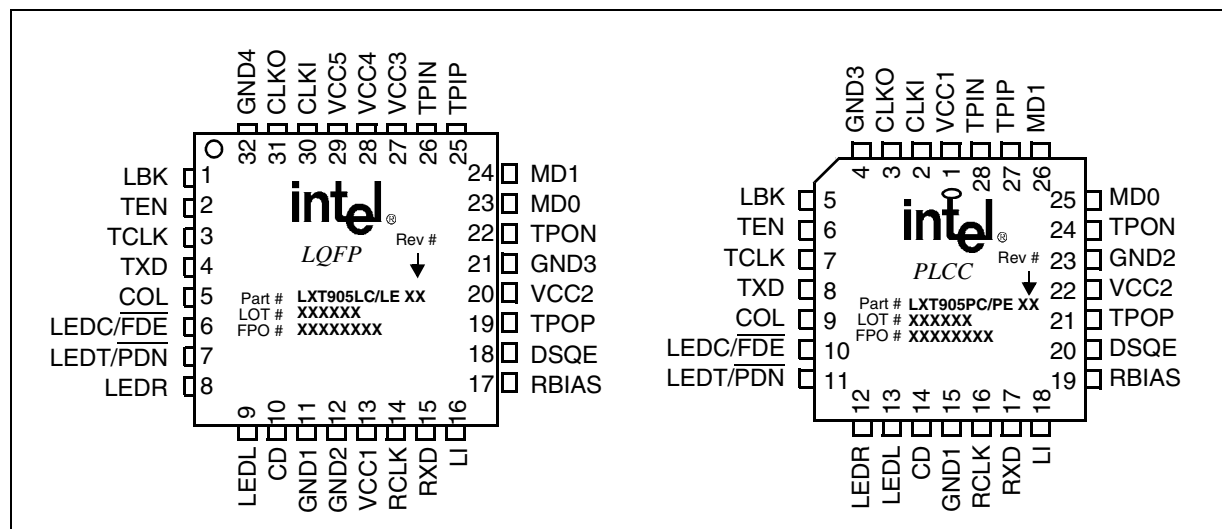


Table 1. LXT905 Signal Descriptions

| LQFP Pin # | PLCC Pin # | Symbol | I/O | Description                                                                                                                                                                                                   |
|------------|------------|--------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13         | 1          | VCC1   | —   | <b>Power Inputs 1 thru 5.</b> Power supply inputs of 3.3V or 5V.                                                                                                                                              |
| 20         | 22         | VCC2   | —   |                                                                                                                                                                                                               |
| 27         | —          | VCC3   | —   |                                                                                                                                                                                                               |
| 28         | —          | VCC4   | —   |                                                                                                                                                                                                               |
| 29         | —          | VCC5   | —   |                                                                                                                                                                                                               |
| 30         | 2          | CLKI   | I   | <b>Crystal Oscillator.</b> A 20 MHz crystal must be connected across these pins, or a 20 MHz clock applied at CLKI with CLKO left open.                                                                       |
| 31         | 3          | CLKO   | O   |                                                                                                                                                                                                               |
| 11         | 15         | GND1   | —   | <b>Ground.</b>                                                                                                                                                                                                |
| 12         | 23         | GND2   | —   |                                                                                                                                                                                                               |
| 21         | 4          | GND3   | —   |                                                                                                                                                                                                               |
| 32         | —          | GND4   | —   |                                                                                                                                                                                                               |
| 1          | 5          | LBK    | I   | <b>Loopback.</b> When High, forces internal loopback. Disables collision and the transmission of both data and link pulses. Pulled Low internally <sup>1</sup> .                                              |
| 2          | 6          | TEN    | I   | <b>Transmit Enable.</b> Enables data transmission and starts the Watch-Dog Timer (WDT). Synchronous to TCLK. Pulled Low internally <sup>1</sup> .                                                             |
| 3          | 7          | TCLK   | O   | <b>Transmit Clock.</b> A 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of the controller.                                                                   |
| 4          | 8          | TXD    | I   | <b>Transmit Data.</b> Input signal containing NRZ data to be transmitted on the network. TXD should be connected directly to the transmit data output of the controller. Pulled Low internally <sup>1</sup> . |
| 5          | 9          | COL    | O   | <b>Collision Signal.</b> Output that drives the collision detect input of the controller.                                                                                                                     |

1. Externally pull-up or pull-down each pin separately using a 10k  $\Omega$ , 1% termination resistor or tie directly to Vcc or ground.  
 2. Do not allow this pin to float. If unused, tie High.

Table 1. LXT905 Signal Descriptions (Continued)

| LQFP Pin #                                                                                                                                                                                         | PLCC Pin # | Symbol       | I/O    | Description                                                                                                                                                                                                                                                                                                                                                                      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6                                                                                                                                                                                                  | 10         | LEDC/<br>FDE | O<br>I | <b>LED Collision or Full Duplex Enable.</b><br><b>LEDC</b> is an open drain driver for the collision indicator pulls Low during collision. LED “on” (which is Low output) time is extended by approximately 100 ms.<br><b>FDE</b> enables full duplex mode (external loopback) if tied Low externally. Pulled High internally <sup>1</sup> .                                     |
| 7                                                                                                                                                                                                  | 11         | LEDT/<br>PDN | O<br>I | <b>LED Transmit or Power Down.</b><br><b>LEDT</b> is an open drain driver for the transmit indicator. LED “on” (which is Low output) time is extended by approximately 100 ms. Output is pulled Low during transmit. <sup>2</sup><br>If externally tied Low, the LXT905 goes to power down state ( <b>PDN</b> ). In power-down mode, all logic inputs and outputs are tristated. |
| 8                                                                                                                                                                                                  | 12         | LEDR         | O      | <b>LED Receive.</b> Open drain driver for the receive indicator LED. LED “on” ( <i>i.e.</i> , Low output) time is extended by approximately 100 ms. Output is pulled Low during receive. Pulled High internally <sup>1</sup> .                                                                                                                                                   |
| 9                                                                                                                                                                                                  | 13         | LEDL         | O      | <b>LED Link.</b> Open drain driver for link integrity indicator. Output is pulled Low during link test pass. Pulled High internally <sup>1</sup> .                                                                                                                                                                                                                               |
| 10                                                                                                                                                                                                 | 14         | CD           | O      | <b>Carrier Detect.</b> An output for notifying the controller that activity exists on the network.                                                                                                                                                                                                                                                                               |
| 14                                                                                                                                                                                                 | 16         | RCLK         | O      | <b>Receive Clock.</b> A recovered 10 MHz clock that is synchronous to the received data and connected to the controller receive clock input.                                                                                                                                                                                                                                     |
| 15                                                                                                                                                                                                 | 17         | RXD          | O      | <b>Receive Data.</b> Output signal connected directly to the receive data input of the controller.                                                                                                                                                                                                                                                                               |
| 16                                                                                                                                                                                                 | 18         | LI           | I      | <b>Link Enable.</b> Controls link integrity test; enabled when LI is High, disabled when LI is Low.                                                                                                                                                                                                                                                                              |
| 17                                                                                                                                                                                                 | 19         | RBIAS        | I      | <b>Bias Circuitry.</b> A 7.5 k $\Omega$ 1% resistor to ground at this pin controls operating circuit bias.                                                                                                                                                                                                                                                                       |
| 18                                                                                                                                                                                                 | 20         | DSQE         | I      | <b>SQE Disable.</b> When DSQE is High, the SQE function is disabled.<br>When DSQE is Low, the SQE function is enabled. SQE should be disabled for normal operation in Hub/Switch/Repeater applications. Pulled Low internally <sup>1</sup> .                                                                                                                                     |
| 19<br>22                                                                                                                                                                                           | 21<br>24   | TPOP<br>TPON | O<br>O | <b>Twisted-Pair Outputs.</b> Differential outputs to the twisted-pair cable. The outputs are pre-equalized.                                                                                                                                                                                                                                                                      |
| 23<br>24                                                                                                                                                                                           | 25<br>26   | MDO<br>MDI   | I<br>I | <b>Mode Select 0 and 1.</b> Mode select pins determine controller compatibility mode in accordance with Table 2. Pulled Low internally <sup>1</sup> .                                                                                                                                                                                                                            |
| 25<br>26                                                                                                                                                                                           | 27<br>28   | TPIP<br>TPIN | I<br>I | <b>Twisted-Pair Inputs.</b> A differential input pair from the twisted-pair cable. Receive filter is integrated on-chip. No external filters are required.                                                                                                                                                                                                                       |
| 1. Externally pull-up or pull-down each pin separately using a 10k $\Omega$ , 1% termination resistor or tie directly to VCC or ground.<br>2. Do not allow this pin to float. If unused, tie High. |            |              |        |                                                                                                                                                                                                                                                                                                                                                                                  |

## 2.0 Functional Description

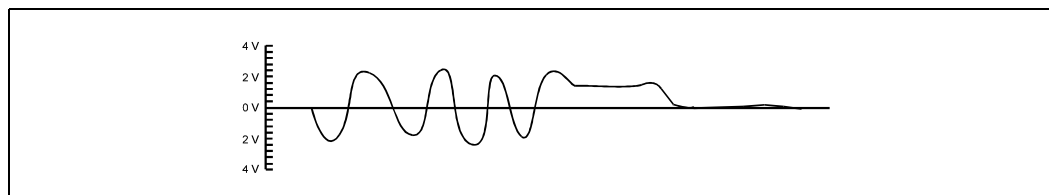
### 2.1 Introduction

The LXT905 Universal 10BASE-T Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an integrated PLS/MAU for use with 10BASE-T twisted-pair networks.

The LXT905 interfaces a back-end controller to a twisted-pair (TP) cable. The controller interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The twisted-pair interface comprises two circuits: Twisted-Pair Input (TPI) and Twisted-Pair Output (TPO). In addition to the two basic interfaces, the LXT905 contains an internal crystal oscillator and four LED drivers for visual status reporting.

Functions are defined from the back-end controller side of the interface. The LXT905 Transmit function refers to data transmitted by the back end to the twisted-pair network. The LXT905 Receive function refers to data received by the back end from the twisted-pair network. The LXT905 performs all required functions defined by the IEEE 802.3 10BASE-T MAU specification such as collision detection, link integrity testing, signal quality error messaging, jabber control, and loopback.

**Figure 3. LXT905 TPO Output Waveform**



### 2.2 Controller Compatibility Modes

The LXT905 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Intel, Fujitsu, National Semiconductor, Seeq, Motorola and Texas Instruments. Four different control signal timing and polarity schemes (Modes 1 through 4) are required to achieve this compatibility. Mode select pins MD0 and MD1 determine controller compatibility modes as listed in [Table 2](#). Refer to the Test Specifications section for timing diagrams and parameters.

### 2.3 Transmit Function

The LXT905 receives NRZ data from the controller at the TXD input as shown in the block diagram, and passes it through a Manchester encoder. The encoded data is then transferred to the twisted-pair network (the TPO circuit). The advanced integrated pulse shaping and filtering network produces the output signal on TPON and TPOP, shown in [Figure 3](#). The TPO output is pre-distorted and prefiltered to meet the 10BASE-T jitter template. An internal continuous resistor-capacitor filter is used to remove any high-frequency clocking noise from the pulse shaping

circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods, the LXT905 transmits link integrity test pulses on the TPO circuit (if LI is enabled and LBK is disabled).

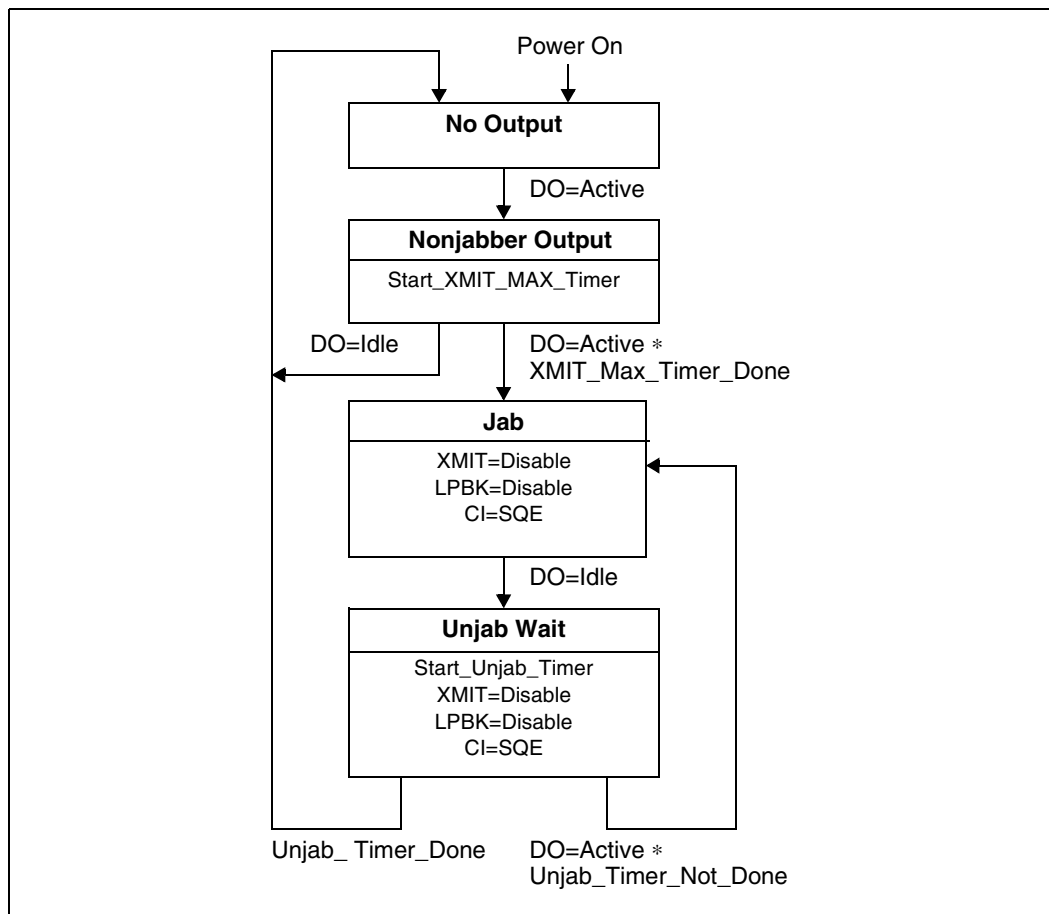
**Table 2. Controller Compatibility Mode Options**

| Controller Mode                                                                                                                                                                                      | MD1  | MD0  |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|
| Mode 1 - For Motorola MC68EN360 or compatible controllers (AMD AM7990)                                                                                                                               | Low  | Low  |
| Mode 2 - For Intel 82596 or compatible controllers <sup>1</sup>                                                                                                                                      | Low  | High |
| Mode 3 - For Fujitsu MB86950, MB86960 or compatible controllers (Seeq 8005) <sup>2</sup>                                                                                                             | High | Low  |
| Mode 4 - For TI TMS380C26 or compatible controllers                                                                                                                                                  | High | High |
| 1. Refer to Intel Application Note 51 (MAC Interface Design Guide for Intel Controllers) when designing with Intel controllers.<br>2. SEEQ controllers require inverters on CLKI, LBK, RCLK and COL. |      |      |

## 2.4 Jabber Control Function

Figure 4 is a state diagram of the LXT905 jabber control function. The LXT905 on-chip Watch-Dog Timer (WDT) prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the WDT disables the transmit and loopback functions and activates the COL pin. Once the LXT905 is in the jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it exits the jabber state.

Figure 4. Jabber Control Function

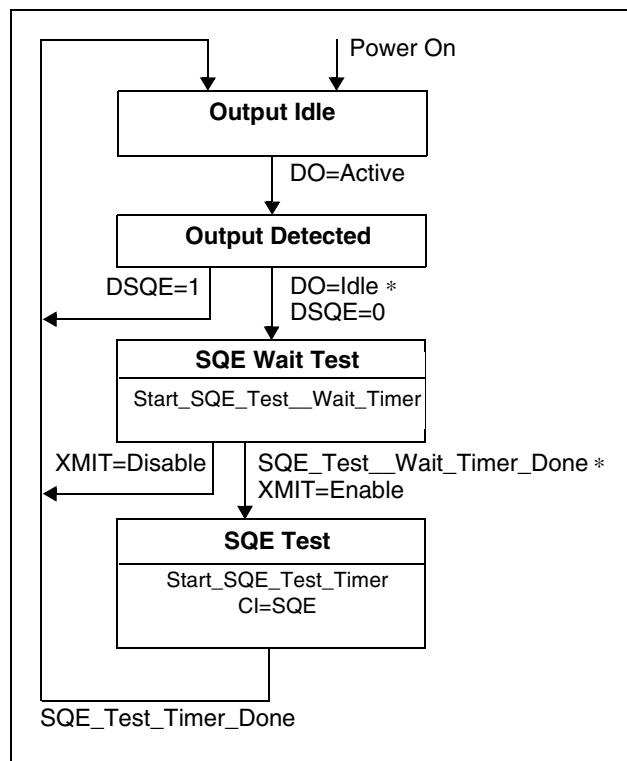


## 2.5 SQE Function

The LXT905 supports the Signal Quality Error (SQE) function as shown in Figure 5. After every successful transmission on the 10BASE-T network, the LXT905 transmits the SQE signal for  $10 \text{ bit times (BT)} \pm 5\text{BT}$  on the COL pin of the device.

The SQE can be disabled for repeater/switch applications. When DSQE is set High, the SQE function is disabled. When DSQE is Low, the SQE function is enabled.

Figure 5. SQE Function



## 2.6 Receive Function

The LXT905 receive function acquires timing and data from the twisted-pair network (the TPI circuit). Valid received signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data and receive timing on the RXD and RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminate noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level with proper timing.

If the differential signal at the TPI circuit inputs falls below 85% of the threshold level (unsquelched) for 8 bit times (typical), the LXT905 receive function enters the idle state. The LXT905 automatically corrects reversed polarity on the TPI circuit.

## 2.7 Polarity Reverse Function

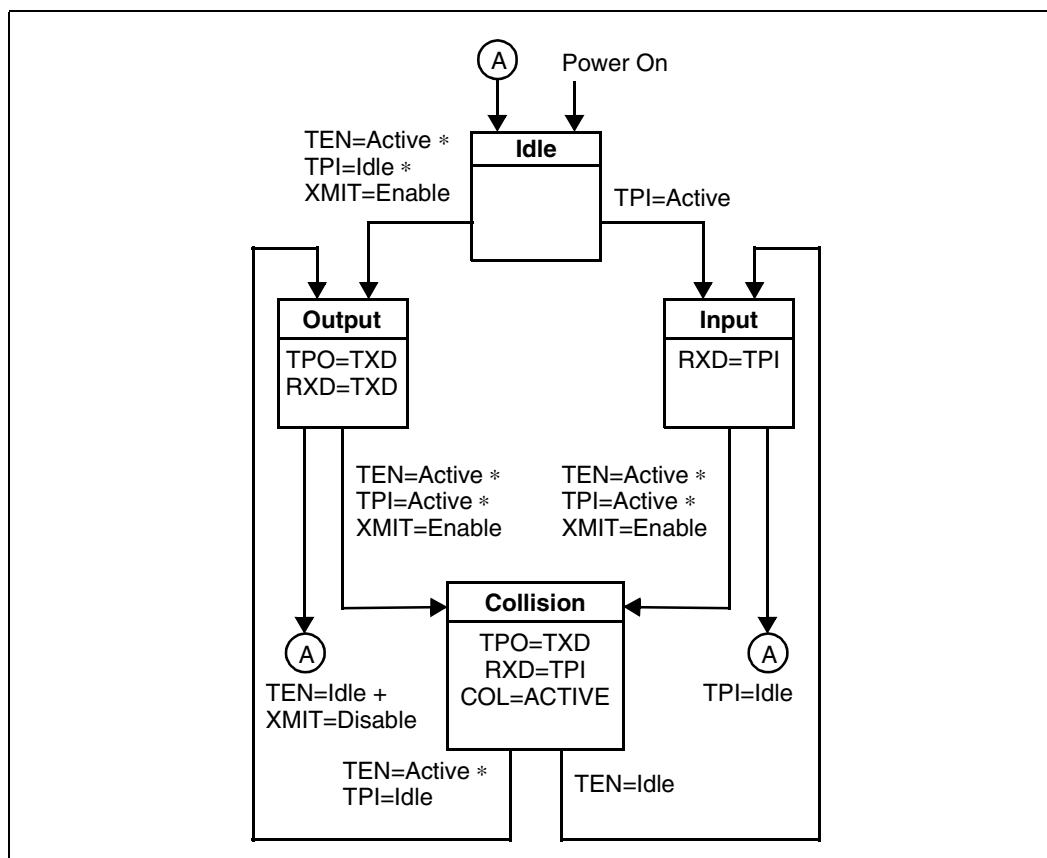
The LXT905 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. If Link Integrity testing is disabled, polarity detection is based only on received data. A reversed polarity condition is detected when eight consecutive opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four consecutive frames are received with a reversed start-of-idle.

Whenever a correct polarity frame or a correct link pulse is received, these two counters are reset to zero. If the LXT905 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. Polarity correction is always enabled.

## 2.8 Collision Detection Function

A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The LXT905 reports collisions to the back-end via the COL pin. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 6 is a state diagram of the LXT905 collision detection function.

Figure 6. Collision Detection Function



## 2.9 Loopback Functions

### 2.9.1 Internal Loopback

The LXT905 provides standard loopback mode as specified in the IEEE specification for the twisted-pair port, as well as a forced internal loopback mode. Loopback mode operates in conjunction with the transmit function. Data transmitted by the MAC is internally looped back within the LXT905 from the TXD pin through the Manchester encoder/decoder to the RXD pin and returned to the MAC.

Standard loopback mode is disabled when a data collision occurs, clearing the RXD circuit for the TPI data. Standard loopback is also disabled during link fail, jabber, and full-duplex states. Loopback is always enabled during forced internal loopback mode.

### 2.9.2 External Loopback/Full Duplex

The LXT905 also provides an external loopback test mode for system-level testing. When both LEDC/ $\overline{\text{FDE}}$  and LBK are Low, the LXT905 enables external loopback and full-duplex mode. Internal loopback circuits, SQE, and collision detection are disabled. Refer to [Table 3](#) for a summary of loopback and duplex modes.

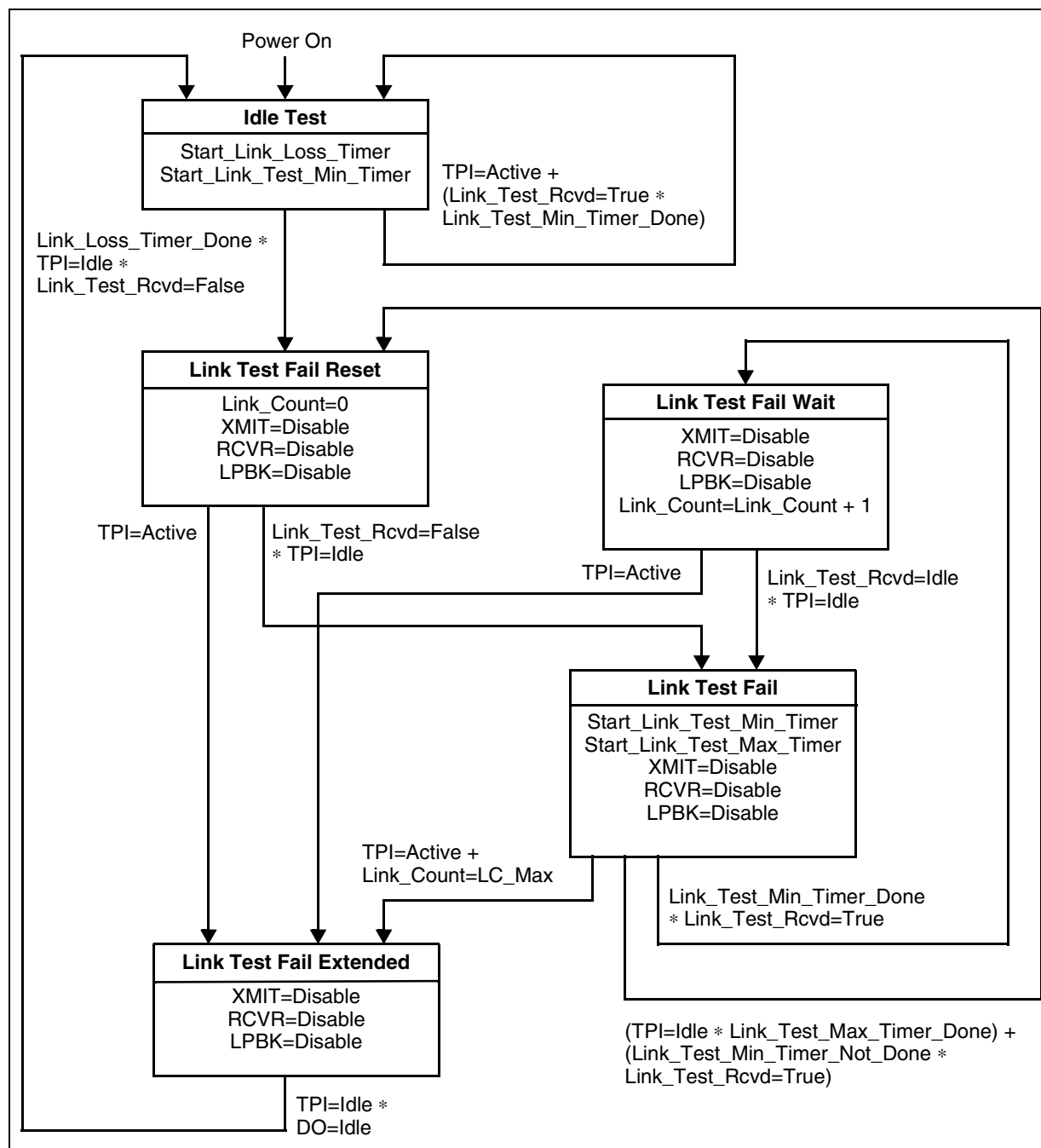
**Table 3. Loopback Modes**

| Pin Settings |              | Mode Description                                                                                                                                                                                                                                           |
|--------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LBK          | LEDC/<br>FDE |                                                                                                                                                                                                                                                            |
| Low          | Low          | Disable internal loopback.<br>Enable external loopback test mode and full-duplex mode.                                                                                                                                                                     |
| Low          | High         | Standard loopback mode (default).<br>Data transmitted by the MAC is internally looped back and returned to the MAC except during collision.<br>Standard loopback is disabled when a data collision occurs, clearing RXD for data on the twisted-pair port. |
| High         | Low          | Not Used.                                                                                                                                                                                                                                                  |
| High         | High         | Forced internal loopback.<br>Transmit data is looped back on the receive data bus and the twisted-pair port is ignored.                                                                                                                                    |

## 2.10 Link Integrity Test Function

[Figure 7](#) is a state diagram of the LXT905 Link Integrity test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is enabled when LI is tied High. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50~150 ms, the chip enters a link fail state and disables the transmit and normal loopback functions. The LXT905 ignores any link integrity pulse with interval less than 2~7 ms. The LXT905 remains in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

Figure 7. Link Integrity Test Function



## 3.0 Application Information

### 3.1 Introduction

Figures 7 through 9 show typical LXT905 applications. These diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins; Transmit Data (TXD), Transmit Clock (TCLK) Transmit Enable (TEN), Receive Data (RXD), Receive Clock (RCLK), Collision Signal (COL) and Carrier Detect (CD) pins are at the upper left.

Power and ground pins are at the bottom of each diagram. VCC1 and VCC2 use a single power supply with decoupling capacitors installed between the power and ground busses. VCC may be powered by a 5V or 3.3V supply.

#### 3.1.1 Termination Circuitry

Several I/O pins are internally pulled-up or pulled-down to keep the signals from floating. It is recommended to hard-wire these pins either High or Low. Externally pull-up pins (LEDT/ $\overline{\text{PDN}}$ , LEDC/FDE, LEDR, LEDL) and pull-down pins (LBK, TEN, TXD, DSQE, MDO, MDI) separately using a 10k  $\Omega$ , 1% resistor or tie directly to VCC or ground.

#### 3.1.2 Twisted-Pair Interface

The Twisted-Pair interface (TPOP/N and TPIP/N) is at the upper right. The I/O pairs have impedance-matching resistors for 100 $\Omega$  UTP, but no external filters are required.

#### 3.1.3 RBIAS Pin

The RBIAS pin sets the levels for the LXT905 output drivers. The LXT905 requires a 7.5k $\Omega$ , 1% resistor directly connected between the RBIAS pin and ground. This resistor should be located as close to the device as possible. Keep the traces as short as possible and isolated from all other high speed signals.

#### 3.1.4 Crystal Information

Based on limited evaluation, [Table 4](#) lists some of the suitable crystals. Designers should test and validate all crystals before committing to a specific component.

**Table 4. Suitable Crystals**

| Manufacturer | Part Number |
|--------------|-------------|
| MTRON        | MP-1        |
|              | MP-2        |

#### 3.1.5 Magnetic Information

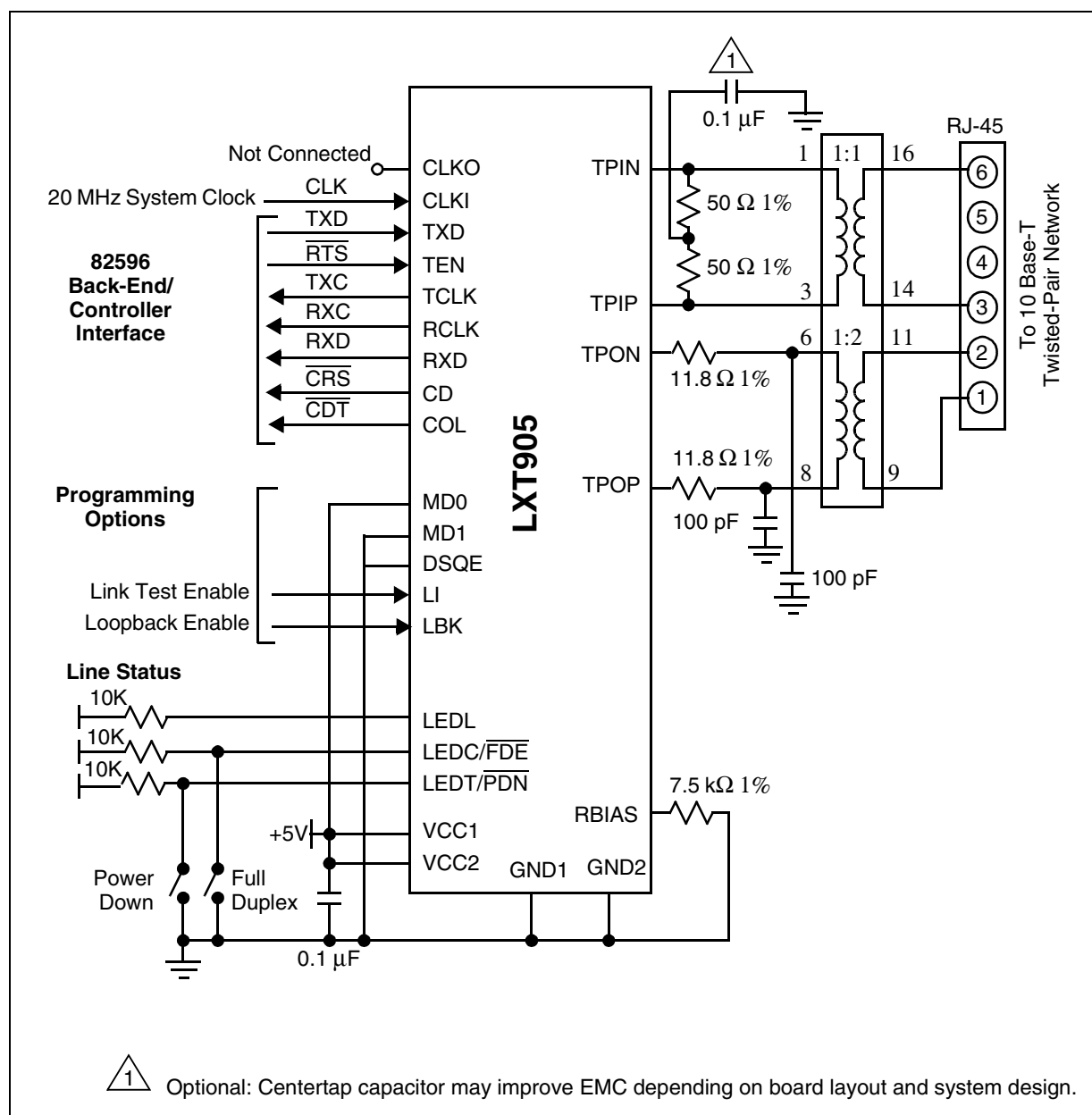
The LXT905 requires a 1:1 turns ratio for the receive transformer and a 1:2 turns ratio for the transmit transformer. [Application Note 073](#) lists transformers suitable for the applications described in this data sheet. Designers are advised to test and validate all magnetics before committing to a specific component.

## 3.2 Typical 10BASE-T Application

Figure 8 is a typical LXT905 application. The DTE is connected to a 10BASE-T network through the twisted-pair RJ-45 connector. With MD0 tied high and MD1 grounded, the LXT905 logic and framing are set to Mode 2 (compatible with Intel 82596 controllers\*). Connect 20 MHz system clock input at CLKI. (Leave CLKO open.) The LI pin externally controls the link test function.

\* Refer to Intel Application Note 51 (MAC Interface Design Guide for Intel Controllers) when designing with Intel controllers.

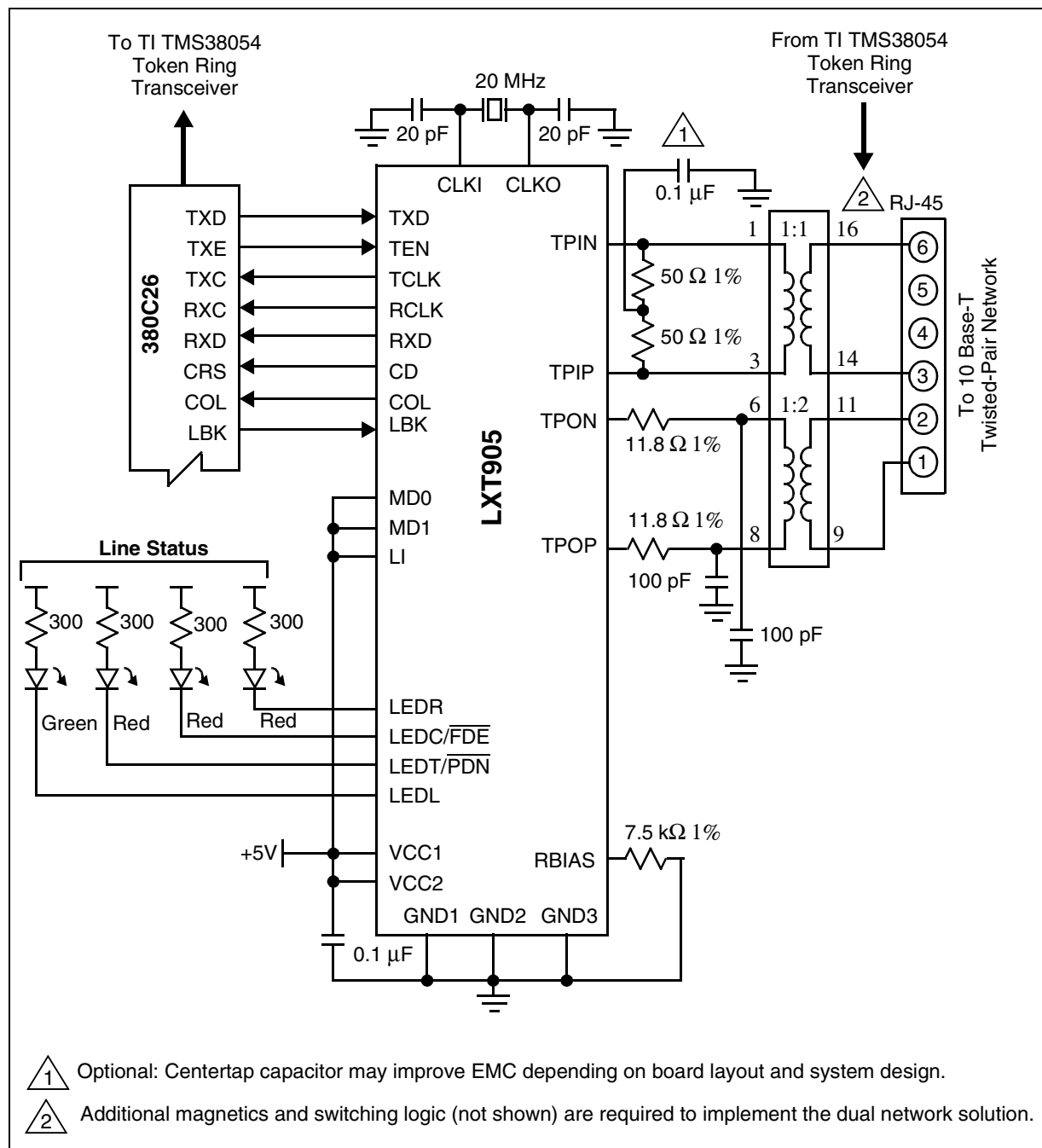
Figure 8. Intel Controller Application (Mode 2)



### **3.3 Dual Network Support - 10BASE-T and Token Ring**

Figure 9 shows the LXT905 with a Texas Instruments 380C26 CommProcessor. The 380C26 is compatible with Mode 4 (MD0 and MD1 both high). When used with the 380C26, both the LXT905 and a TMS38054 Token Ring transceiver can be tied to a single RJ-45 allowing dual network support from a single connector.

**Figure 9. LXT905/380C26 Interface for Dual 10BASE-T and Token Ring Support (Mode 4)**





## 4.0 Test Specifications

**Note:** The minimum and maximum values in Table 5 through Table 13 and Figure 11 through Figure 26 represent the performance specifications of the LXT905 and are guaranteed by test, except where noted by design. Minimum and maximum values in Table 7 through Table 13 apply over the recommended operating conditions specified in Table 6.

**Table 5. Absolute Maximum Values**

| Parameter                                                                                                                                                                                                                | Symbol          | Min  | Max  | Units |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|------|------|-------|
| Supply voltage                                                                                                                                                                                                           | V <sub>CC</sub> | -0.3 | +6   | V     |
| Ambient operating temperature (Commercial)                                                                                                                                                                               | T <sub>OP</sub> | 0    | +70  | °C    |
| Ambient operating temperature (Extended)                                                                                                                                                                                 | T <sub>OP</sub> | -40  | +85  | °C    |
| Storage temperature                                                                                                                                                                                                      | T <sub>ST</sub> | -65  | +150 | °C    |
| <b>Caution:</b> Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. |                 |      |      |       |

**Table 6. Recommended Operating Conditions**

| Parameter                                                        | Symbol          | Min   | Typ | Max  | Units |
|------------------------------------------------------------------|-----------------|-------|-----|------|-------|
| Recommended supply voltage <sup>1</sup>                          | V <sub>CC</sub> | 3.135 | 5.0 | 5.25 | V     |
| Recommended operating temperature (Commercial)                   | T <sub>OP</sub> | 0     | —   | +70  | °C    |
| Recommended operating temperature (Extended)                     | T <sub>OP</sub> | -40   | —   | +85  | °C    |
| 1. Voltage is with respect to ground unless specified otherwise. |                 |       |     |      |       |

**Table 7. I/O Electrical Characteristics**

| Parameter                                                                                                                                                                                                                                                                                                     |      | Sym              | Min | Typ <sup>1</sup> | Max | Units            | Test Conditions           |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------------------|-----|------------------|-----|------------------|---------------------------|
| Input low voltage <sup>2</sup>                                                                                                                                                                                                                                                                                |      | V <sub>IL</sub>  | —   | —                | 0.8 | V                |                           |
| Input high voltage <sup>2</sup>                                                                                                                                                                                                                                                                               |      | V <sub>IH</sub>  | 2.0 | —                | —   | V                |                           |
| Output low voltage                                                                                                                                                                                                                                                                                            |      | V <sub>OL</sub>  | —   | —                | 0.4 | V                | I <sub>OL</sub> = 1.6 mA  |
|                                                                                                                                                                                                                                                                                                               |      | V <sub>OL</sub>  | —   | —                | 10  | %V <sub>CC</sub> | I <sub>OL</sub> < 10 μA   |
| Output low voltage (Open drain LED driver)                                                                                                                                                                                                                                                                    |      | V <sub>OLL</sub> | —   | —                | 0.7 | %V <sub>CC</sub> | I <sub>OLL</sub> = 10 mA  |
| Output high voltage                                                                                                                                                                                                                                                                                           |      | V <sub>OH</sub>  | 2.4 | —                | —   | V                | I <sub>OH</sub> = 40 μA   |
|                                                                                                                                                                                                                                                                                                               |      | V <sub>OH</sub>  | 90  | —                | —   | %V <sub>CC</sub> | I <sub>OH</sub> < 10 μA   |
| Output rise time<br>TCLK & RCLK                                                                                                                                                                                                                                                                               | CMOS | —                | —   | 3                | 15  | ns               | C <sub>LOAD</sub> = 20 pF |
|                                                                                                                                                                                                                                                                                                               | TTL  | —                | —   | 2                | 15  | ns               |                           |
| Output fall time<br>TCLK & RCLK                                                                                                                                                                                                                                                                               | CMOS | —                | —   | 3                | 15  | ns               | C <sub>LOAD</sub> = 20 pF |
|                                                                                                                                                                                                                                                                                                               | TTL  | —                | —   | 2                | 15  | ns               |                           |
| CLKI rise time (externally driven)                                                                                                                                                                                                                                                                            |      | —                | —   | —                | 10  | ns               |                           |
| 1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.<br>2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN. |      |                  |     |                  |     |                  |                           |

**Table 7. I/O Electrical Characteristics**

| Parameter                           |                 | Sym             | Min | Typ <sup>1</sup> | Max   | Units | Test Conditions    |
|-------------------------------------|-----------------|-----------------|-----|------------------|-------|-------|--------------------|
| CLKI duty cycle (externally driven) |                 | —               | —   | 50/50            | 40/60 | %     |                    |
| Supply current                      | Normal          | I <sub>CC</sub> | —   | 40               | 80    | mA    | Idle Mode          |
|                                     | Mode            | I <sub>CC</sub> | —   | 70               | 100   | mA    | Transmitting on TP |
|                                     | Power Down Mode | I <sub>CC</sub> | —   | 0.01             | 1     | μA    |                    |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.  
2. Limited functional tests are performed at these input levels. The majority of functional tests are performed at levels of 0V and 3V. This applies to all inputs except TPIP and TPIN.

**Table 8. TP Electrical Characteristics**

| Parameter                                                               | Symbol           | Min | Typ <sup>1</sup> | Max  | Units | Test Conditions                                                    |
|-------------------------------------------------------------------------|------------------|-----|------------------|------|-------|--------------------------------------------------------------------|
| Transmit output impedance                                               | Z <sub>OUT</sub> | —   | 5                | —    | Ω     |                                                                    |
| Transmit timing jitter addition <sup>2</sup>                            | —                | —   | ±6.4             | ±10  | ns    | 0 line length for internal MAU                                     |
| Transmit timing jitter added by the MAU and PLS sections <sup>2,3</sup> | —                | —   | ±3.5             | ±5.5 | ns    | After line model specified by IEEE 802.3 for 10BASE-T internal MAU |
| Receive input impedance                                                 | Z <sub>IN</sub>  | —   | 24               | —    | kΩ    | Between TPIP/TPIN                                                  |
| Differential squelch threshold                                          | V <sub>DS</sub>  | 300 | 420              | 585  | mV    | 5 MHz square wave input                                            |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.  
2. Parameter is guaranteed by design; not subject to production testing.  
3. IEEE 802.3 specifies maximum jitter additions at 0.5 ns from the encoder, and 3.5 ns from the MAU.

**Table 9. Switching Characteristics**

| Parameter             |                        | Symbol | Minimum | Typical <sup>1</sup> | Maximum | Units |
|-----------------------|------------------------|--------|---------|----------------------|---------|-------|
| Jabber Timing         | Maximum transmit time  | —      | 20      | —                    | 150     | ms    |
|                       | Unjab time             | —      | 250     | —                    | 750     | ms    |
| Link Integrity Timing | Time link loss receive | —      | 50      | —                    | 150     | ms    |
|                       | Link min receive       | —      | 2       | —                    | 7       | ms    |
|                       | Link max receive       | —      | 50      | —                    | 150     | ms    |
|                       | Link transmit period   | —      | 8       | 10                   | 24      | ms    |

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

**Table 10. RCLK/Start-of-Frame Timing**

| Parameter                    |                   | Symbol            | Min | Typ <sup>1</sup> | Max  | Units |
|------------------------------|-------------------|-------------------|-----|------------------|------|-------|
| Decoder acquisition time     |                   | t <sub>DATA</sub> | —   | 1300             | 1500 | ns    |
| CD turn-on delay             |                   | t <sub>CD</sub>   | —   | 400              | 550  | ns    |
| Receive data setup from RCLK | Mode 1            | t <sub>RDS</sub>  | 60  | 70               | —    | ns    |
|                              | Modes 2, 3, and 4 | t <sub>RDS</sub>  | 30  | 45               | —    | ns    |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

**Table 10. RCLK/Start-of-Frame Timing**

| Parameter                                   |                   | Symbol | Min | Typ <sup>1</sup> | Max | Units |
|---------------------------------------------|-------------------|--------|-----|------------------|-----|-------|
| Receive data hold from RCLK                 | Mode 1            | tRDH   | 10  | 20               | —   | ns    |
|                                             | Modes 2, 3, and 4 | tRDH   | 30  | 45               | —   | ns    |
| RCLK shut off delay from CD assert (Mode 3) |                   | tsws   | —   | ±100             | —   | ns    |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

**Table 11. RCLK/End-of-Frame Timing**

| Parameter                                    | Type                 | Sym    | Mode 1 | Mode 2 | Mode 3    | Mode 4 | Units |
|----------------------------------------------|----------------------|--------|--------|--------|-----------|--------|-------|
| RCLK after CD off                            | Min                  | tRC    | 5      | 1      | —         | 5      | BT    |
| Rcv data through-put delay                   | Max                  | tRD    | 400    | 375    | 375       | 375    | ns    |
| CD turn-off delay <sup>2</sup>               | Max                  | tCDOFF | 500    | 475    | 475       | 475    | ns    |
| Receive block out after TEN off <sup>3</sup> | Typical <sup>1</sup> | tIFG   | 5      | 50     | —         | —      | BT    |
| RCLK switching delay after CD off            | Typical <sup>1</sup> | tswe   | —      | —      | 120 (±80) | —      | ns    |

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.  
2. CD Turnoff delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.  
3. Blocking of Carrier Detect is disabled during full duplex operation.

**Table 12. Transmit Timing**

| Parameter                  | Symbol | Minimum | Typical <sup>1</sup> | Maximum | Units |
|----------------------------|--------|---------|----------------------|---------|-------|
| TEN setup from TCLK        | tEHCH  | 22      | —                    | —       | ns    |
| TXD setup from TCLK        | tDSCH  | 22      | —                    | —       | ns    |
| TEN hold after TCLK        | tCHEL  | 5       | —                    | —       | ns    |
| TXD hold after TCLK        | tCHDU  | 5       | —                    | —       | ns    |
| Transmit start-up delay    | tSTUD  | —       | 350                  | 450     | ns    |
| Transmit through-put delay | tTPD   | —       | 338                  | 350     | ns    |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

**Table 13. Miscellaneous Timing**

| Parameter                                  | Symbol | Minimum | Typical <sup>1</sup> | Maximum | Units |
|--------------------------------------------|--------|---------|----------------------|---------|-------|
| COL (SQE) Delay after TEN off <sup>2</sup> | tsQED  | 0.65    | —                    | 1.6     | µs    |
| COL (SQE) Pulse Duration <sup>2</sup>      | tsQEP  | 500     | —                    | 1500    | ns    |
| Power Down recovery time                   | tPDR   | —       | 25                   | —       | ms    |

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.  
2. When SQE is enabled (DSQE is Low).

## 4.1 Timing Diagrams for Mode 1(MD1 = Low, MD0 = Low)

(Figure 11 through Figure 14)

Figure 11. Mode 1 RCLK/Start-of-Frame Timing

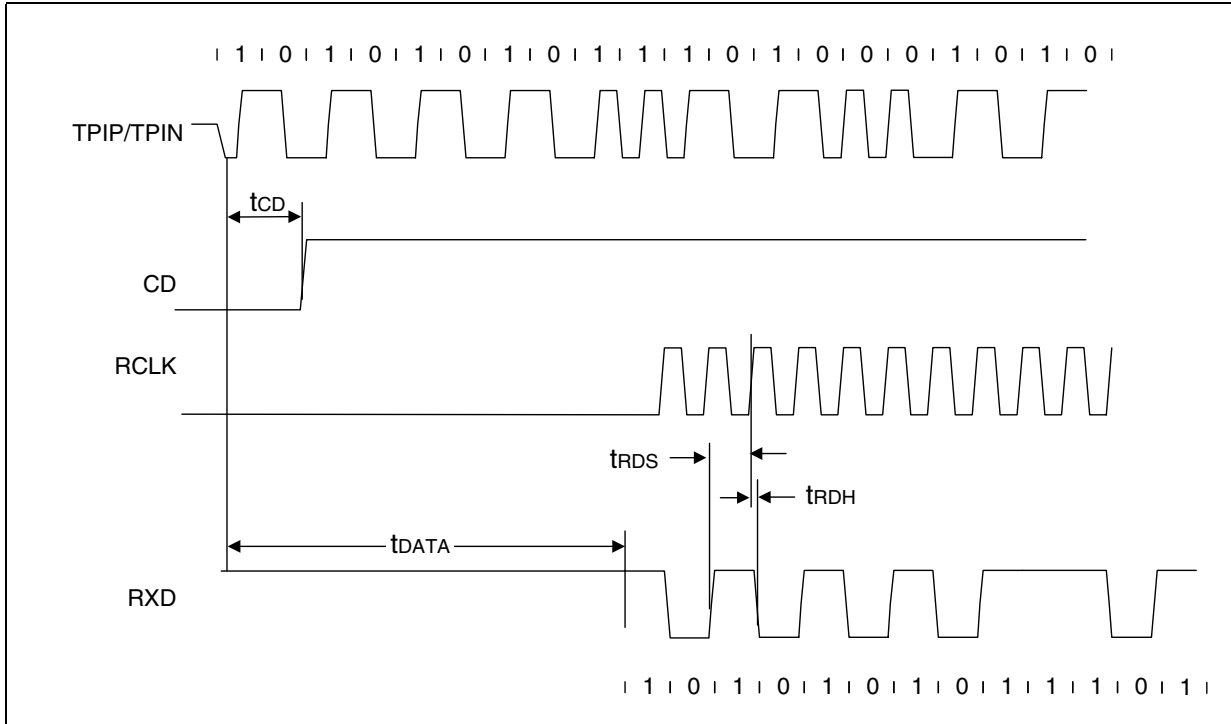


Figure 12. Mode 1 RCLK/End-of-Frame Timing

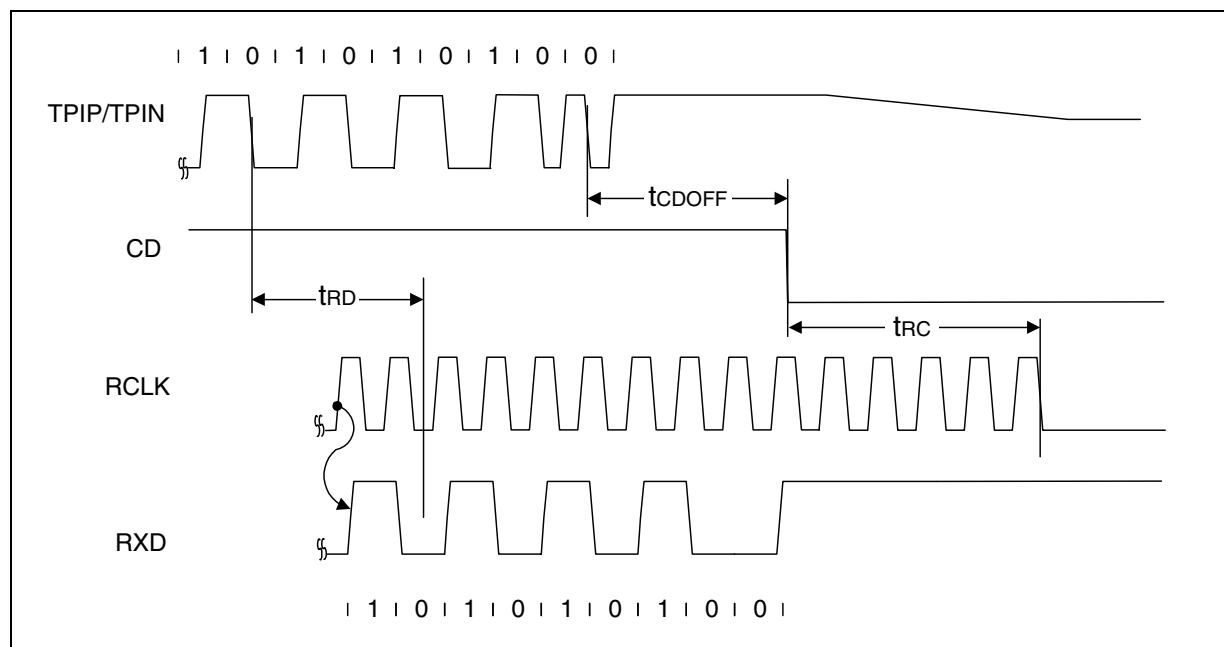


Figure 13. Mode 1 Transmit Timing

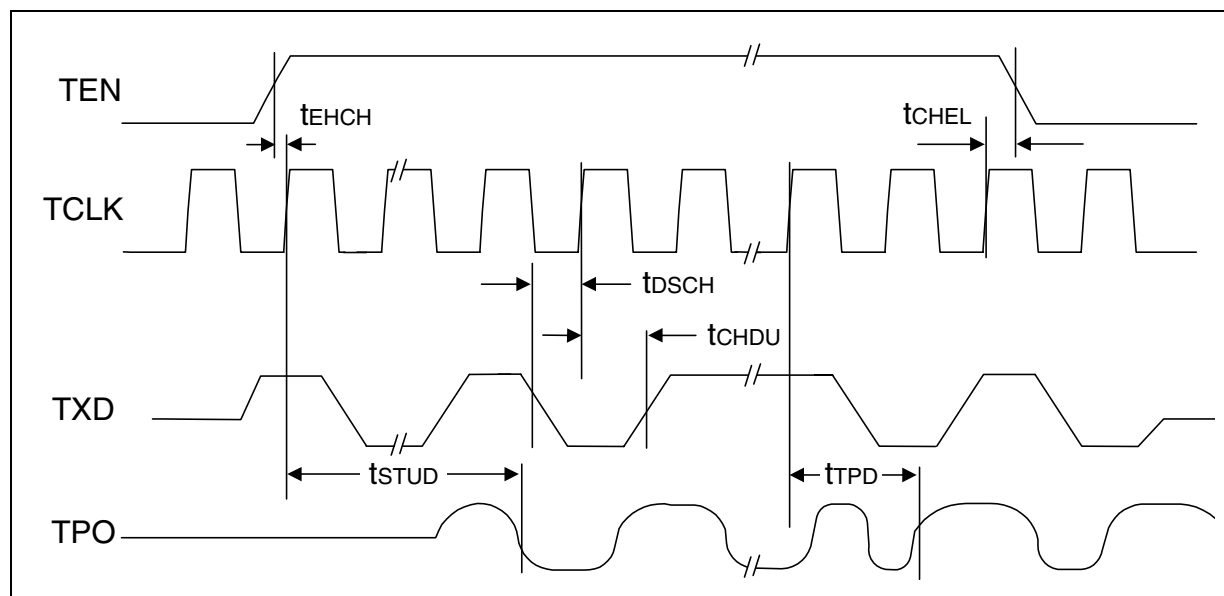
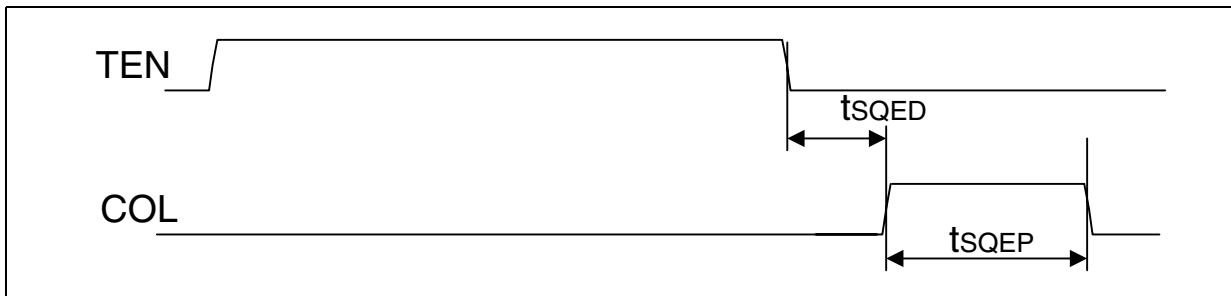


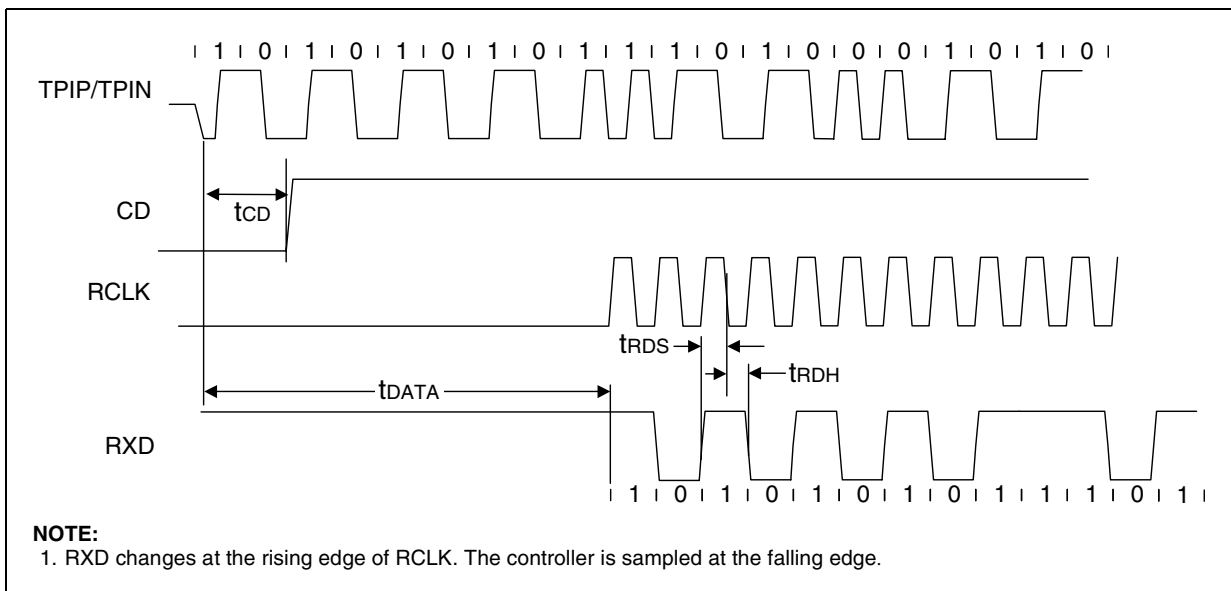
Figure 14. Mode 1 COL Output Timing



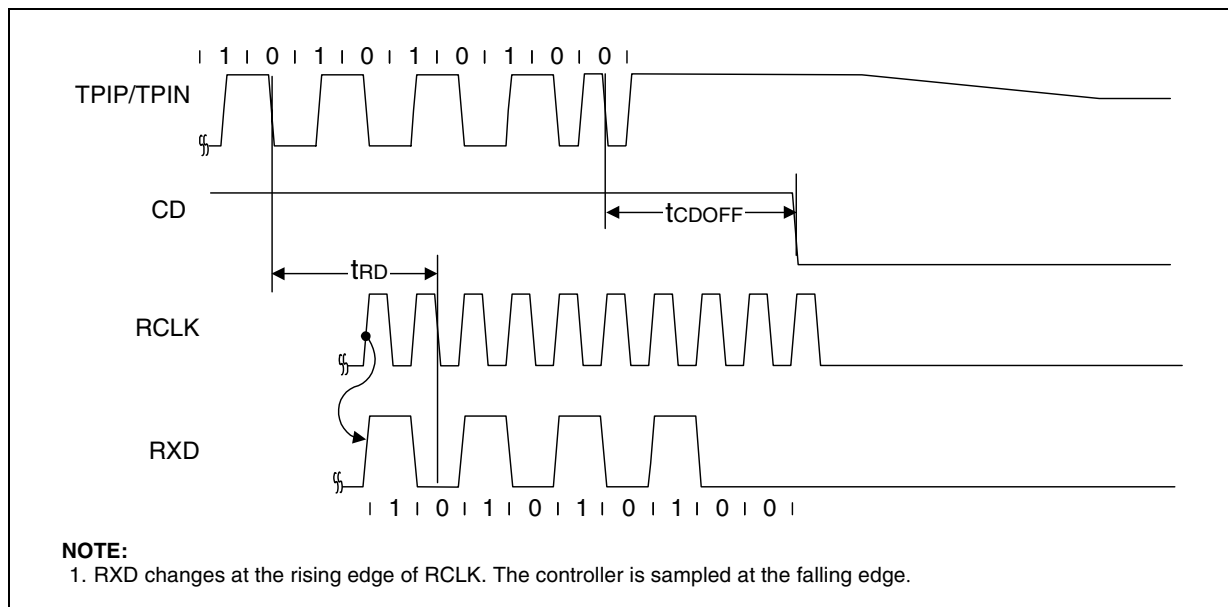
## 4.2 Timing Diagrams for Mode 2 (MD1=Low, MD0=High)

(Figure 15 through Figure 18)

Figure 15. Mode 2 RCLK/Start-of-Frame



### Figure 16. Mode 2 RCLK/End-of-Frame Timing



### Figure 17. Mode 2 Transmit Timing

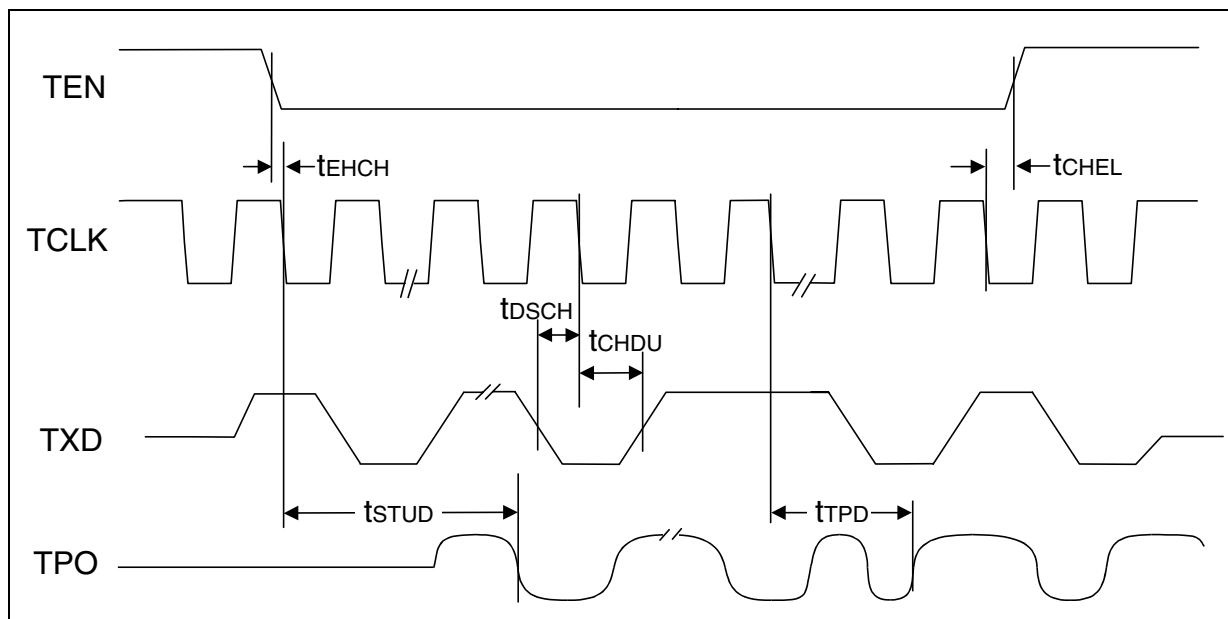
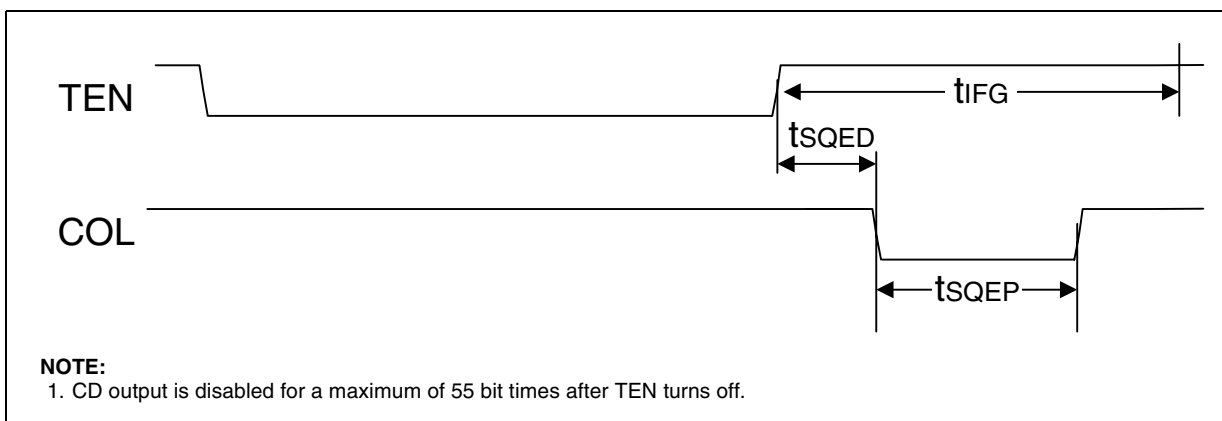


Figure 18. Mode 2 COL Output Timing



## 4.3 Timing Diagrams for Mode 3 (MD1 = High, MD0 = Low)

(Figure 19 through Figure 22)

Figure 19. Mode 3 RCLK/Start-of-Frame Timing

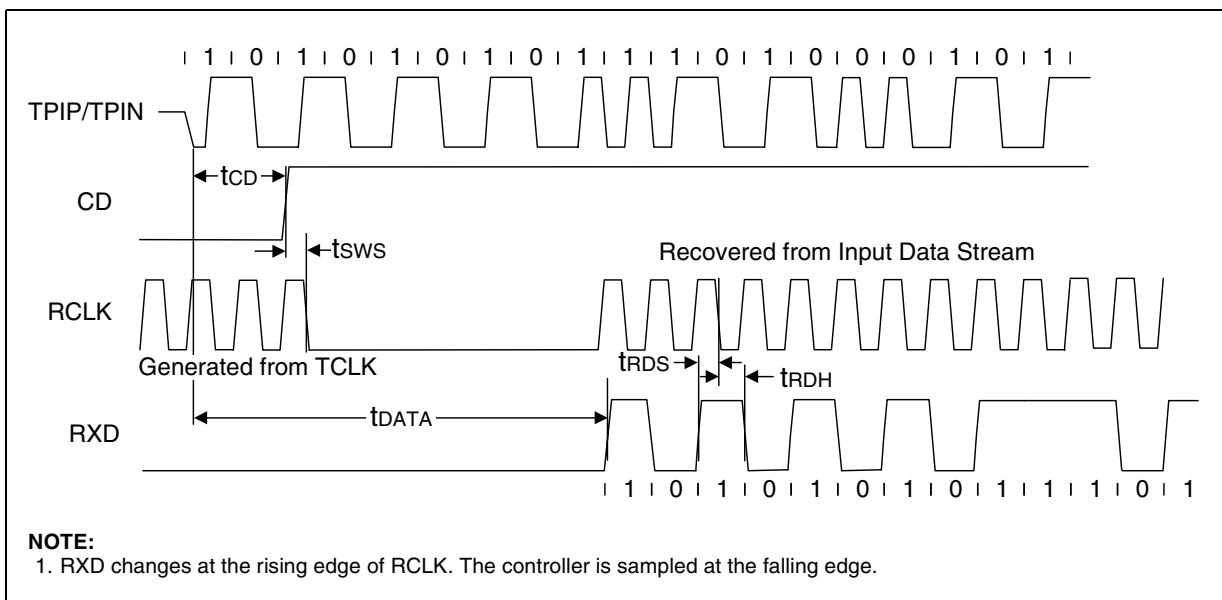


Figure 20. Mode 3 RCLK/End-of-Frame Timing

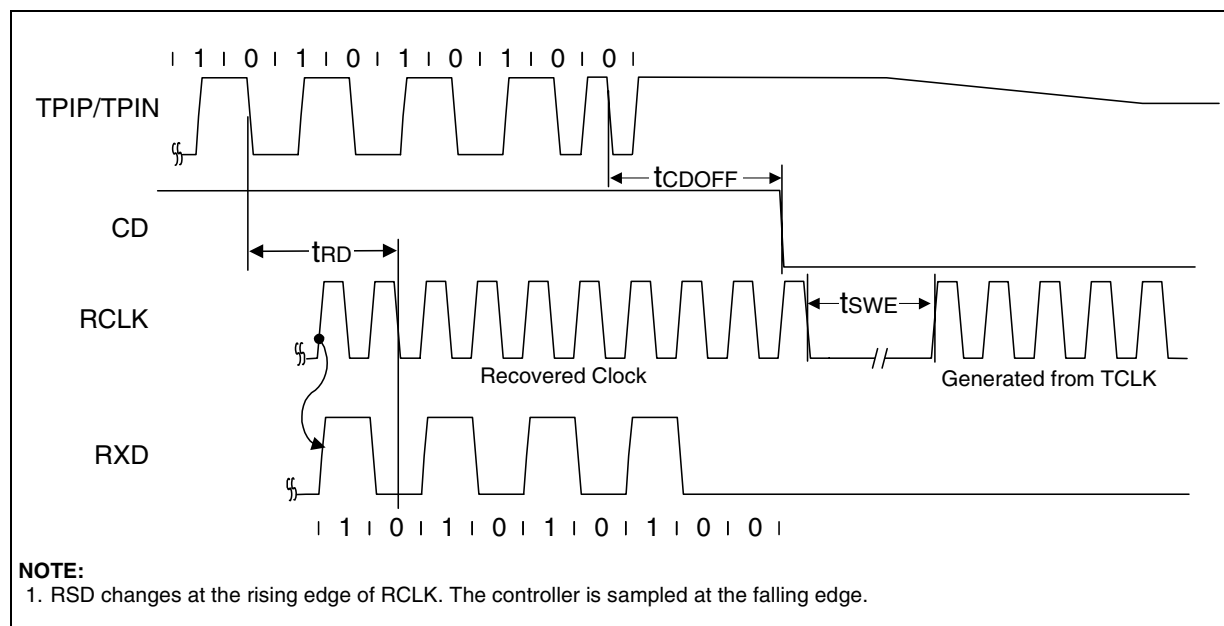


Figure 21. Mode 3 Transmit Timing

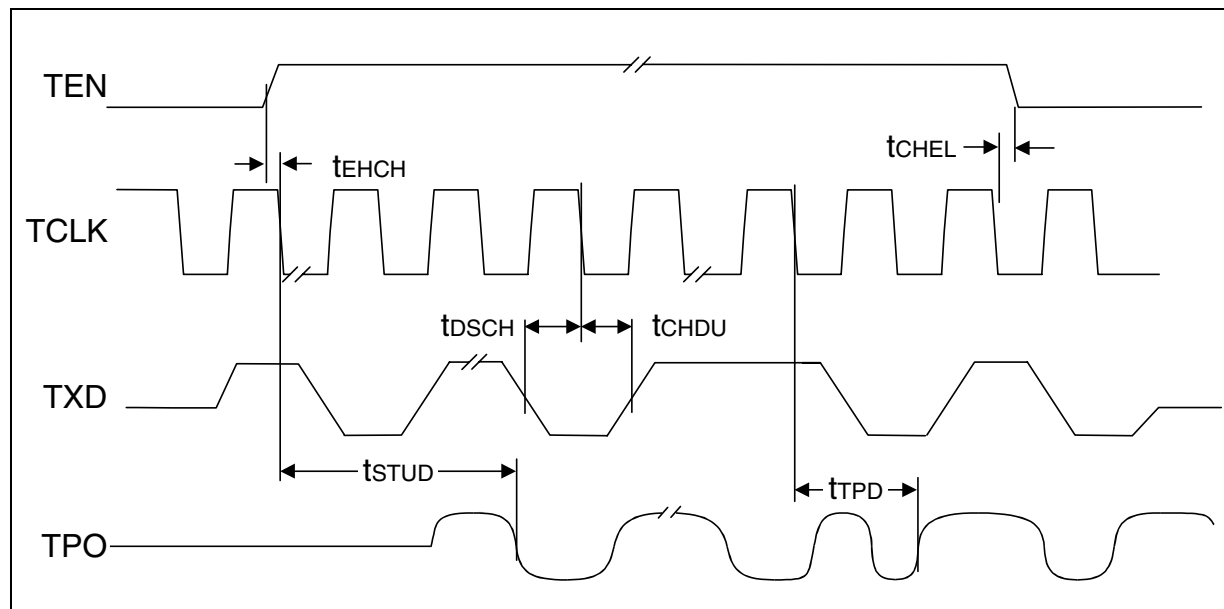
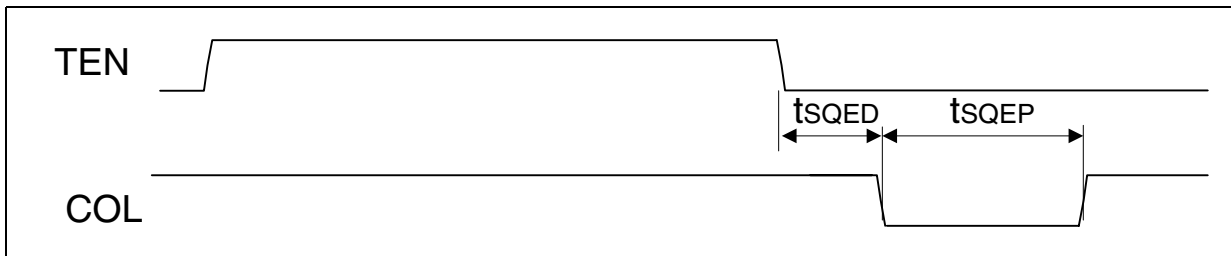


Figure 22. Mode 3 COL Output Timing



## 4.4 Timing Diagrams for Mode 4 (MD1 = High, MD0 = High)

(Figure 23 through Figure 26)

Figure 23. Mode 4 RCLK/Start-of-Frame Timing

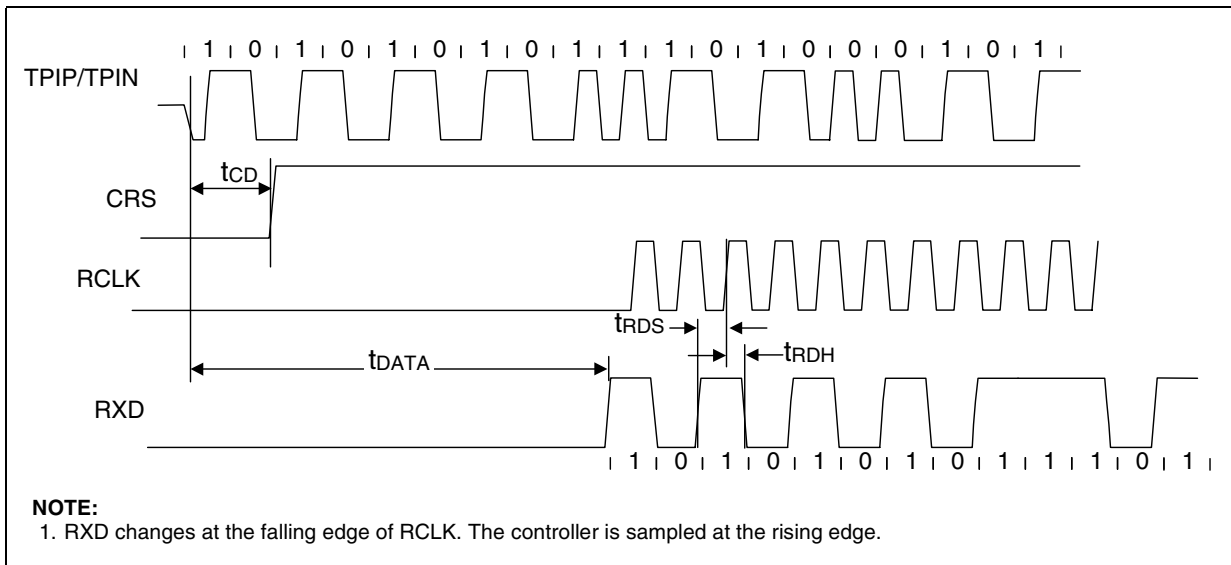


Figure 24. Mode 4 RCLK/End-of-Frame Timing

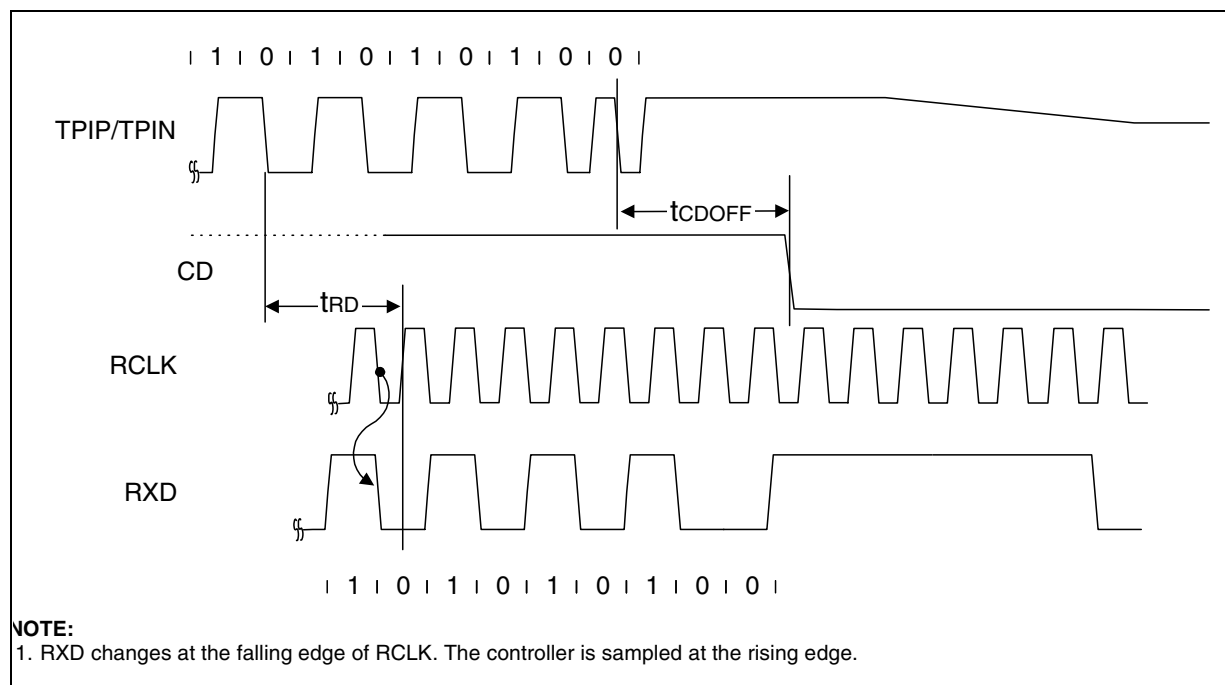


Figure 25. Mode 4 Transmit Timing

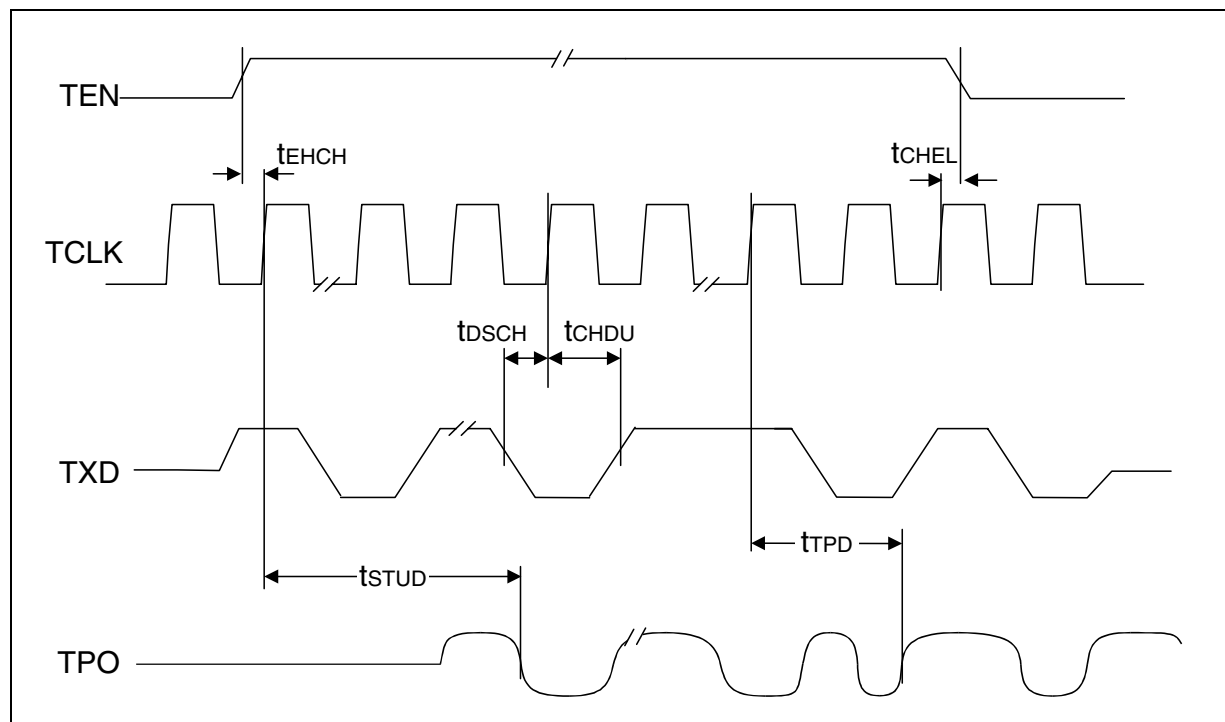
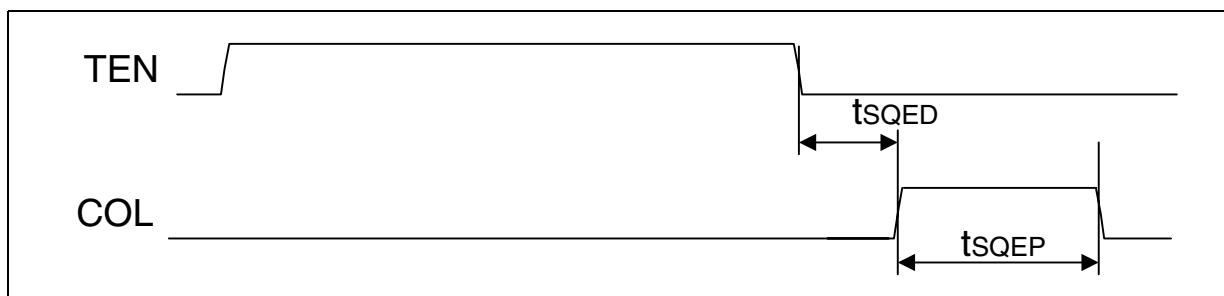


Figure 26. Mode 4 COL Output Timing



# 5.0 Mechanical Specifications

Figure 27. LXT905PC Package Specifications

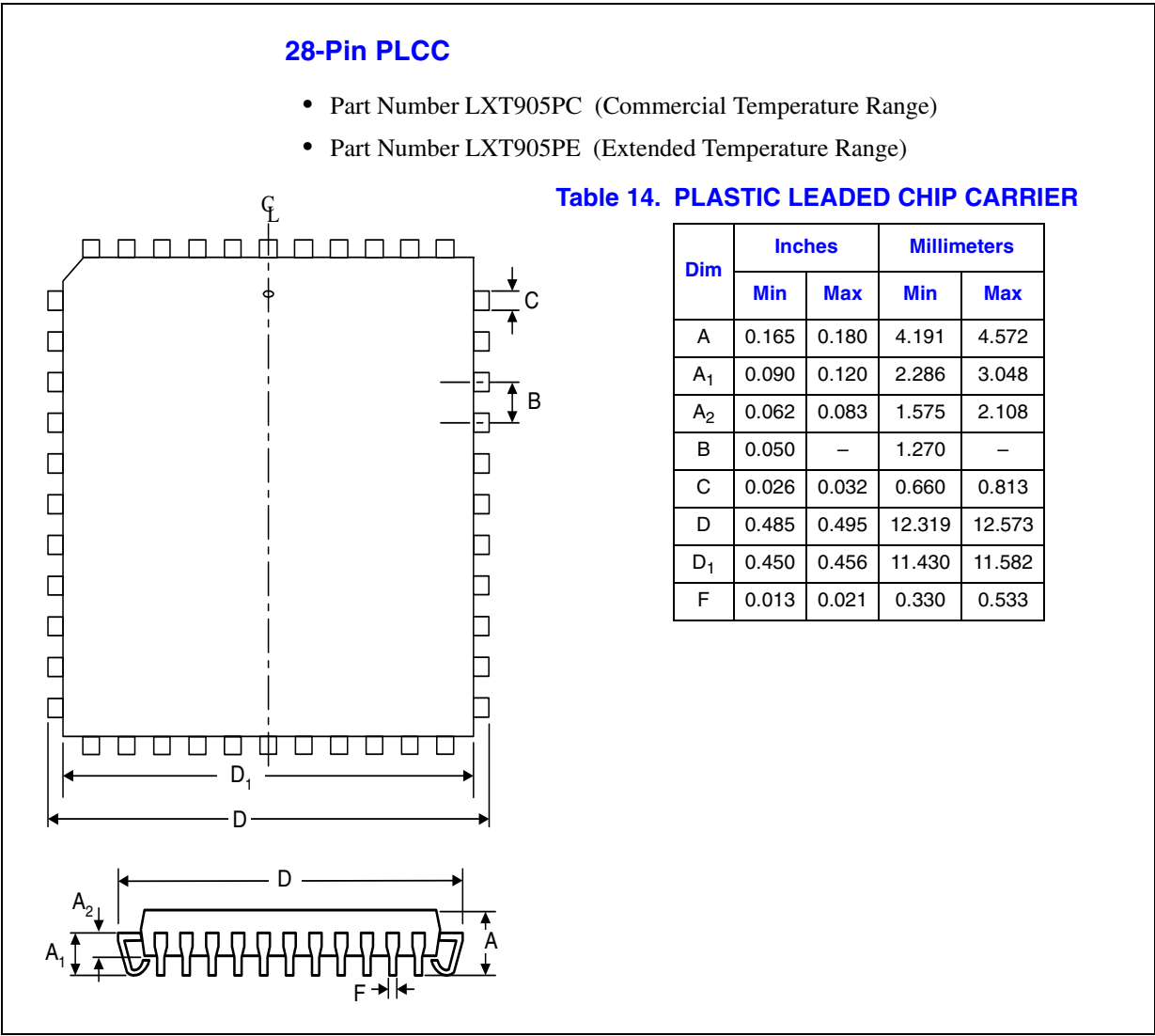


Figure 28. LXT905LC Package Specifications

### 32-Pin LQFP

- Part Number LXT905LC (Commercial Temperature Range)
- Part Number LXT905LE (Extended Temperature Range)

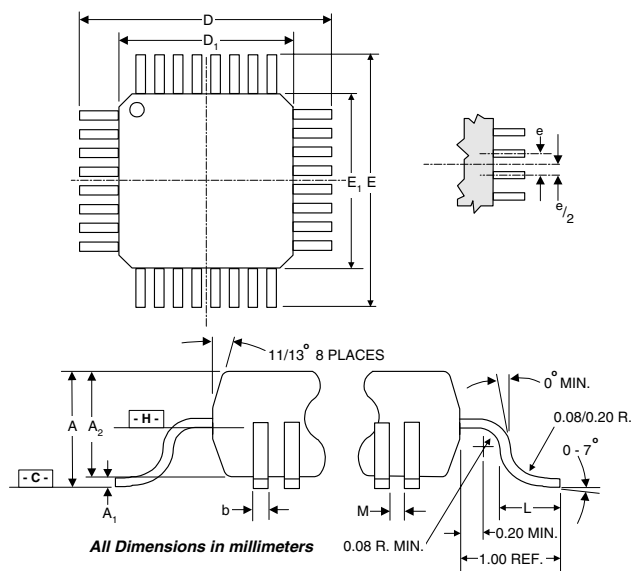


Table 15. QUAD FLAT PACKAGE

| Dim.           | All Dimensions in millimeters |      |      |         |
|----------------|-------------------------------|------|------|---------|
|                | Min.                          | Typ. | Max. | Notes   |
| A              | ---                           | ---  | 1.60 |         |
| A <sub>1</sub> | 0.05                          | 0.10 | 0.15 |         |
| A <sub>2</sub> | 1.35                          | 1.40 | 1.4  |         |
| D              | 9.00 BSC.                     |      |      | 5       |
| D <sub>1</sub> | 7.00 BSC.                     |      |      | 6, 7, 8 |
| E              | 9.00 BSC                      |      |      | 5       |
| E <sub>1</sub> | 7.00 BSC                      |      |      | 6, 7, 8 |
| L              | 0.45                          | 0.60 | 0.75 |         |
| M              | 0.15                          | ---  | ---  |         |
| b              | 0.30                          | 0.37 | 0.45 | 9       |
| e              | 0.80 BSC.                     |      |      |         |

#### NOTES:

1. All dimensions are in millimeters.
2. This package conforms to JEDEC publication 95 registration MO-136, variation BC.
3. Datum plane -H- located at mold parting line and is coincident with leads where leads exit plastic body at bottom of parting line.
4. Measured at seating plane -C-.
5. Measured at datum plane -H-.
6. Dimensions D<sub>1</sub> and E<sub>1</sub> do not include mold protrusion. Allowable mold protrusion is 0.254 mm.
7. Package top dimensions are smaller than bottom dimensions. Top of package will not overhang bottom of package.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion is no more than 0.08 mm.

