National Semiconductor

microCMOS

NSC858 Universal Asynchronous Receiver/Transmitter

November 1995

General Description

The NSC858 is a CMOS programmable Universal Asynchronous Receiver/Transmitter (UART). It has an on chip programmable baud rate generator. The UART, which is fabricated using microCMOS silicon gate technology, functions as a serial receiver/transmitter interface for your microcomputer system.

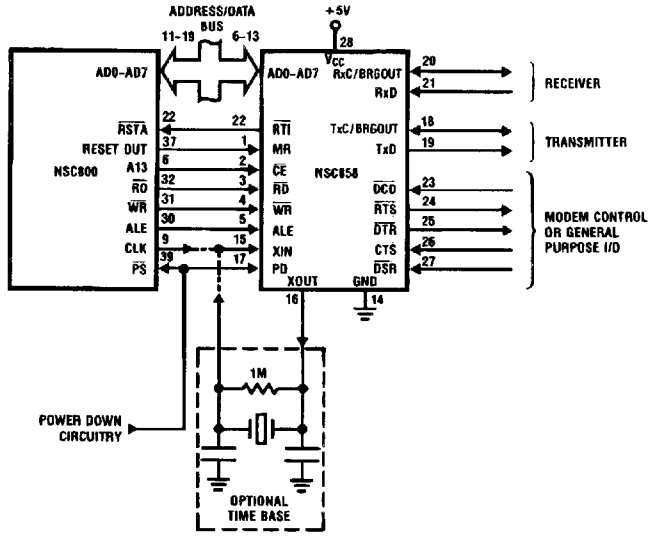
The transmitter converts parallel data from the CPU to serial form and shifts it out in the standard asynchronous communication data format. Appropriate start, parity, and stop bits are added to the outgoing serial stream. Incoming serial data is converted to parallel form by the receiver. The receiver checks incoming data for errors (parity, overrun, framing or break interrupt) and then converts it from serial to parallel for transfer to the CPU. Five pins on the chip are available for modem control functions or general purpose I/O.

The NSC858 has a programmable baud generator that is capable of dividing the timing reference clock input by divisors of 1 to ($2^{16}-1$), and producing a 1X, 16X, 32X, 64X clock for driving the transmitter and/or receiver logic. Both the transmitter and receiver can either be driven by an external clock or the internal baud rate generator. The NSC858 has an interrupt system that can be tailored to the user's requirements. In addition to the CMOS power consumption levels there are hardware and software power down modes which further reduce power consumption levels.

Features

- Maximum baud rate 256k BPS (16X), 1M BPS (1X)
- Programmable baud rate generator
- Double buffered receiver and transmitter
- Independently configured receiver and transmitter
  - 5-, 6-, 7-, 8-bit characters
  - Odd, even, force high, force low, or no parity
  - 1, 1½, 2 stop bits
- Five bits modem I/O or general purpose I/O (3 input, 2 output)
- Programmable auto enables for $\overline{CTS}$ and $\overline{DCD}$
- Local and remote loopback diagnostics
- False start bit detection
- Break condition detection and generation
- Program polled, or interrupt driven operation
  - 8 maskable status conditions for receiver and transmitter interrupt
  - 4 maskable status conditions for modem interrupt
- Variable power supply (2.4V–6.0V)
- Low power consumption with software and hardware power down modes
- 8-bit multiplexed address/data bus directly compatible with NSC800™

System Configuration



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RRD-B30M115/Printed in U. S. A.

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1.0 Absolute Maximum Ratings

(Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Maximum V_{CC}	7V
Power Dissipation	1W
Lead Temp. (Soldering, 10 seconds)	300°C

2.0 Operating Conditions $V_{CC}=5V\pm10\%$

Ambient Temperature	
Industrial	−40°C to +85°C
Commercial	0°C to +70°C

3.0 DC Electrical Characteristics V_{CC} = 5V±10%, GND = 0V, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logical 1 Input Voltage		0.8 V_{CC}		V_{CC}	V
V_{IL}	Logical 0 Input Voltage		0		0.2 V_{CC}	V
V_{HY}	Hysteresis at RESET IN Input	$V_{CC}=5V$	0.25	0.5		V
V_{OH1}	Logical 1 Output Voltage	$I_{OUT}=-1.0$ mA	2.4			V
V_{OH2}	Logical 1 Output Voltage	$I_{OUT}=-10\ \mu A$	$V_{CC}-0.5$			V
V_{OL1}	Logical 0 Output Voltage	$I_{OL}=2$ mA except X_{OUT}	0		0.4	V
V_{OL2}	Logical 0 Output Voltage	$I_{OUT}=10\ \mu A$	0		0.1	V
I_{IL}	Input Leakage Current	$0\le V_{IN}\le V_{CC}$	−10.0		10.0	μA
I_{OL}	Output Leakage Current	$0\le V_{IN}\le V_{CC}$	−10.0		10.0	μA
I_{CC}	Active Supply Current	T_A = 25°C		2	10	mA
I_{HPD}	Current Hardware Power Down	Pin $\overline{PD}=0$, No Resistive Output Loads, $V_{IN}=0V$ or $V_{IN}=V_{CC}$, T_A = 25°C		100		μA
I_{SPD}	Current Software Power Down	Power Down Reg Bit 0 = 1, No Resistive Output Loads, $V_{IN}=0V$ or $V_{IN}=V_{CC}$, T_A = 25°C		300		μA
C_{IN}	Input Capacitance			6	10	pF
C_{OUT}	Output Capacitance			8	12	pF
V_{CC}	Power Supply Voltage	(Note 2)	2.4	5	6	V

Note 1: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

Note 2: Operation at lower power supply voltages will reduce the maximum operating speed. Operation at voltages other than 5V ±10% is guaranteed by design, not tested.

AC Testing Input/Output Waveform

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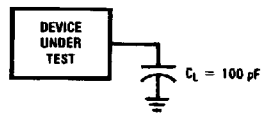
AC Testing Load Circuit



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4.0 AC Electrical Characteristics V_{CC} = 5V±10%, GND = 0V, C_L = 100 pF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BUS						
t_{AS}	Address 0–7 Set-Up Time		40			ns
t_{AH}	Address 0–7 Hold Time		30			ns
t_{ALE}	ALE Strobe Width (High)		100			ns
t_{ARW}	ALE to Read or Write Strobe		75			ns
t_{CRW}	Chip Enable to Read or Write		110			ns
t_{RD}	Read Strobe Width		250			ns
t_{DDR}	Data Delay from Read			180	200	ns
t_{RDD}	Data Bus Disable				75	ns
t_{CH}	Chip Enable Hold After Read or Write		60			ns
t_{RWA}	Read or Write to Next ALE		45			ns
t_{WR}	Write Strobe Width		200	250		ns
t_{DS}	Data Set-Up Time		100			ns
t_{DH}	Data Hold Time		75			ns
MODEM						
t_{MD}	$\overline{WR}$ Command Reg. to Modem Outputs Delay			180		ns
t_{SIM}	Delay to Set Interrupt from Modem Input			200		ns
t_{RIM}	Delay to Reset Modem Status Interrupt from $\overline{RD}$			240		ns
t_{SMI}	$\overline{WR}$ to Status Mask Reg., Delay to $\overline{RTI}$				230	ns
POWER DOWN						
t_{PCS}	Power Down to All Clocks Stopped			1	2	$t_{BIT} + t_{XC}$
t_{PCR}	Power Down Removed to Clocks Running			1	2	$t_{BIT} + t_{XC}$
t_{PXS}	Power Down Removed to XTAL Oscillator Stable	When Using On Chip Inverter for Oscillator Circuit		100		ms
t_{PSE}	Power Down Set-Up to $\overline{RD}$ or $\overline{WR}$ Edge		160	260		ns
t_{EPI}	$\overline{WR}$ or $\overline{RD}$ Edge Following $\overline{PD}$ to Internal Signals	Enable or Disable		100		ns
BAUD GENERATOR						
t_{XH}	XTAL In High		100			ns
t_{XL}	XTAL In Low		100			ns
f_{BRC}	Baud Rate Clock Input Frequency				4.1	MHz
t_{BD1}	Baud Out Delay ÷ 1			160		ns
t_{BD2}	Baud Out Delay ÷ 2			200		ns
t_{BD3}	Baud Out Delay ÷ 3			200		ns
t_{BDN}	Baud Out Delay ÷ N > 3			200		ns
t_{XC}	Baud Clock Cycle	$t_{XC} = \frac{1}{f_{BRC}}$	243			ns

4.0 AC Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
TRANSMITTER						
t_{TCD}	TxD Delay from $\overline{TxC}$	External Clock		275		ns
		Internal Clock		140		ns
t_{TXC}	Cycle Time $\overline{TxC}$	16X, 32X, 64X Clock Factor	243			ns
		1X Clock Factor	1000			ns
t_{TCH}	$\overline{TxC}$ High		100			ns
t_{TCL}	$\overline{TxC}$ Low		100			ns
t_{HRI}	$\overline{WR}$ TxHR to Reset TxBE $\overline{RTI}$			260		ns
t_{HTS}	$\overline{WR}$ TxHR to TxD Start		2	3	4	t_{BIT}
t_{TSI}	Skew Start Bit to $\overline{RTI}$		−100	+20	+120	ns
t_{ETS}	Enable Tx to Start Bit		3	4	5	t_{BIT}
t_{BIT}[1]	One Bit Time	1X	1000			ns
		16X	3.88			μs
		32X	7.77			μs
		64X	15.55			μs
RECEIVER						
t_{RS}	RxD Set-Up	1X Clock Factor		160		ns
t_{RH}	RxD Hold	1X Clock Factor		100		ns
t_{RXC}	Cycle time $\overline{RxC}$	16X, 32X, 64X Clock Factor	243			ns
		1X Clock Factor	1000			ns
t_{RCH}	$\overline{RxC}$ High		100			ns
t_{RCL}	$\overline{RxC}$ Low		100			ns
t_{RRI}	$\overline{RD}$ to Reset $\overline{RTI}$			300		ns
t_{BIT}[1]	One Bit Time	1X	1000			ns
		16X	3.88			μs
		32X	7.77			μs
		64X	15.55			μs
t_{ERS}	Enable Rx to Correctly Detect Start Bit	All Clock Factors	2	3	4	t_{RXC}
t_{RNO}	Read RxHR Before Next Data; No OE		240			ns
t_{BI}	$\overline{RxC}$, Break to $\overline{RTI}$			340		
t_{REI}	Receiver Error Int			½ Clock Factor		t_{RXC}
t_{RDI}	Receiver Ready Int			$t_{REI}+1$		t_{RXC}
t_{RSI}	$\overline{RxC}$ to $\overline{RTI}$			300		ns
RESET TIMING						
t_{MR}	MR Pulse Width			100		ns
t_{RA}	MR to ALE if Valid $\overline{WR}$ or $\overline{RD}$ Cycle			100		ns

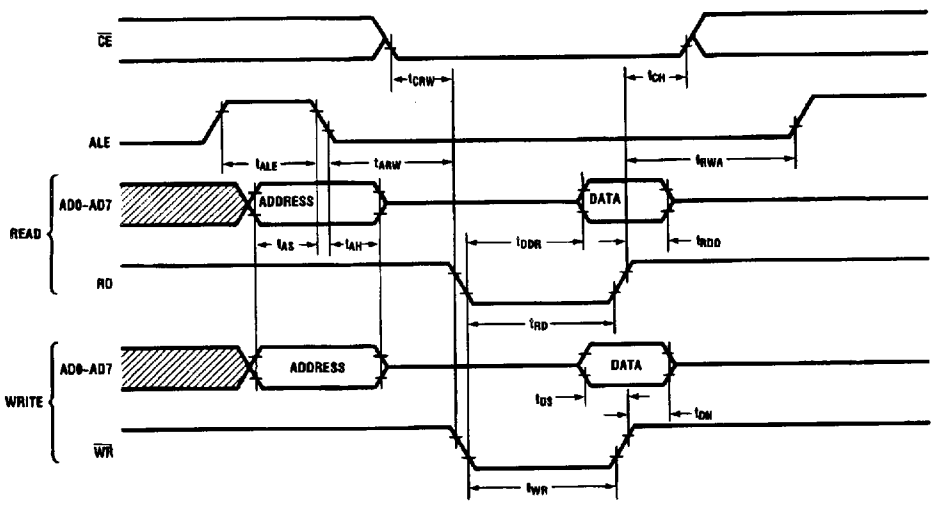
Note 1: $t_{BIT} = t_{TXC} \times$ Clock Factor (1, 16, 32, 64), transmitter

$t_{BIT} = t_{RXC} \times$ Clock Factor (1, 16, 32, 64), receiver

$$t_{BIT} = \frac{1}{\text{Baud Rate}}$$

5.0 Timing Waveforms

Read and Write Cycles



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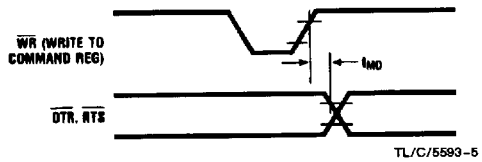
Note: The internal write is made inactive by either the next ALE or $\overline{CE}$ going invalid

Modem Timing



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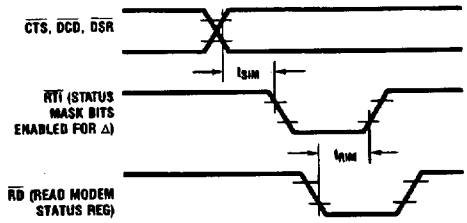

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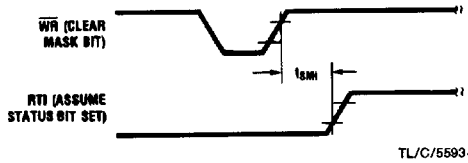

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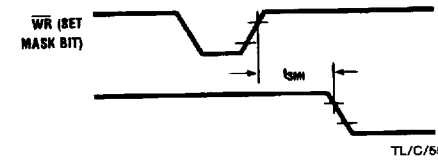

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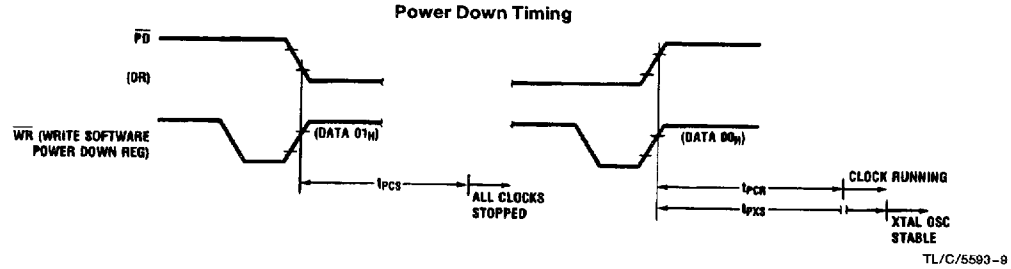
5.0 Timing Waveforms (Continued)

Power Down Timing



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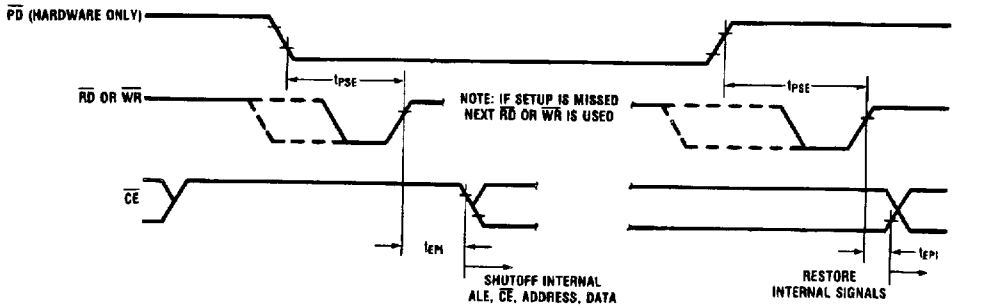

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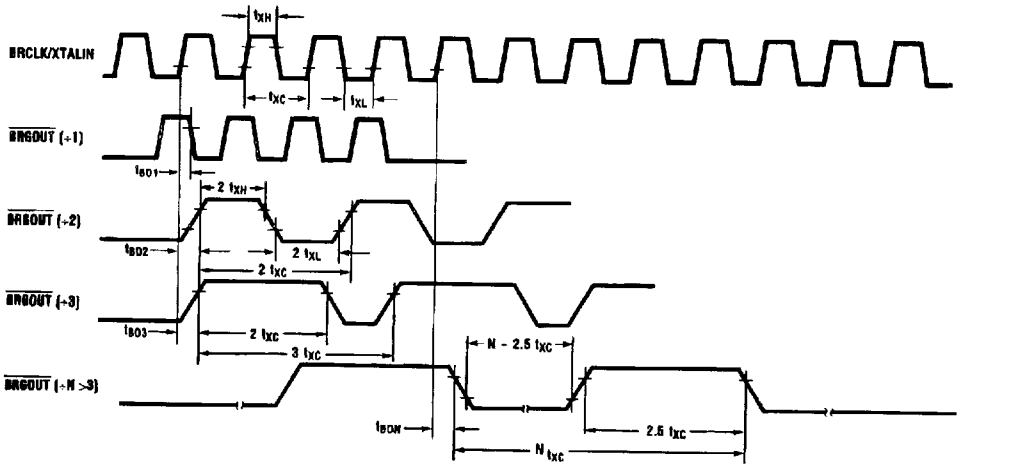
Baud Out Timing



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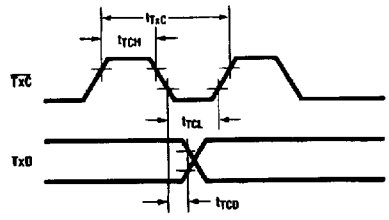
5.0 Timing Waveforms (Continued)

Transmitter Timing



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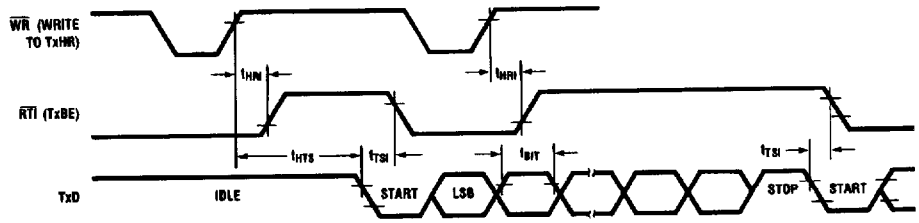

$$t_{BIT} = \frac{1}{\text{BAUD RATE}} = t_{TxC} \times \text{CLOCK FACTOR (1, 16, 32, 64)}$$

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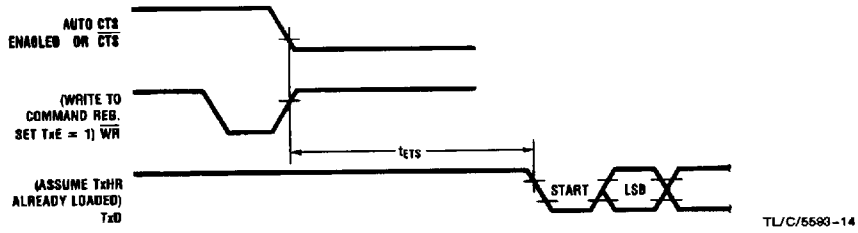
Note: The AC Timing Spec for $\overline{RTI}$ due to TXU or TBK will be published in the next data sheet.



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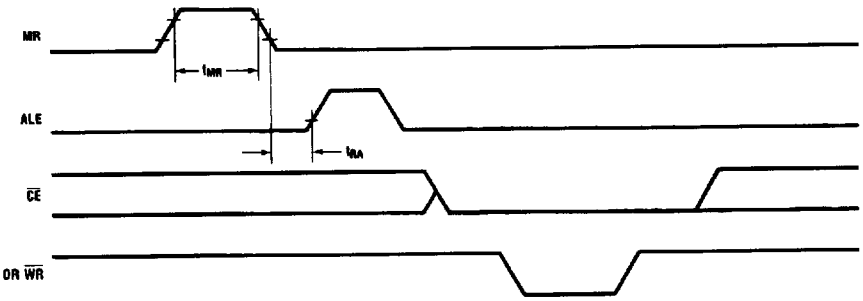
Reset Timing



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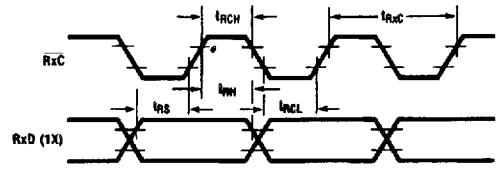
5.0 Timing Waveforms (Continued)

Receiver Timing



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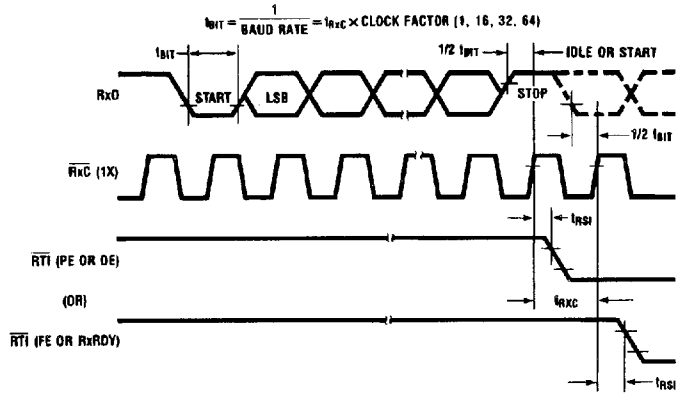

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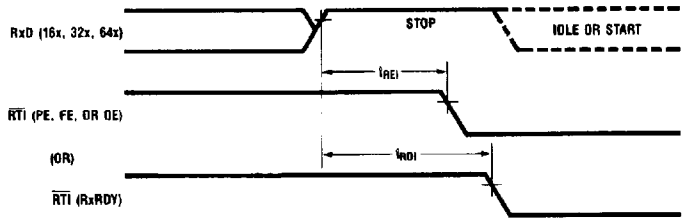

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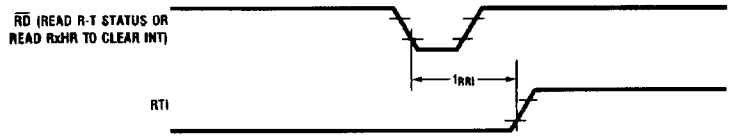

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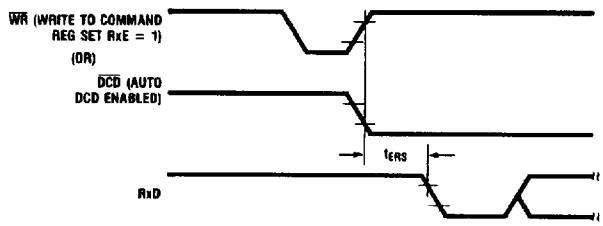
5.0 Timing Waveforms (Continued)

Receiver Timing (Continued)



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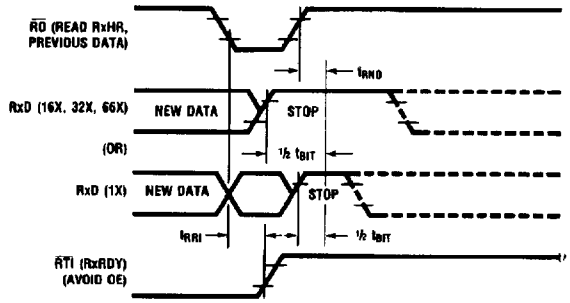

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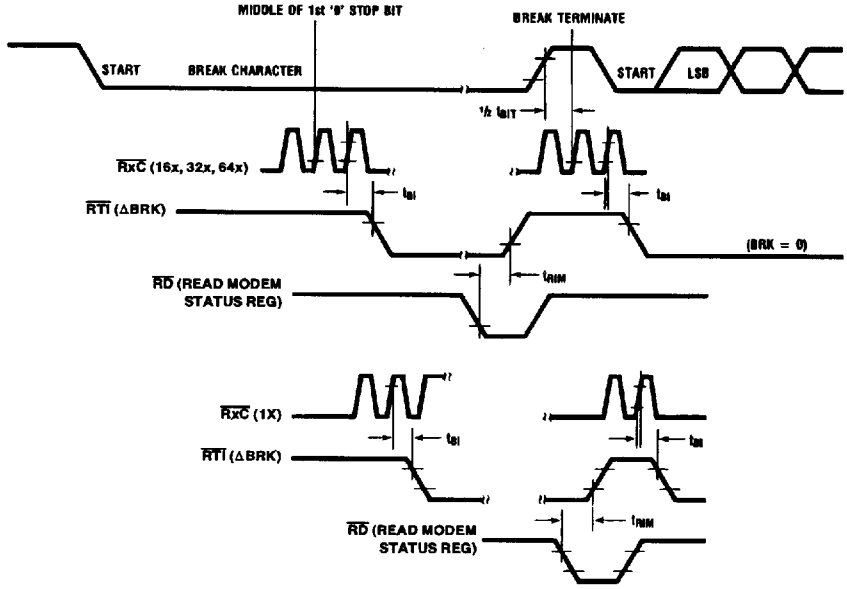

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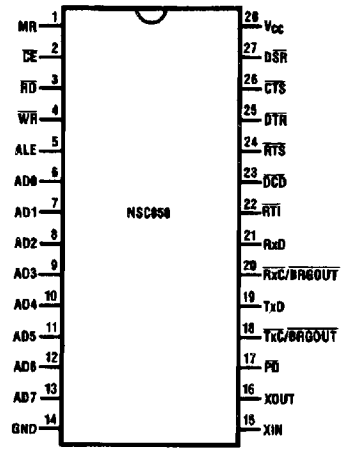
6.0 Connection Diagrams

Dual-In-Line Package



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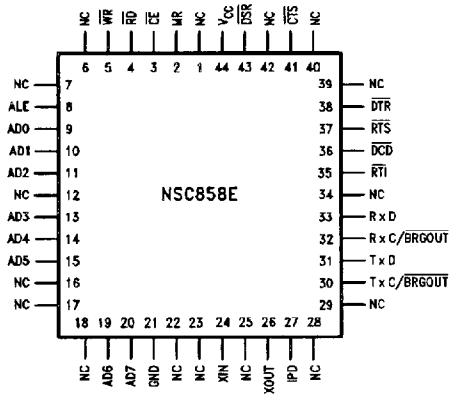
Top View

Order Number NSC858D or N
See NS Package D28C or N28B

Leadless Chip Carrier



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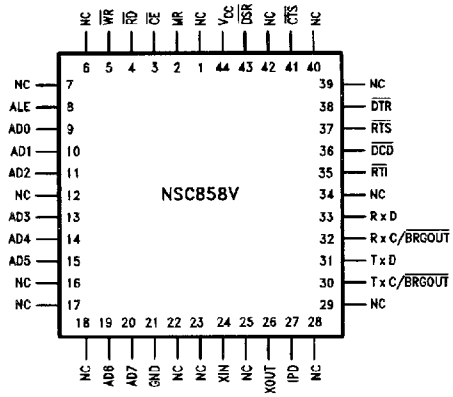
Top View

Order Number NSC858E
See NS Package Number E44A

Plastic Chip Carrier



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Top View

Order Number NSC858V
See NS Package Number V44A

7.0 Pin Descriptions

7.1 INPUT SIGNALS

Master Reset (MR): active high, Pin 1. This Schmitt trigger input has a 0.5V typical hysteresis. When high, the following registers are cleared: receiver mode, transmitter mode, global mode, R-T status (except for TxBE which is set to one), R-T status mask, modem mask, command (which disables receiver "Rx" and the transmitter "Tx"), power down, and receiver holding. In the modem status register, ΔCTS, ΔDCD, ΔDSR, BRK and ΔBRK are cleared.

Chip Enable ($\overline{CE}$): active low, Pin 2. Chip enable must be low during a valid read or write pulse in order to select the device. Chip enable is not latched.

Read ($\overline{RD}$): active low, Pin 3. While the chip is enabled the CPU latches data from the selected register on the rising edge of $\overline{RD}$.

Write ($\overline{WR}$): active low, Pin 4. While the chip is enabled it latches data from the CPU on the rising edge of $\overline{WR}$.

Address Latch Enable (ALE): negative edge sensitive, Pin 5. The negative edge (high to low) of ALE latches the address for the register select during a read or write operation.

7.0 Pin Descriptions (Continued)

Power Down ($\overline{PD}$): active low, Pin 17. When active it disables all internal clocks, shuts off the oscillator, clears RxE, TxE, and break control bits in the command register. All other registers retain their data. Unlike software power down, $\overline{PD}$ also disables the internal ALE, $\overline{CE}$, $\overline{RD}$, $\overline{WR}$, address and data paths for minimum power consumption. Registers cannot be accessed in hardware power down; they may be in software power down.

Receiver Data (RxD): Pin 21. This accepts serial data input from the communications link (peripheral device, modem, or data set). Serial data is received least significant bit (LSB) first. "Mark" is high (1), "space" is low (0).

Data Carrier Detect ($\overline{DCD}$): active low, Pin 23. Can be used as a modem or general purpose input. When this modem input is low it indicates that the data carrier has been detected by the modem or data set. The $\overline{DCD}$ signal is a modem control function input whose complement value can be tested by the CPU by reading bit 5 (DCD) of the modem status register. Bit 1 (ΔDCD) of the modem status register indicated whether the $\overline{DCD}$ input has changed state since the previous reading of the modem status register. $\overline{DCD}$ can also be programmed to become an auto enable for the receiver.

NOTE: Whenever the DCD bit of the modem status register changes state, an interrupt is generated if the ΔDCD mask and the DSCHG mask bits are set.

Clear to Send ($\overline{CTS}$): active low, Pin 26. Can be used as a modem or a general purpose input. The $\overline{CTS}$ inputs complement can be tested by the CPU by reading bit 4 (CTS) of the modem status register. Bit 0 (ΔCTS) of the modem status register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the modem status register. $\overline{CTS}$ can be programmed to automatically enable the transmitter. Note: Whenever the CTS bit of the modem status register changes state, an interrupt is generated if the ΔCTS mask and the DSCHG mask bits are set.

Data Set Ready ($\overline{DSR}$): active low, Pin 27. Can be used as a modem or a general purpose input. When this modem input is low it indicates that the modem or data set is ready to establish the communication link and transfer data with the NSC858. The $\overline{DSR}$ is a modem-control function input whose complement value can be tested by the CPU by reading bit 6 (DSR) of the modem status register. Bit 2 (ΔDSR) of the modem status register indicates whether the ($\overline{DSR}$) input has changed state since the previous reading of the modem status register.

NOTE: Whenever the DSR bit of the modem status register changes state, an interrupt is generated if ΔDSR mask and the DSCHG mask bits are set.

Power (V_{CC}): Pin 28. +5V supply.

Ground (GND): Pin 14. Ground (0V) supply.

7.2 OUTPUT SIGNALS

Transmit Data (TxD): Pin 19: Composite serial data output to the communication link (peripheral, modem or data set) least significant bit first. The TxD signal is set to the marking (logic 1) state upon a master reset. In hardware or software power down this pin will always be a one.

Receiver-Transmitter Interrupt ($\overline{RTI}$): active low, Pin 22. Goes low when any R-T status register bit and its corresponding mask bit are set. This bit can change states during either hardware or software power down due to a change in modem status information.

Request to Send ($\overline{RTS}$): active low, Pin 24. Can be used as a modem or a general purpose output. When this modem output is low it informs the modem or data set that the NSC858 is ready to transmit data. The $\overline{RTS}$ output or general purpose output signal can be set to an active low by programming bit 6 of the command register with a 1. The $\overline{RTS}$ signal is set high upon a master reset operation. During remote loopback $\overline{RTS}$ signal reflects the complement of bit 6 of the command register. During local loopback the $\overline{RTS}$ signal is forced to its inactive state (high). $\overline{RTS}$ cannot change states during hardware power down; it can during software power down.

Data Terminal Ready ($\overline{DTR}$): active low, Pin 25. Can be used as a modem or general purpose output. When this modem output is low it informs the modem or data set that the NSC858 is ready to communicate. The $\overline{DTR}$ output or the general purpose output signal can be set to an active low by programming bit 7 of the command register with a 1. The $\overline{DTR}$ signal is set high upon a master reset operation. During remote loopback $\overline{DTR}$ signal reflects the complement of bit 7 of the command register. During local loopback the $\overline{DTR}$ signal is forced to its inactive state (high). $\overline{DTR}$ signal cannot change state during hardware power down; it can during software power down.

7.3 INPUT/OUTPUT SIGNALS

Address/Data Bus (AD0–AD7): Pins 6–13. The multiplexed bidirectional address/data bus, AD0–AD7 pins, are in the high impedance state when the NSC858 is not selected or whenever it is in hardware power down. AD0–AD3 are latched on the trailing edge of ALE, providing the four address inputs. The rising edge of the $\overline{WR}$ input enables 8 bits to be written in, through AD0–AD7, to the addressed register. $\overline{RD}$ input enables 8 bits to be read from a register out through AD0–AD7.

Transmitter Clock/Baud Rate Generator Output ($\overline{TxC}$/$\overline{BRGOUT}$): Pin 18. If the transmitter is programmed for an external clock, $\overline{TxC}$ is an input. If the transmitter is programmed for an internal clock, then the Baud Rate Generator is used for the transmitter, and it is output at $\overline{TxC}$/$\overline{BRGOUT}$. In either case, $\overline{TxC}$/$\overline{BRGOUT}$ signal is running at 1X, 16X, 32X, 64X the data rate, as selected by the clock factor. If this pin is used as an output it will be set to a zero (0) in both hardware and software power down.

Receiver Clock/Baud Rate Generator Output ($\overline{RxC}$/$\overline{BRGOUT}$): Pin 20. If the receiver is programmed for an external clock, RxC is an input. If the receiver is programmed for an internal clock, the Baud Rate Generator is used for the receiver, and it is output at $\overline{RxC}$/$\overline{BRGOUT}$. In either case, $\overline{RxC}$/$\overline{BRGOUT}$ signal is running at 1X, 16X, 32X, 64X, the data rate as selected by the clock factor. If this pin is programmed as an output it will be set to one (1) in both hardware and software power down.

Crystal (XIN, XOUT): Pins 15, 16. These two pins connect the main timing reference. A crystal network can be connected across these two pins, or a square wave can be driven into XIN with XOUT left floating. In hardware and software power down XOUT is set to a 1. Ground XIN when using both RxC and TxC to supply external clocks to the UART.

8.0 Block Diagram

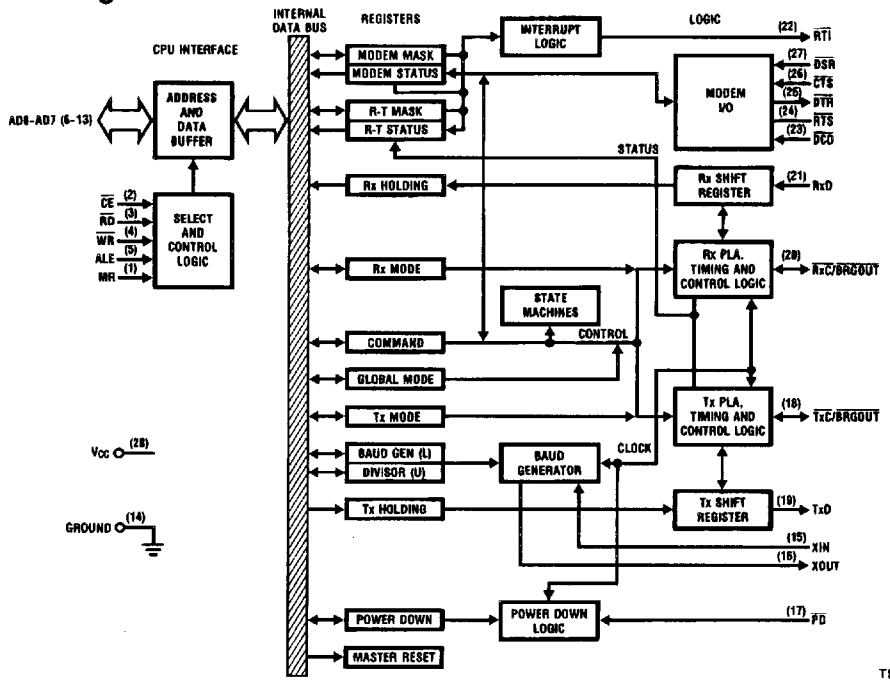

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FIGURE 1. NSC858 Functional Block Diagram

9.0 Registers

The system programmer may access control of any of the NSC858 registers summarized in Table I via the CPU. These 8-bit registers are used to control NSC858 operation and to transmit and receive data.

TABLE I. Register Address Designations

Address				Register	Read/ Write
A_3	A_2	A_1	A_0		
0	0	0	0	Rx Holding	R
0	0	0	0	Tx Holding	W
0	0	0	1	Receiver Mode	R/W
0	0	1	0	Transmitter Mode	R/W
0	0	1	1	Global Mode	R/W
0	1	0	0	Command	R/W
0	1	0	1	Baud Rate Generator Divisor Latch (Lower)	R/W
0	1	1	0	Baud Rate Generator Divisor Latch (Upper)	R/W
0	1	1	1	R-T Status Mask	R/W
1	0	0	0	R-T Status	R
1	0	0	1	Modem Status Mask	R/W
1	0	1	0	Modem Status	R
1	0	1	1	Power Down	R/W
1	1	0	0	Master Reset	W

Note: Offset address OD, OE, OF are unused.

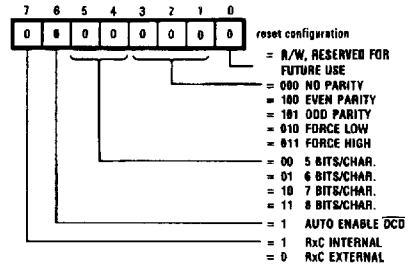
9.1 RECEIVER AND TRANSMITTER HOLDING REGISTER

A read to offset location 00 will access the Receiver holding register; a write will access the Transmitter holding register.

9.2 RECEIVER MODE REGISTER

The system programmer specifies the data format of the receiver (which may differ from the transmitter) by programming the Receiver mode register at offset location "01." This read/write register programs the parity, bits/character, auto enable option, and clock source. When bit 6 of this register is set high the receiver will be enabled any time the $\overline{DCD}$ signal input is low (provided CR0 = 1). When bit 7 is set to a "1" the receiver clock source is the internal baud rate generator and $\overline{RxC}$ is then an output. After reset this register is set to "00."

TABLE II. Receiver Mode Register (Address "01") (Bits RMO-7)



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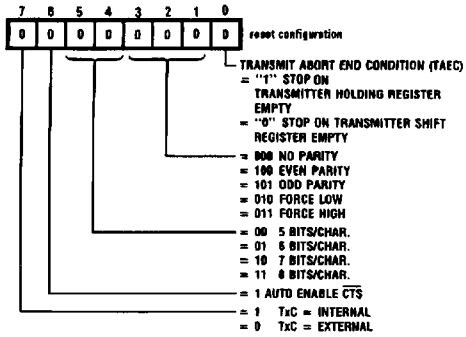
9.0 Registers (Continued)

9.3 TRANSMITTER MODE REGISTER

The system programmer specifies the data format of the transmitter (which may differ from the receiver) by programming the transmitter mode register at offset location "02."

TABLE III. Transmit Mode Register (Address "02") (Bits TM0–7)



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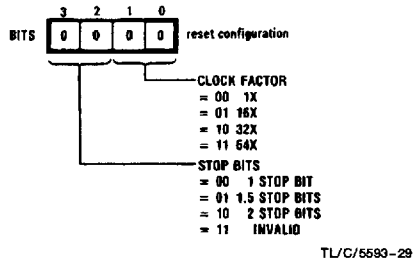
The transmitter mode register is similar in operation to the receiver mode register except for the addition of the Transmit Abort End Condition (TAEC). If this bit is set to a one when a request to disable the transmitter or send a break is pending then the data in the shift register and holding register will be transmitted prior to such action occurring. If TAEC equals 0 then the action will take place after the shift register has been emptied. When bit 6 of this register is set high the transmitter will be enabled any time the $\overline{CTS}$ signal is low (provided CR1 = 1). When bit 7 is set to a "1" the transmitter clock source is the internal baud rate generator, and $\overline{TxC}$ is then an output. After reset this register is set to "00."

9.4 GLOBAL MODE REGISTER

This register is used to program the number of stop bits and the clock factor for both the receiver and transmitter. Only the lower four bits of this register are used, the upper four can be programmed as don't cares and they will be read back as zeros. Programming the number of stop bits is for the transmitter only; the receiver always checks for one stop bit. If a 1X clock factor with 1.5 stop bits is selected for the transmitter the number of stop bits will default to 1. After reset this register is set to "00."

Note: Selecting the 1x clock requires that the clock signal be sent or received along with the data.

TABLE IV. Global Mode Register (Address "03") (Bits GM0–3)



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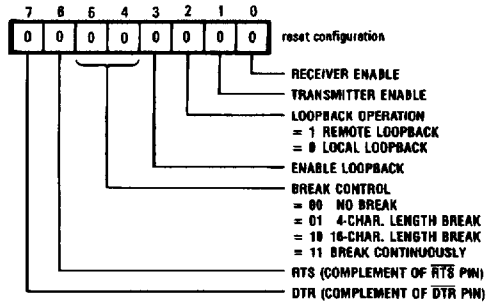
Bits 4–7 are don't care, read as 0s.

9.5 COMMAND REGISTER

The Command register is an eight bit read/write register which is accessed at offset location "04." After reset the command register equals "00."

TABLE V. Command Register (Address "04") (Bits CR0–7)



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Bit 0: Receive Enable, when set to a one the receiver is enabled. If auto enable for the receiver has been programmed then in addition to CR0 = 1, the $\overline{DCD}$ input must be low to enable receiver.

Bit 1: Transmitter Enable, when set to a one the transmitter is enabled. If auto enable for the transmitter is programmed then in addition to CR1 = 1, the $\overline{CTS}$ input must be low to enable transmitter.

Bit 2: A zero selects local loopback and a one selects remote loopback.

Bit 3: A one enables either of the diagnostic modes selected in bit 2 of the command register.

Bits 4 and 5: Bits 4 and 5 of the command register are used to program the length of a transmitted break condition. A continuous break must be terminated by the CPU, but the 4 and 16 character length breaks are self clearing. (At the beginning of the last break character bits 4 and 5 will automatically be reset to 0.) Break commands affect the status of bit 6 (TBK) of the R-T Status register (see R-T Status register). Break control bits are cleared by software or hardware power down.

Bits 6 and 7: These two bits control the status of the output pins $\overline{RTS}$ (pin 24) and $\overline{DTR}$ (pin 25) respectively. They may be used as modem control functions or be used as general purpose outputs. The output pins will always reflect the complement of the register bits.

9.6 R-T STATUS REGISTER

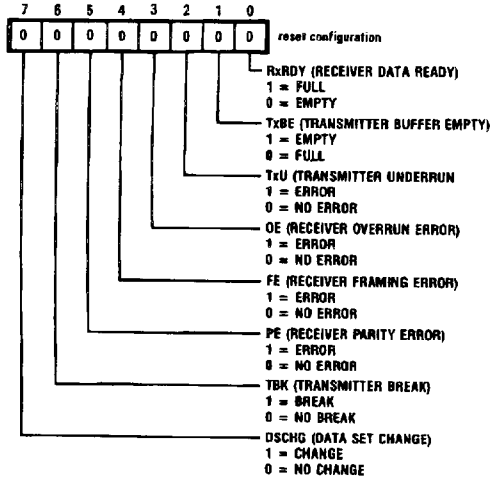
This 8-bit register contains status information of the NSC858 and therefore is a read only register at offset location "08." Each bit in this register can generate an interrupt ($\overline{RTI}$). If any bit goes active high and its associated mask bit is set then the $\overline{RTI}$ will go low. $\overline{RTI}$ will be cleared when all unmasked R-T Status bits are cleared. Bits 0 and 1, receiver ready and transmitter empty are cleared by reading the receiver holding register or writing the transmitter holding register respectively. Bits 2 through 5, transmit underrun, receiver overrun, framing error, parity error are cleared by reading the R-T Status register. Bit two, transmitter underrun will occur when both the transmit holding register and the transmit shift register are empty.

9.0 Registers (Continued)

Bit three, overrun error, will occur when the CPU does not read a character before the next one becomes available. The OE bit informs the programmer or CPU that RXHR data has been overrun or overwritten. The byte in the shift register is always transferred to the holding register, even after an overrun occurs. If an OE occurs, it is standard protocol to request a re-transmission of that block of data. A read of RXHR, when a subsequent read of R-T status shows that no OE is present, indicates current receiver data is available. Bit four, framing error, occurs when a valid stop bit is not detected. Bit 5 is set when a parity error is detected. Bits three, four and five are affected by the receiver only.

Bit 6, Transmit Break (TBK) is set at the beginning of each break character during a break continuously command, or at the beginning of the final break character in a 4 or 16 character programmed break length. It is cleared by reading the R-T Status register. Bit 7, Data Set Change (DSCHG) will be set whenever any of the bits 0–3 of the Modem Status register and their associated mask bit are set. Data Set Change bit is cleared by reading the Modem Status register or is masked off by writing "0" to all modem register bits. After reset the R-T Status register equals '02', i.e. all bits except TxBE are reset to zero.

TABLE VI. R-T Status Register (Address "08") (Bits SR0–7)



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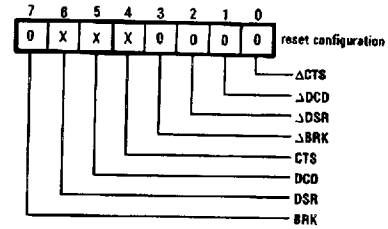
9.7 R-T STATUS MASK REGISTER (SM0–7)

This register is used in conjunction with the R-T Status register to enable or disable conditional interrupts A one in any bit unmasks its associated bit in the R-T Status register, and allows it to generate an interrupt out through $\overline{RTI}$. The mask affects only the interrupt and not the R-T Status bits. This eight bit register is both read and writable at offset location "07." After reset it is set to "0" which disables all interrupts. Each bit in the R-T Status mask register is associated with that bit in the R-T Status register (e.g., SM0 is SR0's mask).

9.8 MODEM STATUS

This eight bit read only register which is addressed at offset location "0A" contains modem or general purpose input and receiver break information.

TABLE VII. Modem Status Register (Address "0A") (Bits MS0–7)



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Each of the four status signals in this register also have an associated delta bit in this register. Each delta bit (bits MS0–3) will be set when its corresponding bit changes states. These four delta bits are cleared when the Modem Status register is read. If any of these four delta bits and associated mask bits are set they will force DSCHG (bit 7) of the R-T Status register high. Bits 4–6, CTS, DCD, DSR can be used as modem signals or general purpose inputs. In either case the value in the register represents the complements of the input pins $\overline{CTS}$ (pin 26), $\overline{DCD}$ (pin 23), and $\overline{DSR}$ (Pin 27). Bit 7 (BRK) when set to a one indicates that the receiver has detected a break condition. It is cleared when break terminates. After reset ΔCTS, ΔDCD, ΔDSR, ΔBRK and BRK are cleared.

9.9 MODEM MASK REGISTER (MM0–3)

This 4-bit read/write register, which is addressed at offset location "09," contains mask bits for the four delta bits of the Modem Status register (MS0–3). A one ("1") in any of three bits and a one in the associated delta bit of the Modem Status register will set the DSCHG bit of the R-T Status register. Modem Mask bit 0 is associated with Modem Status bit 0, etc. The four (4) most significant bits of this register will read as zeros. After reset the register equals '00'.

9.10 POWER DOWN REGISTER (PD0)

This one bit register can both be read and written at offset location "0B." When bit zero is set to a one the NSC858 will be put into software power down. This disables the receiver and transmitter clocks, shuts off the baud rate generator and crystal oscillator, and clears the RxE, TxE, and break control bits in the command register. Registers on chip can still be accessed by the CPU during software power down. Bits 1 through 7 will always read as 0.

9.11 MASTER RESET REGISTER

This write only register is addressed at offset location "0C." When writing to this register the data can be any value (don't cares). Resetting the NSC858 by way of the reset register is functionally identical to resetting it by the MR pin.

9.12 BAUD RATE GENERATOR DIVISOR LATCH

These two 8-bit read/write registers which are accessed at offset locations "05" (lower) and "06" (upper) are used to program the baud rate divisor. These registers are not affected by the reset function and are powered up in a random state.

10.0 Functional Description

10.1 PROGRAMMABLE BAUD GENERATOR

The NSC858 contains a programmable Baud Generator that is capable of taking any clock input (DC to 4.1 MHz) and dividing it by any divisor from 1 to ($2^{16}-1$). The output frequency of the Baud Generator (available at $\overline{TxC}/\overline{BRGOUT}$ or $\overline{RxC}/\overline{BRGOUT}$, if internal $\overline{TxC}$ or $\overline{RxC}$ is selected) is equal to the clock factor (1X, 16X, 32X, 64X) times the baud rate. The divisor number is determined by the following equation:

$$\text{divisor \#} = \frac{\text{Frequency Input } (f_{BRC})}{[\text{Baud Rate} \times \text{Clock Factor } (1, 16, 32, 64)]}$$

Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables VIII and IX illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

TABLE VIII. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used To Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

TABLE IX. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used To Generate 16 x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	0.317
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—

10.2 RECEIVER AND TRANSMITTER OPERATION

The NSC858 transmits and receives data in an asynchronous communications mode. The CPU must set up the appropriate mode of operation, number of bits per character, parity, number of stop bits, etc. Separate mode registers exist for the independent specification of receiver and transmitter operation. These independent specifications include parity, character length, and internal or external clock source. Only the Global Mode Register, which controls the number of stop bits and the clock factor, exercises common control over the receiver and transmitter (receiver looks for only one stop bit).

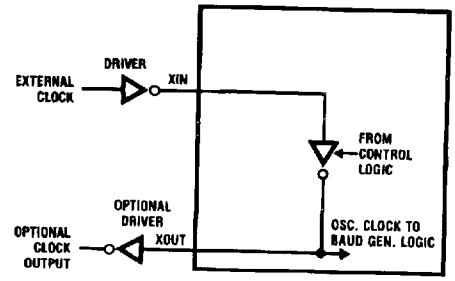
10.3 TRANSMITTER OPERATION

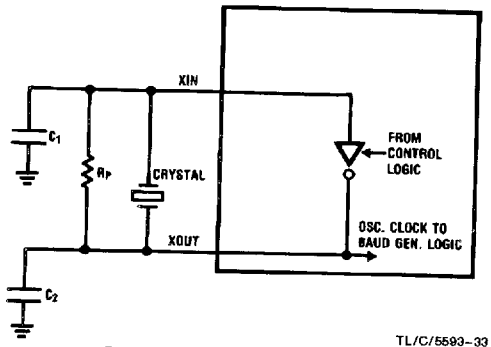
The Transmitter Holding register is loaded by the CPU. To enable the transmitter, TxE must be set in the Command register. $\overline{CTS}$ must be low if the auto enable is set in the Tx Mode register. The Transmitter Holding register is then parallel loaded into the Transmitter Shift register, and the start bit, parity bit and the specified number of stop bits are inserted. This serialized data is available at the TxD output pad, and changes on the rising edge of $\overline{TxC}$, or equivalently the falling edge of $\overline{TxC}$. The TxD output remains in a mark ("1") condition when no data is being transmitted, with the exception of sending a break ("0").

A break condition is initiated by writing either a continuous or specified length break request to the Command Register. A finite break specification of either 4 or 16 character lengths can be extended by re-writing the break command before the specified break length is completed. Each break character is transmitted as a start bit, logical zero data, logical zero parity (if specified) and logical zero stop bit(s). The number of data and stop bits, plus the presence of a parity bit are determined by the Transmitter and Global Mode registers. Thus, the total number of (all zero) bits in a break character is the same as that for data. The break is terminated by writing "00" to the Break Control bits in the Command Register. The Set Break bits in the Command register are always reset to "00" after the termination of the specified break transmission or if the transmitter is disabled during a break transmission. The TxD output will always return to a mark condition for at least one bit time before transmitting a character after a break condition. Data in the Transmitter Holding register, whether loaded before (on TAEC=0) or during the break will be transmitted after the break is terminated.

10.0 Functional Description (Continued)

10.4 TYPICAL CLOCK CIRCUITS





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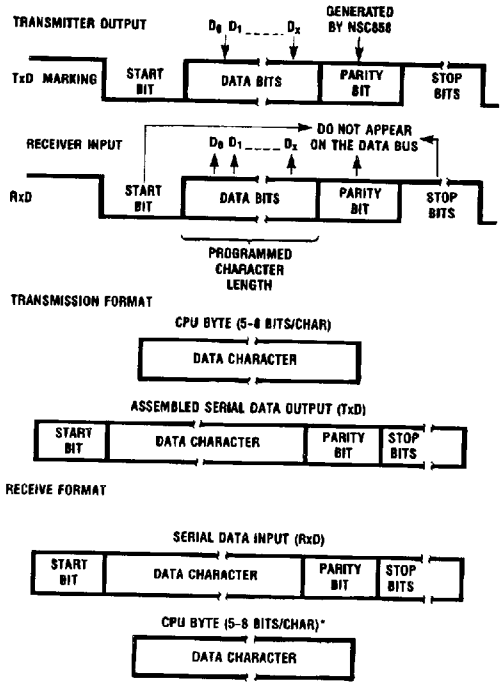
CRYSTAL	R_P	C_1	C_2
3.1 MHz	1 MΩ	10–30 pF	40–60 pF
1.8 MHz	1 MΩ	10–30 pF	40–60 pF

FIGURE 2. Typical Crystal Oscillator Network



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Note: If character length is defined as 5, 6 or 7 bits, the unused bits are set to "0").

FIGURE 3

10.5 RECEIVER OPERATION

The NSC858 receives serial data on the RxD input. To enable the receiver, $\overline{DCD}$ must be low if the $\overline{DCD}$ Auto Enable bit in the Receiver Mode register is set ("1"). RxE must be set in the Command register. RxD is sampled on the falling edge of RxC or equivalently on the rising edge of $\overline{RxC}$. If a high ("1") to low ("0") transition of RxD is detected, RxD is sampled again, for all except the 1X clock factor, at ½ of a bit time later. If RxD is still low, then a valid start bit has been received and character assembly proceeds. If RxD has returned high, then a valid start bit has not been received, and the search for a valid start bit continues. When a character has been assembled in the Receiver Shift Register and transferred to the Receiver Holding Register, the RxRDY bit (and any error bits that may have occurred) in the R-T Status register will be set and $\overline{RTI}$ will go low (if the proper mask bits are set). After the CPU reads the Receiver Holding register, the RxRDY will go low and the $\overline{RTI}$ will go inactive ("1").

The receiver will detect a break condition on RxD if an all zero character with zero parity bit (if parity is specified) and a zero stop bit is received. For the break condition to terminate, RxD must be high for one half a bit time. If a break condition is detected, bits 3 and 7 in the Modem Status register (ΔBRK and BRK respectively) will be set. Bit 3 (ΔBRK) will then cause bit 7 (DSCHG) in the R-T Status register to be set which in turn forces $\overline{RTI}$ to an asserted state ("0"). These interrupts will occur only if the appropriate mask bits are set for the registers in question.

When the 1x clock factor is selected:

The RxC pin on the NSC858 should be connected to the clock signal of the incoming data stream and bit 7 of the receiver mode register should be cleared to A0.

The TxC output of the NSC858 does not have to be sent to the remote receiver unless the receiver is using a 1x clock factor.

10.6 PROGRAMMING THE NSC858

There are two distinct steps in programming the 858. During initialization, the modes, clocks, masks and commands are set up. Then, in operation, Modem I/O takes place, status is monitored, the receiver and transmitter are run as needed.

To initialize the 858, first pulse the MR line or write to the Master Reset register. Then, write to the following registers in any order, except for enabling the Rx and Tx, which must

10.0 Functional Description (Continued)

be at the end of the set up procedure. The Global, Receiver and Transmitter Mode registers determine the modes for the Rx and Tx. These latter two registers often will have the same data byte written to them, but are kept independent for flexibility. If the mode registers indicate that the receiver and/or the transmitter use an internal clock, then data (determined by the crystal frequency and desired bit time and clock factor) should be written to the upper and lower Baud Rate Generator Divisor Latches. The Modem Status Mask register enables Data Set change in R-T Status. If interrupts are required, the R-T Status Mask register allows $\overline{RTI}$ to occur. Write to the Command register to enable the receiver and/or transmitter only when all else is set up.

In operation, the 858 can transmit, receive and handle I/O simultaneously. Modem outputs are written to at the Command register, while the inputs are read at the Modem Status register. Data flow and errors are read at the R-T Status register. When serial data has been shifted in and assembled, the receiver is ready, and the word can be read at the Rx Holding register. When the transmitter buffer is empty, the Tx Holding register can be written to, and the word will be shifted out as serial asynchronous data.

Once the 858 is running, several options may be exercised. Masks can be changed at any time. The Rx and Tx are disabled or enabled, as needed, by writing to the Command register, or toggling the auto enable modem inputs (if used). Both the Rx and Tx should be disabled before either altering any mode or engaging a loopback diagnostic, and they can be re-enabled then or at a later time. Power down is allowed at any time except during loopback, although data may be lost if PD occurs in the middle of a word.

Thus, software for the NSC858 is of two types. The initialization routine is performed once. The operation routines, usually incorporating polling or interrupts, are then run continuously or on demand, depending upon the system or application.

10.7 DIAGNOSTIC CAPABILITIES

The NSC858 offers both remote and local loopback diagnostic capabilities. These features are selected through the Command register.

Local Loopback Mode (see *Figure 4*)

1. The transmitter output is internally connected to the receiver input.
2. $\overline{DTR}$ is internally connected to $\overline{DCD}$, and $\overline{RTS}$ is internally connected to $\overline{CTS}$.
3. $\overline{TxC}$ is internally connected to $\overline{RxC}$.
4. The DSR is internally held low (inactive).
5. The TxD, $\overline{DTR}$ and $\overline{RTS}$ outputs are held high.
6. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and $\overline{RxD}$ inputs are ignored.
7. Except as noted, all other Status, Mode and Command Register bits and interrupts retain their functions and settings.

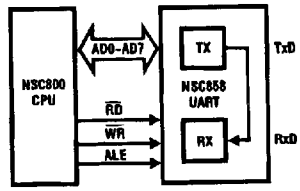

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FIGURE 4. Local Loopback

Remote Loopback Mode (see *Figure 5*)

1. The contents of the Receiver Holding Register, when RxRDY = 1 indicates it is full, are transferred to the Transmitter Holding register, when TxBE = 1 indicates it is empty. After this action, both RxRDY and TxBE are cleared.
2. $\overline{RxC}$ is connected internally to $\overline{TxC}$.
3. Setting the Remote Loopback Mode places all receiver and transmitter flags under control of the remote loopback sequencer. RxRDY and TxBE can be monitored to follow automatic remote loopback data flow, while OE and TxU can indicate system problems.
4. The CPU can read the Receiver Holding register if desired, but this is not necessary. The CPU cannot load the Transmitter Holding Register.
5. Modem Status, all Mode and Command register bits retain their functions and interrupts are generated.

Under certain conditions entering the remote loopback mode causes a character in the receiver or transmitter holding registers to be sent, even though, the transmitter is disabled.

1. If the UART enters the remote loopback mode immediately after receiving a break character in the normal receive mode, it will then automatically transmit that character.
2. If the UART enters the remote loopback mode before the CPU has read the latest character in the receiver holding register, it will then automatically transmit that character.
3. If the UART enters the remote loopback mode before the last character written to the transmitter holding register is transmitted, then it will automatically transmit this character.

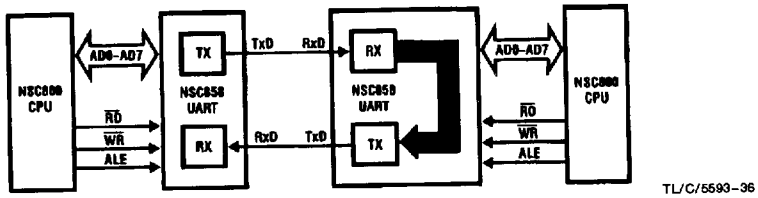

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FIGURE 5. Remote Loopback

11.0 Ordering Information

NSC858XX

- **/A+ = A+ Reliability Screening**
- **D = Ceramic Package**
- **N = Plastic Package**
- **E = Ceramic Leadless Chip Carrier (LCC)**
- **V = Plastic Leaded Chip Carrier (PCC) (Availability to be announced)**

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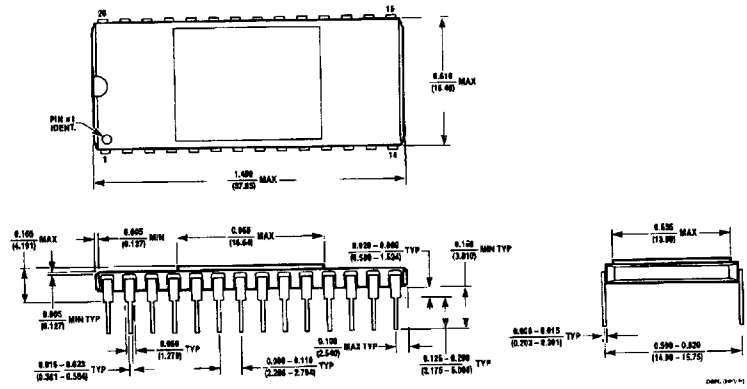
12.0 Reliability Information

Gate Count 4280

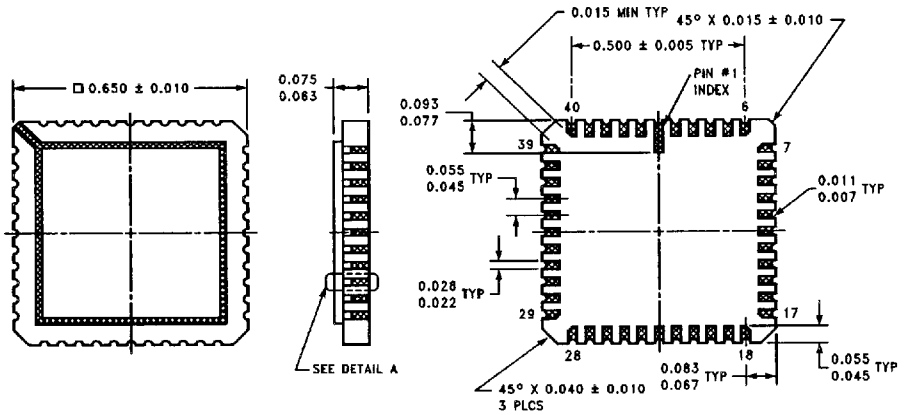
Transistor Count 8450

Physical Dimensions inches (millimeters)

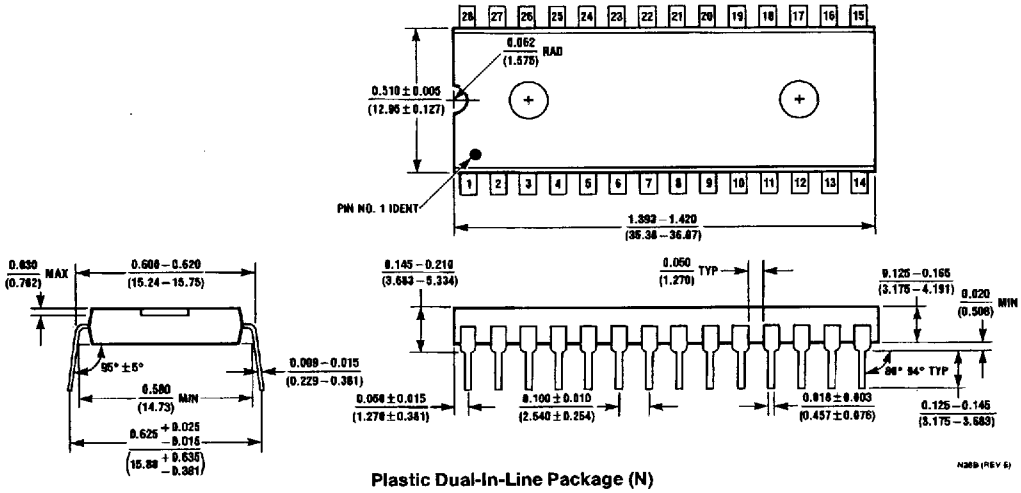


Hermetic Dual-In-Line Package (D)
Order Number NSC858D
NS Package Number D28C

Physical Dimensions inches (millimeters) (Continued)

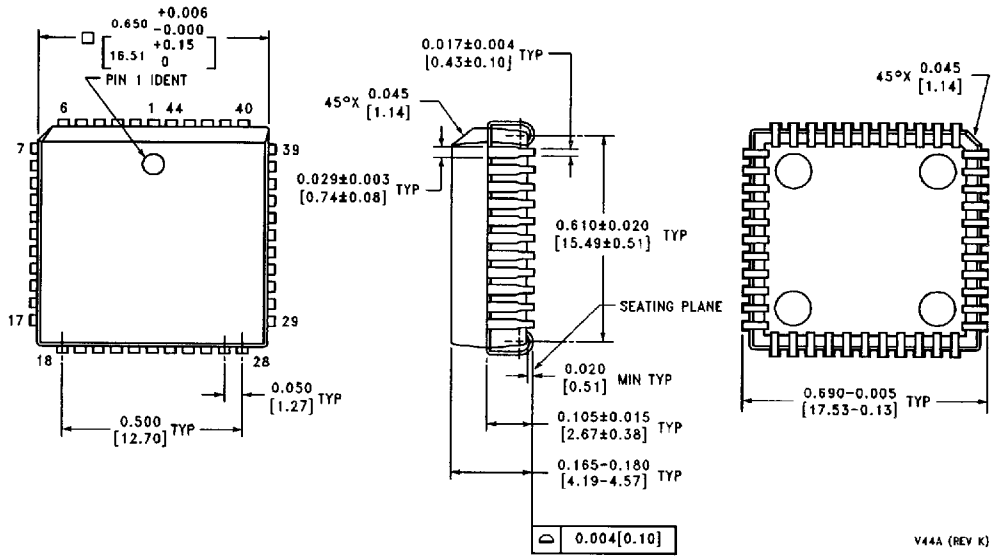


44-Pin Hermetic Leadless Chip Carrier (E)
Order Number NSC858E
NS Package Number E44A



Plastic Dual-In-Line Package (N)
Order Number NSC858N
NS Package Number N28B

Physical Dimensions inches (millimeters) (Continued)



44 Lead Plastic Chip Carrier (V)
Order Number NSC858V
NS Package Number V44A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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