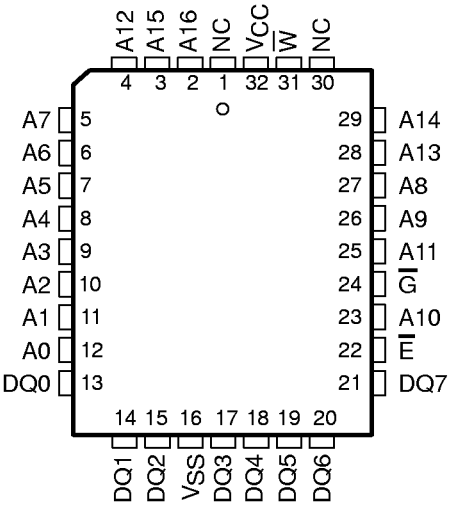
- **Single Power Supply**
  5 V ± 10%
- **Organization . . . 131072 by 8 Bits**
- **Eight Equal Sectors of 16K Bytes**
  - **Any Combination of Sectors Can Be Erased**
  - **Any Combination of Sectors Can Be Marked as Read-Only**
- **Compatible With JEDEC EEPROM Command Set**
- **Fully Automated On-Chip Erase and Byte-Program Operations**
- **100000 Program/Erase Cycles**
- **Compatible With JEDEC Byte-Wide Pinouts**
- **Low-Current Consumption**
  - **Active Read . . . 20 mA Typical**
  - **Active Program/Erase . . . 30 mA Typical**
- **All Inputs/Outputs TTL-Compatible**

FM PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A[0:16]	Address Inputs
DQ[0:7]	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	5-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable
NC	No Connection

description

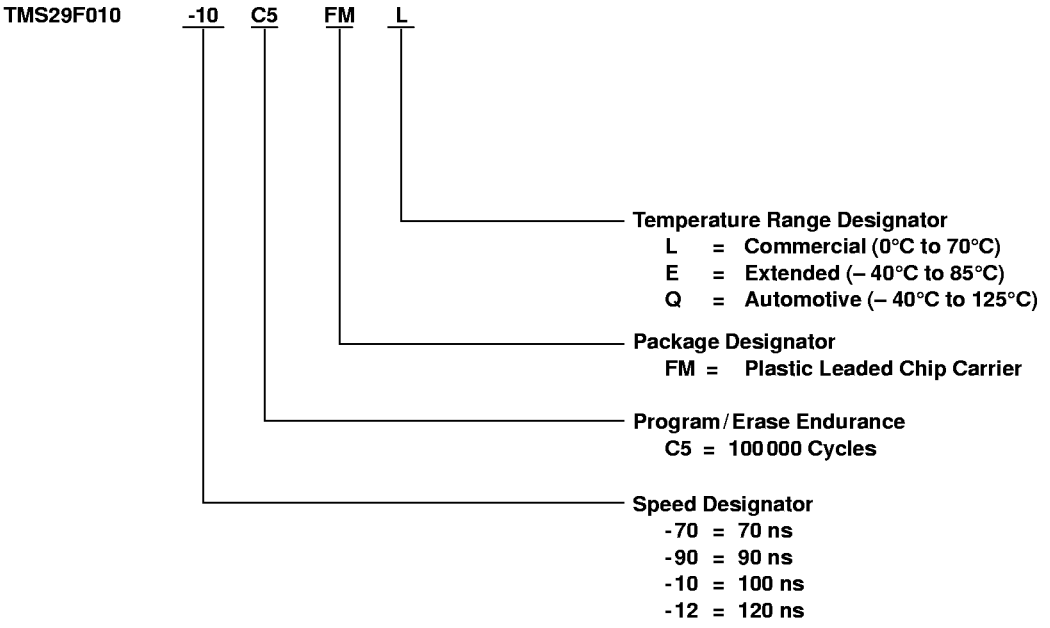
The TMS29F010 is a 131072 by 8-bit (1048576-bit), 5-V single-supply, programmable read-only memory device that can be electrically erased and reprogrammed. This device is organized as eight independent 16K-byte sectors and is offered with access times between 70 ns and 120 ns.

An on-chip state machine controls the program and erase operations. The embedded byte-program and sector/chip-erase functions are fully automatic. The command set is compatible with that of JEDEC 1M-bit EEPROMs. Data-protection of any sector combination is accomplished using a hardware sector-protection feature.

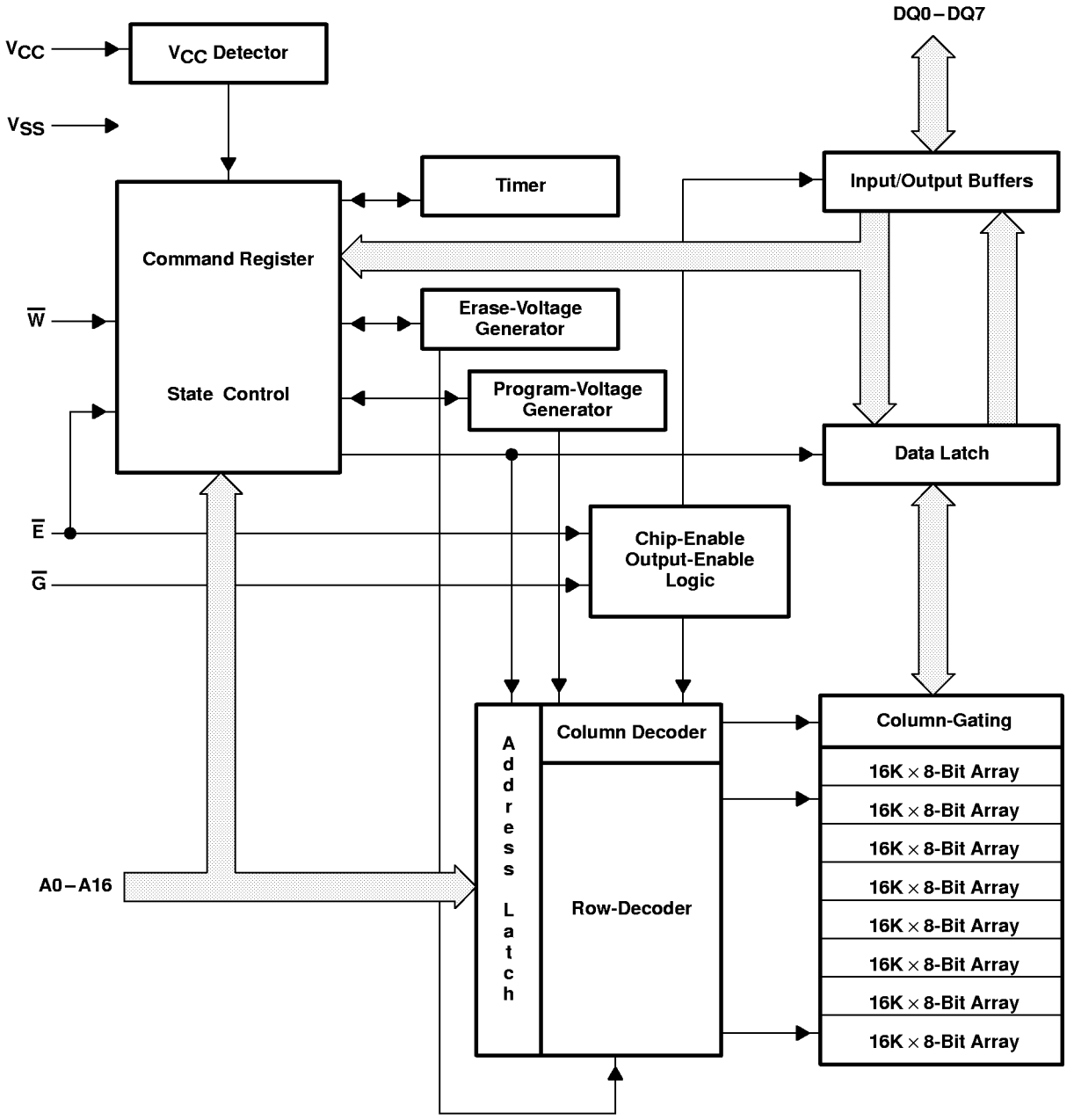
Device operations are selected by writing JEDEC-standard commands into the command register using standard microprocessor write timings. The command register acts as an input to an internal-state machine that interprets the commands, controls the erase and programming operations, outputs the status of the device, outputs data stored in the device, and outputs the device algorithm-selection code. On initial power-up operation, the device defaults to the read mode.

The TMS29F010 is offered in a 32-pin plastic leaded chip carrier (FM suffix) using 1.27-mm (50-mil) lead pitch.

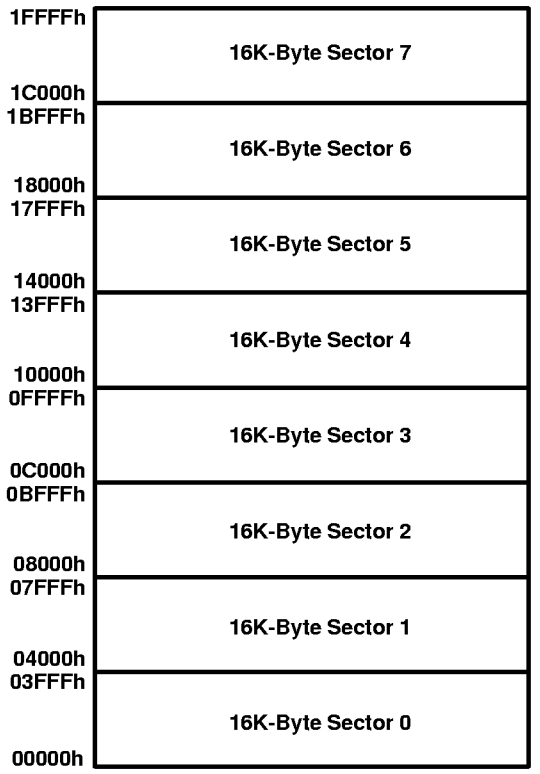
device symbol nomenclature



block diagram



memory sector architecture



	A16	A15	A14	Address Range
Sector 0	0	0	0	00000h – 03FFFh
Sector 1	0	0	1	04000h – 07FFFh
Sector 2	0	1	0	08000h – 0BFFFh
Sector 3	0	1	1	0C000h – 0FFFFh
Sector 4	1	0	0	10000h – 13FFFh
Sector 5	1	0	1	14000h – 17FFFh
Sector 6	1	1	0	18000h – 1BFFFh
Sector 7	1	1	1	1C000h – 1FFFFh

operation

Table 1 summarizes the operation modes.

Table 1. Operation Modes

MODE	FUNCTIONS†							
	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	DQ0–DQ7
Read	V_{IL}	V_{IL}	V_{IH}	A0	A1	A6	A9	Data out
Output disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	Hi-Z
Standby and write inhibit	V_{IH}	X	X	X	X	X	X	Hi-Z
Algorithm-selection mode	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	X	V_{ID}	Manufacturer-equivalent code 01h
				V_{IH}				Device-equivalent code 20h
Write‡	V_{IL}	V_{IH}	V_{IL}	A0	A1	A6	A9	Data in
Sector-protect§	V_{IL}	V_{ID}	V_{IL}	X	X	X	V_{ID}	X
Sector-protect verify§	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{ID}	Data out
Sector-unprotect§ (see Note 1)	V_{ID}	V_{ID}	V_{IL}	X	X	V_{IL}	V_{ID}	X
Sector-unprotect verify§	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{ID}	Data out
Erase operations	V_{IL}	V_{IH}	See Note 2	See Note 2	See Note 2	See Note 2	See Note 2	See Note 2

† X can be V_{IL} or V_{IH}.
‡ See Table 3 for valid address and data during write (byte program).
§ Operation at V_{CC} = 5.0 V and T_A = 25°C.
NOTES: 1. Address pins A7, A12 = V_{IH}.
2. See Figure 6 through Figure 9.

read mode

To read the output of the TMS29F010, a low-level logic signal is applied to the $\overline{E}$ and $\overline{G}$ pins. When two or more TMS29F010 devices are connected in parallel, the output of any one device can be read without interference. The $\overline{E}$ pin is power control and is used for device selection. The $\overline{G}$ pin is output control and is used to gate the data output onto the bus from the selected device.

The address-access time (t_{AVQV}) is the delay from stable address to valid output data. The chip-enable access time (t_{ELQV}) is the delay from $\overline{E} = V_{IL}$ and stable addresses to valid output data. The output-enable access time (t_{GLQV}) is the delay from $\overline{G} = V_{IL}$ to valid output data when $\overline{E} = V_{IL}$ and addresses are stable for at least the duration of $t_{AVQV} - t_{GLQV}$.

standby mode

The I_{CC} supply current is reduced by applying a logic-high level on $\overline{E}$ to enter the standby mode. In the standby mode, the outputs are placed in the high-impedance state. Applying a CMOS logic-high level on $\overline{E}$ reduces the current to 100 μA maximum. Applying a TTL logic-high level on $\overline{E}$ reduces the current to 1 mA maximum.

If the TMS29F010 is deselected during erasure or programming, the device continues to draw active current until the operation is complete.

output disable

When either $\overline{G} = V_{IH}$ or $\overline{E} = V_{IH}$, output from the device is disabled and the output pins (DQ0–DQ7) are placed in the high-impedance state.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code that matches the device with its proper programming- and erase-command operations. This mode is activated when V_{ID} (11.5 V to 12.5 V) is placed on address pin A9. Address pin A1 must be logic-low. Two bytes of code are accessed by toggling address pin A0 from V_{IL} to V_{IH}. All other address pins can be logic-low or logic-high.

The algorithm-selection code can also be read by using the command register. This is useful when V_{ID} is not available to be placed on address pin A9. Table 2 shows the binary algorithm-selection codes for the TMS29F010.

Table 2. Algorithm-Selection Codes†

ALGORITHM SELECTION	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
Byte 0	0	0	0	0	0	0	0	0	1	01h
Byte 1	1	0	0	1	0	0	0	0	0	20h

† A1 = V_{IL}, $\overline{E}$ = $\overline{G}$ = V_{IL}

erasure and programming

Erasure and programming of the TMS29F010 are accomplished by writing a sequence of commands using standard microprocessor-write timings. The commands are written to a command register and input to the command-state machine (CSM). The CSM interprets the command entered and initiates program and erase operations as instructed. The CSM acts as the interface between the write-state machine (WSM) and the external chip operations. The WSM controls all voltage generation, pulse generation, preconditioning, and verification of the memory contents. Program and sector/chip-erase functions are fully automatic. Once the end of a program or erase operation is reached, the device internally resets to the read mode. If V_{CC} drops below the low-voltage-detect level (V_{LKO}), any operation in progress is aborted and the device resets to the read mode. If a byte-program or chip-erase operation is in progress, additional program/erase commands are ignored until the operation ends.

command definitions

Device operating modes are selected by writing specific address and data sequences into the command register. Table 3 defines the valid command sequences. Writing incorrect address and data values or writing them in the incorrect sequence causes the device to reset to the read mode. The command register does not occupy an addressable memory location. The register stores the command sequence, along with the address and data needed by the memory array. Commands are written by setting $\overline{E}$ = V_{IL} and $\overline{G}$ = V_{IH}, and bringing $\overline{W}$ from V_{IH} to V_{IL}. Addresses are latched on the falling edge of $\overline{W}$ and data is latched on the rising edge of $\overline{W}$. Holding $\overline{W}$ = V_{IL} and toggling $\overline{E}$ is an alternative method. See the byte-program and chip/sector-erase sections for a more complete description.

command definitions (continued)

Table 3. Command Definitions†

COMMAND	BUS CYCLES	1ST CYCLE ADDR DATA	2ND CYCLE ADDR DATA	3RD CYCLE ADDR DATA	4TH CYCLE ADDR DATA	5TH CYCLE ADDR DATA	6TH CYCLE ADDR DATA
Read‡	1	RA RD					
Reset/Read§	2	XXXXh F0h	RA RD				
	4	5555h AAh	2AAAh 55h	5555h F0h	RA RD		
Algorithm selection	4	5555h AAh	2AAAh 55h	5555h 90h	RA RD		
Byte program	4	5555h AAh	2AAAh 55h	5555h A0h	PA PD		
Chip erase	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	5555h 10h
Sector erase	6	5555h AAh	2AAAh 55h	5555h 80h	5555h AAh	2AAAh 55h	SA 30h

RA = Address of the location to be read
PA = Address of the location to be programmed
SA = Address of the sector to be erased
Addresses A14, A15, and A16 select one of eight sectors
RD = Data to be read at the selected address location
PD = Data to be programmed at the selected address location

† Address pins A15 and A16 = V_{IL} or V_{IH} for all bus-cycle addresses except for program address (PA), sector address (SA), and read address (RA).

‡ No command cycles are required when the device is in read mode.

§ The reset command is required to return to the read mode when the device is in the algorithm-selection mode or if DQ5 goes high.

reset/read command

The read mode is activated by writing either of the two reset command sequences into the command register. The device remains in this mode until another valid command sequence is input into the command register. Memory data is available in the read mode and can be read with standard microprocessor read-cycle timing.

On power up, the device defaults to the read mode; therefore, a reset command sequence is not required and memory data is available.

algorithm-selection command

The algorithm-selection command allows access to a binary code that matches the device with the proper programming- and erase-command operations. After writing the three-bus-cycle command sequence, the first byte of the algorithm-selection code (01h) can be read from address XX00h. The second byte of the code (20h) can be read from address XX01h (see Table 2). This mode remains in effect until another valid command sequence is written to the device.

Sector protection can be determined by using the algorithm-selection command. After issuing the three bus-cycle command sequence, the sector-protection status can be read on DQ0. Set address pins A0 = V_{IL} and A1 = V_{IH}, and then the sector address pins A14, A15, and A16 select the sector to be checked. The remaining address pins can be V_{IL} or V_{IH}. If the sector that is selected is protected, DQ0 outputs a 1 state, and, if the sector selected is not protected, DQ0 outputs a 0 state. This mode remains in effect until another valid command sequence is written to the device.

byte-program command

Byte programming is a four-bus-cycle command sequence. The first three bus cycles put the device into the program-setup state, and the fourth bus cycle loads the address location and the data to be programmed into the device. The addresses are latched on the falling edge of $\overline{W}$ and the data is latched on the rising edge of $\overline{W}$ in the fourth bus cycle. The rising edge of $\overline{W}$ starts the byte-program operation. The embedded byte-programming function automatically provides needed voltage and timing to program and to verify the cell margin. Any further commands written to the device during the program operation are ignored.

byte-program command (continued)

Programming can be performed at any address location in any order, resulting in logic 0s being programmed into the device. Attempting to program a logic 1 into a bit that has been previously programmed to a logic 0 causes the internal pulse counter to exceed the pulse-count limit. This sets the exceed-timing-limit indicator (DQ5) to a logic-high state. Only an erase operation can change bits from logic 0s to logic 1s. When erased, all bits become logic 1. Figure 3 shows a flow chart of the typical byte-programming operation.

The status of the device during the automatic programming operation can be monitored for completion using the data-polling feature or the toggle-bit feature. See the operation-status section for a full description.

chip-erase command

Chip erase is a six-bus-cycle command sequence. The first three bus cycles put the device into the erase-setup state, and the next two bus cycles unlock the erase mode. The sixth bus cycle loads the chip-erase command. This command sequence is required to ensure that the memory contents are not erased accidentally. The rising edge of $\overline{W}$ starts the chip-erase operation. Any further commands written to the device during the chip-erase operation are ignored.

The embedded chip-erase function automatically provides voltage and timing needed to program and verify all the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. The user is not required to program the memory cells prior to erase. The status of the device during the automatic chip-erase operation can be monitored for completion using the data-polling feature or the toggle-bit feature. See the operation status section for a full description. Figure 6 shows a flow chart for the typical chip-erase operation.

sector-erase command

Sector erase is a six-bus-cycle command sequence. The first three bus cycles cause the device to go into the erase-setup state, and the next two bus cycles unlock the erase mode. The sixth bus cycle loads the sector-erase command and the sector-address location to be erased. Any address location within the desired sector can be used. The addresses are latched on the falling edge of $\overline{W}$ and the sector-erase command (30h) is latched on the rising edge of $\overline{W}$ in the sixth bus cycle. After a delay of 80 μs from the rising edge of $\overline{W}$, the sector-erase operation begins on the selected sector(s).

Additional sectors can be selected to be erased concurrently during the sector-erase command sequence. For each additional sector selected for erase, another bus cycle is issued. The bus cycle loads the next sector-address location and the sector-erase command. The time between the end of the previous bus cycle and the start of the next bus cycle must be less than 80 μs—otherwise, the new sector location is not loaded. A time delay of 80 μs from the rising edge of the last $\overline{W}$ cycle starts the sector-erase operation. If there is a falling edge of $\overline{W}$ within the 80-μs time delay, the timer is reset.

One to eight sector-address locations can be loaded in any order. The state of the delay timer can be monitored using the sector-erase-delay indicator (DQ3). If DQ3 is logic low, the time delay has not expired. See the operation-status section for a full description.

Any command other than sector-erase (30h) written to the device during the sector-erase operation causes the device to exit the sector-erase mode; meanwhile, the contents of the sector(s) selected for erase are no longer valid. To complete the sector-erase operation, the sector-erase command sequence must be repeated.

The embedded sector-erase function automatically provides needed voltage and timing to program and to verify all of the memory cells prior to electrical erase and then erases and verifies the cell margin automatically. Programming the memory cells prior to erase is not required. The status of the device during the automatic sector-erase operation can be monitored for completion by using the data-polling feature or the toggle-bit feature. See the operation-status section for a full description. Figure 8 shows a flow chart of the typical sector-erase operation.

operation status

status bit definitions

During operation of the embedded program and erase functions, the status of the device can be determined by reading the data state of designated outputs. The data-polling bit (DQ7) and toggle-bit (DQ6) require multiple successive reads to observe a change in the state of the designated output. Table 4 defines the values of the status flags.

Table 4. Operation Status Flags†

Device Operation‡	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Byte-programming in progress	$\overline{DQ7}$	T	0	X	0	X	X	X
Byte-programming exceed time limit	$\overline{DQ7}$	T	1	X	0	X	X	X
Byte-programming complete	D	D	D	D	D	D	D	D
Sector/chip-erase in progress	0	T	0	X	1	X	X	X
Sector/chip-erase exceed time limit	0	T	1	X	1	X	X	X
Sector/chip-erase complete	1	1	1	1	1	1	1	1

† T= toggle, D = data, X = data undefined, $\overline{DQ7}$ = complement of data written to DQ7
‡ DQ4, DQ2, DQ1, DQ0 are reserved for future use.

data-polling (DQ7)

The data-polling status function outputs the complement of the data latched into the DQ7 data register while the write-state machine (WSM) is engaged in a program or erase operation. Data bit DQ7 changes from complement to true to indicate the end of an operation. Data polling is available only during the byte-programming, chip-erase, sector-erase, and sector-erase timing delay. Data polling is valid after the rising edge of $\overline{W}$ in the last bus cycle of the command sequence loaded into the command register. Figure 10 shows a flow chart of the data-polling operation.

During a byte-program operation, reading DQ7 outputs the complement of the DQ7 data to be programmed at the selected address location. Upon completion, reading DQ7 outputs the true DQ7 data loaded into the program data register. During erase operations, reading DQ7 outputs a logic 0, and upon completion, reading DQ7 outputs a logic 1. Also, data polling must be performed at a sector address that is within a sector being erased; otherwise, the status is not valid. When using data polling, the address must remain stable throughout the operation.

During a data-polling read, while $\overline{G}$ is low, DQ7 can change asynchronously with the other DQs. Depending on the read timing, the system can read valid data on DQ7, while other DQ pins are still invalid. The data on DQ0–DQ7 is valid with a subsequent read of the device. See Figure 11 for the data-polling timing diagram.

toggle-bit (DQ6)

The toggle-bit status function outputs data on DQ6 that toggles between logic 1 and logic 0 while the WSM is engaged in a program or erase operation. When toggle-bit DQ6 stops toggling after two consecutive reads to the same address, the operation is complete. The toggle bit is available only during the byte-programming, chip-erase, sector-erase, and sector-erase timing delay. Toggle bit data is valid after the rising edge of $\overline{W}$ in the last bus cycle of the command sequence loaded into the command register. Figure 12 shows a flow chart for the toggle-bit status-read algorithm. Depending on the read timing, DQ6 can stop toggling while other DQ pins are still invalid. The data on DQ0–DQ7 is valid with a subsequent read of the device. Figure 13 shows the toggle-bit timing diagram.

exceed-time-limit (DQ5)

The program and erase operations use an internal pulse counter to limit the number of pulses applied. If the pulse count limit is exceeded, DQ5 is set to a logic 1, indicating that the program or erase operation has failed. DQ7 will not change from complemented data to true data and DQ6 will not stop toggling when read. To continue operation, the device must be reset.

The exceed-time-limit condition occurs when attempting to program a logic 1 into a bit that has been programmed previously to a logic 0. Only an erase operation can change bits from logic 0 to logic 1. After reset, the device is functional and can be erased and reprogrammed.

sector-load-timer (DQ3)

The sector-load-timer status bit, DQ3, is used to determine if the time to load additional sector addresses has expired. After completion of a sector-erase command sequence, DQ3 remains at a logic 0 for 80 μs. This indicates that another sector-erase command sequence can be issued. DQ3 set at a logic 1 indicates that the delay has expired and attempts to issue additional sector-erase commands are ignored. See the sector-erase command section for a description.

The data-polling bit and toggle bit are valid during the 80-μs time delay and can be used to determine if a valid sector-erase command has been issued. To ensure additional sector-erase commands have been accepted, the status of DQ3 should be read before and after each additional sector-erase command. If DQ3 is at a logic low on both reads, then the additional sector-erase command was accepted.

data protection

hardware-sector protect feature

This feature disables both programming and erase operations on any combination of one to eight sectors. Commands to program or erase a protected sector do not change the data contained in the sector. The data-polling and toggle bits operate for 2 μs to 100 μs and then return to valid data. This feature is enabled using high-voltage V_{ID} (11.5 V to 12.5 V) on address pin A9 and control pin $\overline{G}$, and V_{IL} on control pin $\overline{E}$. Figure 14 shows a flow chart of the sector-protect operation.

The device is delivered with all sectors unprotected; however, sector-unprotect mode is available to unprotect protected sectors. Figure 16 is a flow chart of the sector-unprotect operation.

sector-protect operation

The sector-protect mode is activated when V_{CC} = 5.0 V (and operation at T_A = 25°C), $\overline{W} = V_{IH}$, $\overline{E} = V_{IL}$, and address pin A9 and control pin $\overline{G}$ are forced to V_{ID}. The sector-select address pins A14, A15, and A16 are used to select the sector to be protected. Address pins A0–A8, A10–A13, and I/O pins DQ0–DQ7 must be stable and can be V_{IL} or V_{IH}. Once the addresses are stable, $\overline{W}$ is pulsed low for 100 μs. The operation begins on the falling edge of $\overline{W}$ and terminates on the rising edge of $\overline{W}$. Figure 15 shows a timing diagram of the sector-protect operation.

sector-protect verify

Verification of sector protection is activated when V_{CC} = 5.0 V (and operation at T_A = 25°C), $\overline{W} = V_{IH}$, $\overline{G} = V_{IL}$, $\overline{E} = V_{IL}$, and address pin A9 = V_{ID}. Address pins A0 and A6 are set to V_{IL}, and A1 is set to V_{IH}. The sector-address pins A14, A15, and A16 select the sector to be verified. The other address pins can be V_{IL} or V_{IH}. If the sector selected is protected, the DQs output 01h, and if the sector selected is not protected, the DQs output 00h.

sector unprotect operation

Prior to the sector-unprotect operation, all sectors should be protected using the sector-protect mode. Sector unprotect is activated when V_{CC} = 5.0 V (and operation at T_A = 25°C), $\overline{W}$ = V_{IH}, and address pin A9 and control pins $\overline{G}$ and $\overline{E}$ are forced to V_{ID}. Address pin A6 = V_{IL}, and pins A7 and A12 are set to V_{IH}. The sector-select address pins A14, A15, and A16 can be V_{IL} or V_{IH}. All eight sectors are unprotected in parallel, and once the inputs are stable, $\overline{W}$ is pulsed low for 10 ms. The unprotect operation begins on the falling edge of $\overline{W}$ and terminates on the rising edge of $\overline{W}$. Figure 17 shows a timing diagram of the sector-unprotect operation.

sector-unprotect verify

Verification of sector-unprotect is accomplished when V_{CC} = 5.0 V (and operation at T_A = 25°C), $\overline{W}$ = V_{IH}, $\overline{G}$ = V_{IL}, $\overline{E}$ = V_{IL}, and address pin A9 = V_{ID}, and then select the sector to be verified. Address pins A1 and A6 are set to V_{IH} while pin A0 is set to V_{IL}. The other address pins can be V_{IH} or V_{IL}. If the sector that is selected is protected, the DQs output 01h and if the sector is not protected, the DQs output 00h.

low V_{CC} write lockout

During power up and power down, write operations are locked out for V_{CC} less than V_{LKO}. If $V_{CC} < V_{LKO}$, the command input is disabled and the device is reset to the read mode. On power up, if $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL}, and $\overline{G}$ = V_{IH}, the device does not accept commands on the rising edge of $\overline{W}$. The device automatically powers up in the read mode.

glitching

Pulses of less than 5 ns (typical) on $\overline{G}$, $\overline{W}$, or $\overline{E}$ do not issue a write cycle.

power supply considerations

Each device should have a 0.1-µF ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Printed circuit traces to V_{CC} should be appropriate to handle the current demand and minimize inductance.

absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Voltage range with respect to ground:
- Supply voltage range, V_{CC} (see Note 3) . . . . . –2.0 V to + 7.0 V
- All pins except A9, $\overline{E}$, $\overline{G}$ (see Note 3) . . . . . –2.0 V to + 7.0 V
- A9, $\overline{E}$, $\overline{G}$ (see Note 4) . . . . . –2.0 V to + 14.0 V

Ambient temperature range during read/erase/program, T_A
- Commercial (L) . . . . . 0°C to 70°C
- Extended (E) . . . . . –40°C to 85°C
- Automotive (Q) . . . . . –40°C to 125°C

Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 3. Minimum dc voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum dc voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.

4. Minimum dc input voltage on A9, $\overline{E}$, and $\overline{G}$ pins is –0.5 V. During voltage transitions, A9, $\overline{E}$, and $\overline{G}$ may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum dc input voltage on A9, $\overline{E}$, and $\overline{G}$ pins is +12.5 V, which may overshoot to +14.0 V for periods up to 20 ns.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Ambient temperature during read/erase/program	Commercial (L)	0		70	°C
		Extended (E)	–40		85	
		Automotive (Q)	–40		125	

electrical dc characteristics over recommended ranges of supply voltage and ambient temperature

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{IH}	High-level dc input voltage	TTL			2	V_{CC}+0.5	V
		CMOS			0.7*V_{CC}	V_{CC}+0.5	
V_{IL}	Low-level dc input voltage	TTL			–0.5	0.8	V
		CMOS			–0.5	0.8	
V_{ID}	Algorithm-selection and sector-protect/unprotect input voltage		V_{CC} = 5.0 V		11.5	12.5	V
V_{LKO}	Low V_{CC} lock-out voltage (see Note 5)				3.2		V
V_{OH}	High-level dc output voltage	TTL	V_{CC}=V_{CC} MIN†	I_{OH} = – 2.5 mA	2.4		V
		CMOS	V_{CC}=V_{CC} MIN	I_{OH} = – 100 µA	V_{CC} – 0.4		
		CMOS	V_{CC}=V_{CC} MIN	I_{OH} = – 2.5 mA	0.85*V_{CC}		
V_{OL}	Low-level dc output voltage (see Note 6)	TTL	V_{CC}=V_{CC} MIN	I_{OL} = 5.8 mA		0.45	V
		CMOS	V_{CC}=V_{CC} MIN	I_{OL} = 5.8 mA		0.45	
I_I	Input current (leakage)		V_{CC}=V_{CC} MAX	V_I =V_{SS} to V_{CC}		±1	µA
I_O	Output current (leakage)		V_{CC} = V_{CC} MAX	V_O = V_{SS} to V_{CC}		±1	µA
I_{ID}	High-voltage load current		V_{CC} = V_{CC} MAX	A9 = 12.5 V		50	µA
I_{CC1}	V_{CC} active current (see Note 7)		$\overline{E}$ = V_{IL},	$\overline{G}$ = V_{IH}		30	mA
I_{CC2}	V_{CC} active current (see Note 8)		$\overline{E}$ = V_{IL},	$\overline{G}$ = V_{IH}		50	mA
I_{CC3}	V_{CC} supply current (standby)	TTL-input level	V_{CC} = V_{CC} MAX	$\overline{E}$ = V_{IH}		1	mA
		CMOS input level	V_{CC} = V_{CC} MAX	$\overline{E}$ = V_{CC} ± 0.5 V		100	µA

† See the recommended operating conditions table

NOTES: 5. Typical value at nominal condition (T_A = 25°C)
6. 12-mA I_{OL} also available
7. I_{CC} current in the read mode, switching at 6 MHz, I_{OUT} = 0 mA
8. I_{CC} current while erase or program operation is in progress

capacitance over recommended ranges of supply voltage and ambient temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C_{i1}	Input capacitance (All inputs except A9, $\overline{E}$, $\overline{G}$)	V_I = 0 V, f = 1 MHz		7.5	pF
C_{i2}	Input capacitance (A9, $\overline{E}$, $\overline{G}$)	V_I = 0 V, f = 1 MHz		9	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz		12	pF

switching characteristics over recommended ranges of supply voltage and ambient temperature, read-only operation† (see Figure 2, Figure 11, Figure 13, Figure 15, and Figure 17)

PARAMETER		ALTERNATE SYMBOL	'29F010-70		'29F010-90		'29F010-10		'29F010-12		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AVQV}	Access time, address	$t_{a(A)}$		70		90		100		120	ns
t_{ELQV}	Access time, $\overline{E}$	$t_{a(E)}$		70		90		100		120	ns
t_{GLQV}	Access time, $\overline{G}$	$t_{a(G)}$		30		35		45		50	ns
t_{AVAV}	Cycle time, read	$t_{c(R)}$	70		90		100		120		ns
t_{EHQZ}	Disable time, $\overline{E}$ to high impedance	$t_{dis(E)}$		20		20		20		30	ns
t_{GHQZ}	Disable time, $\overline{G}$ to high impedance	$t_{dis(G)}$		20		20		20		30	ns
t_{AXQX}	Hold time, output from address, $\overline{E}$ or $\overline{G}$ change	$t_{h(D)}$	0		0		0		0		ns
t_{WHGL1}	Hold time, $\overline{G}$ read		0		0		0		0		ns
t_{WHGL2}	Hold time, $\overline{G}$ toggle and data polling		10		10		10		10		ns

† See Figure 1 for AC test output load circuit and voltage waveforms.

timing requirements controlled by $\overline{W}$ (see Figure 4, Figure 7, Figure 9, Figure 11, Figure 13, Figure 15, and Figure 17)

		ALTERNATE SYMBOL	'29F010-70			'29F010-90			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AVAV}	Cycle time, write	$t_{c(W)}$	70			90			ns
t_{WHWH1}	Cycle time, programming operation	$t_{c(W)PR}$		18			18		µs
t_{WHWH2}	Cycle time, sector-erase operation			1	15		1	15	s
t_{WHWH3}	Cycle time, chip-erase operation			2	60		2	60	s
t_{WLAX}	Hold time, address	$t_{h(A)}$	45			45			ns
t_{WHDX}	Hold time, data valid after $\overline{W}$ high	$t_{h(D)}$	0			0			ns
t_{WHEH}	Hold time, $\overline{E}$	$t_{h(E)}$	0			0			ns
t_{WHWL}	Pulse duration, $\overline{W}$ high	$t_{w(WH)}$	20			20			ns
t_{WLWH1}	Pulse duration, $\overline{W}$ low	$t_{w(WL)}$	35			45			ns
t_{WLWH2}	Pulse duration, $\overline{W}$ low (see Note 9)		100			100			µs
t_{WLWH3}	Pulse duration, $\overline{W}$ low (see Note 10)		10			10			ms
t_{GHWL}	Recovery time, read-before-write	$t_{rec(R)}$	0			0			ns
t_{AVWL}	Setup time, address	$t_{su(A)}$	0			0			ns
t_{DVWH}	Setup time, data	$t_{su(D)}$	30			45			ns
t_{AVGH}	Setup time, A0 and A6 low and A1 high to $\overline{G}$ high (see Note 9)		0			0			ns
t_{AVGEH}	Setup time, A0 low and A1 and A6 high to $\overline{G}$ and $\overline{E}$ high (see Note 10)		0			0			ns
t_{ELWL}	Setup time, $\overline{E}$	$t_{su(E)}$	0			0			ns
t_{GHWH}	Setup time, $\overline{G}$		0			0			ns
t_{VCEL}	Setup time, V_{CC}		50			50			µs
t_{EHVWL}	Setup time, $\overline{E}$ V_{ID} to $\overline{W}$ (see Note 10)		4			4			µs
t_{GHVWL}	Setup time, $\overline{G}$ V_{ID} to $\overline{W}$ (see Notes 9 and 10)		4			4			µs
t_{WHAH}	Setup time, $\overline{W}$ high to A6 going high (see Note 10)		0			0			ns
t_{HVT}	Transition time, V_{ID} (see Notes 9 and 10)		4			4			µs

NOTES: 9. Sector-protect timing (see Figure 15)
10. Sector-unprotect timing (see Figure 17)

timing requirements controlled by $\overline{W}$ (see Figure 4, Figure 7, Figure 9, Figure 11, Figure 13, Figure 15, and Figure 17) (continued)

		ALTERNATE SYMBOL	'29F010-10			'29F010-12			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AVAV}	Cycle time, write	$t_{c(W)}$	100			120			ns
t_{WHWH1}	Cycle time, programming operation	$t_{c(W)PR}$		18			18		µs
t_{WHWH2}	Cycle time, sector-erase operation			1	15		1	15	s
t_{WHWH3}	Cycle time, chip-erase operation			2	60		2	60	s
t_{WLAX}	Hold time, address	$t_{h(A)}$	45			50			ns
t_{WHDX}	Hold time, data valid after $\overline{W}$ high	$t_{h(D)}$	0			0			ns
t_{WHEH}	Hold time, $\overline{E}$	$t_{h(E)}$	0			0			ns
t_{WHWL}	Pulse duration, $\overline{W}$ high	$t_{w(WH)}$	20			20			ns
t_{WLWH1}	Pulse duration, $\overline{W}$ low	$t_{w(WL)}$	45			50			ns
t_{WLWH2}	Pulse duration, $\overline{W}$ low (see Note 9)		100			100			µs
t_{WLWH3}	Pulse duration, $\overline{W}$ low (see Note 10)		10			10			ms
t_{GHWL}	Recovery time, read-before-write	$t_{rec(R)}$	0			0			ns
t_{AVWL}	Setup time, address	$t_{su(A)}$	0			0			ns
t_{DVWH}	Setup time, data	$t_{su(D)}$	45			50			ns
t_{AVGH}	Setup time, A0 and A6 low and A1 high to $\overline{G}$ high (see Note 9)		0			0			ns
t_{AVGEH}	Setup time, A0 low and A1 and A6 high to $\overline{G}$ and $\overline{E}$ high (see Note 10)		0			0			ns
t_{ELWL}	Setup time, $\overline{E}$	$t_{su(E)}$	0			0			ns
t_{GHWH}	Setup time, $\overline{G}$		0			0			ns
t_{VCEL}	Setup time, V_{CC}		50			50			µs
t_{EHVWL}	Setup time, $\overline{E}$ V_{ID} to $\overline{W}$ (see Note 10)		4			4			µs
t_{GHVWL}	Setup time, $\overline{G}$ V_{ID} to $\overline{W}$ (see Notes 9 and 10)		4			4			µs
t_{WHAH}	Setup time, $\overline{W}$ high to A6 going high (see Note 10)		0			0			ns
t_{HVT}	Transition time, V_{ID} (see Notes 9 and 10)		4			4			µs

NOTES: 9. Sector-protect timing (see Figure 15)
10. Sector-unprotect timing (see Figure 17)

timing requirements controlled by $\overline{E}$ (see Figure 5)

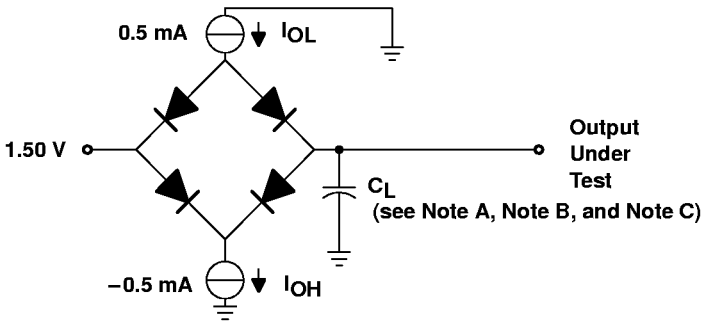
		ALTERNATE SYMBOL	'29F010-70			'29F010-90			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AVAV}	Cycle time, write	$t_{c(W)}$	70			90			ns
t_{EHEH1}	Cycle time, programming operation			18			18		µs
t_{EHEH2}	Cycle time, sector-erase operation (see Note 11)			1	15		1	15	s
t_{EHEH3}	Cycle time, chip-erase operation (see Note 12)			2	60		2	60	s
t_{ELAX}	Hold time, address	$t_{h(A)}$	45			45			ns
t_{EHDX}	Hold time, data	$t_{h(D)}$	0			0			ns
t_{EHWH}	Hold time, $\overline{W}$	$t_{h(W)}$	0			0			ns
t_{ELEH}	Pulse duration, $\overline{E}$ low	$t_{w(EL)}$	35			45			ns
t_{EHEL}	Pulse duration, $\overline{E}$ high	$t_{w(EH)}$	20			20			ns
t_{GHEL}	Recovery time, read-before-write	$t_{rec(R)}$	0			0			ns
t_{AVEL}	Setup time, address	$t_{su(A)}$	0			0			ns
t_{DVEH}	Setup time, data	$t_{su(D)}$	30			45			ns
t_{WLEL}	Setup time, $\overline{W}$	$t_{su(W)}$	0			0			ns

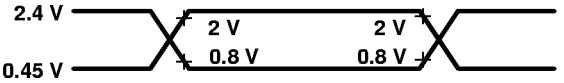
NOTES: 11. Timing diagram of $\overline{E}$-controlled sector-erase operation not enclosed.
12. Timing diagram of $\overline{E}$-controlled chip-erase operation not enclosed.

		ALTERNATE SYMBOL	'29F010-10			'29F010-12			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AVAV}	Cycle time, write	$t_{c(W)}$	100			120			ns
t_{EHEH1}	Cycle time, programming operation			18			18		µs
t_{EHEH2}	Cycle time, sector-erase operation (see Note 11)			1	15		1	15	s
t_{EHEH3}	Cycle time, chip-erase operation (see Note 12)			2	60		2	60	s
t_{ELAX}	Hold time, address	$t_{h(A)}$	45			50			ns
t_{EHDX}	Hold time, data	$t_{h(D)}$	0			0			ns
t_{EHWH}	Hold time, $\overline{W}$	$t_{h(W)}$	0			0			ns
t_{ELEH}	Pulse duration, $\overline{E}$ low	$t_{w(EL)}$	45			50			ns
t_{EHEL}	Pulse duration, $\overline{E}$ high	$t_{w(EH)}$	20			20			ns
t_{GHEL}	Recovery time, read-before-write	$t_{rec(R)}$	0			0			ns
t_{AVEL}	Setup time, address	$t_{su(A)}$	0			0			ns
t_{DVEH}	Setup time, data	$t_{su(D)}$	45			50			ns
t_{WLEL}	Setup time, $\overline{W}$	$t_{su(W)}$	0			0			ns

NOTES: 11. Timing diagram of $\overline{E}$-controlled sector-erase operation not enclosed.
12. Timing diagram of $\overline{E}$-controlled chip-erase operation not enclosed.

PARAMETER MEASUREMENT INFORMATION



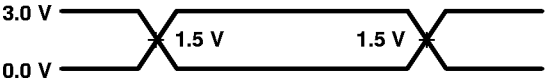


VOLTAGE WAVEFORMS FOR -90, -10, -12

Conditions: V_{IH} = 2.4 V
V_{IL} = 0.45 V
C_L = 100 pF

Measurements taken at: 2.0 V for logic high
0.8 V for logic low

Input rise and fall = <20 ns



VOLTAGE WAVEFORMS FOR -70

Conditions: V_{IH} = 3.0 V
V_{IL} = 0.0 V
C_L = 30 pF

Measurements taken at: 1.5 V for logic high
1.5 V for logic low

Input rise and fall = <5 ns

NOTES: A. C_L includes probe and fixture capacitance.
B. The ac testing inputs for -70 voltage waveforms are driven at 3 V for logic high and 0 V for logic low. Timing measurements for -70 voltage waveforms are made at 1.5 V for logic high and 1.5 V for logic low on both inputs and outputs. The ac testing inputs for -90, -10, and -12 voltage waveforms are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements for -90, -10, and -12 voltage waveforms are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs.
C. Each device should have a 0.1-μF ceramic capacitor connected between V_{CC} and V_{SS}, as closely as possible to the device pins.

Figure 1. AC Test Output Load Circuit and Voltage Waveforms

read operation

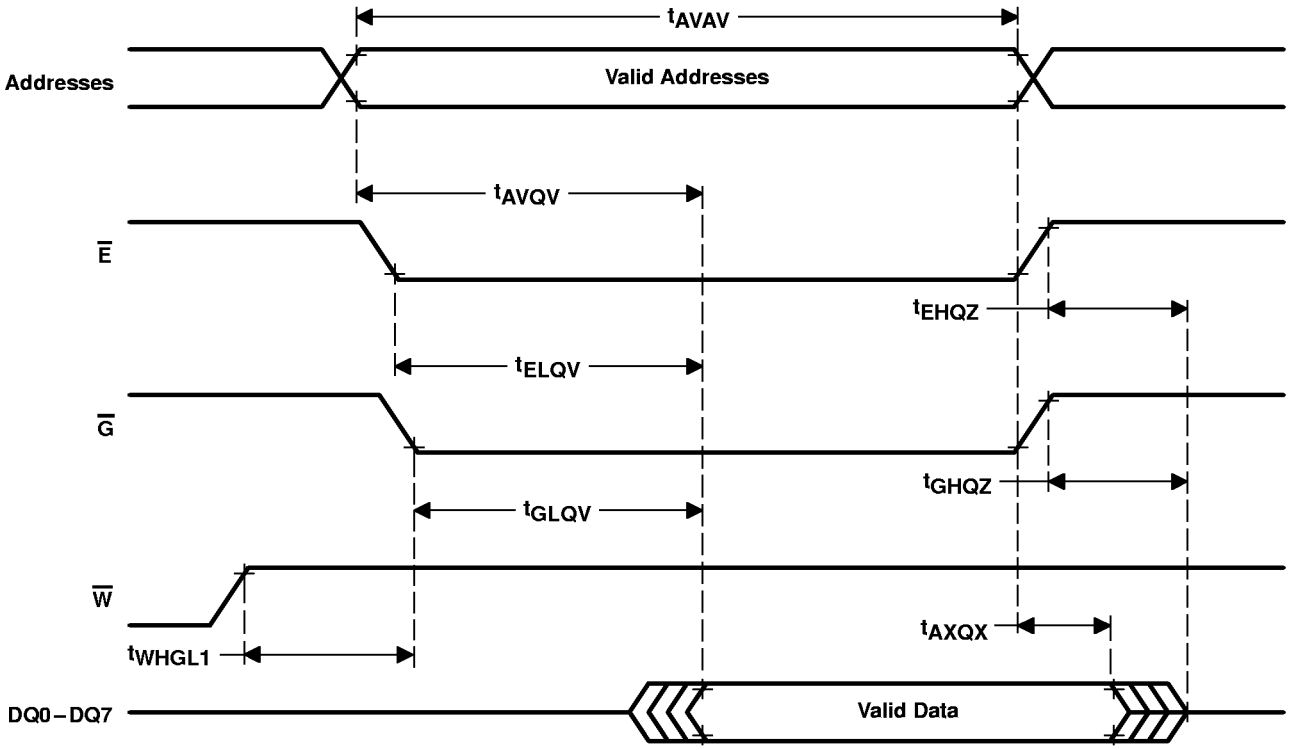


Figure 2. AC Waveform for Read Operation

write operation

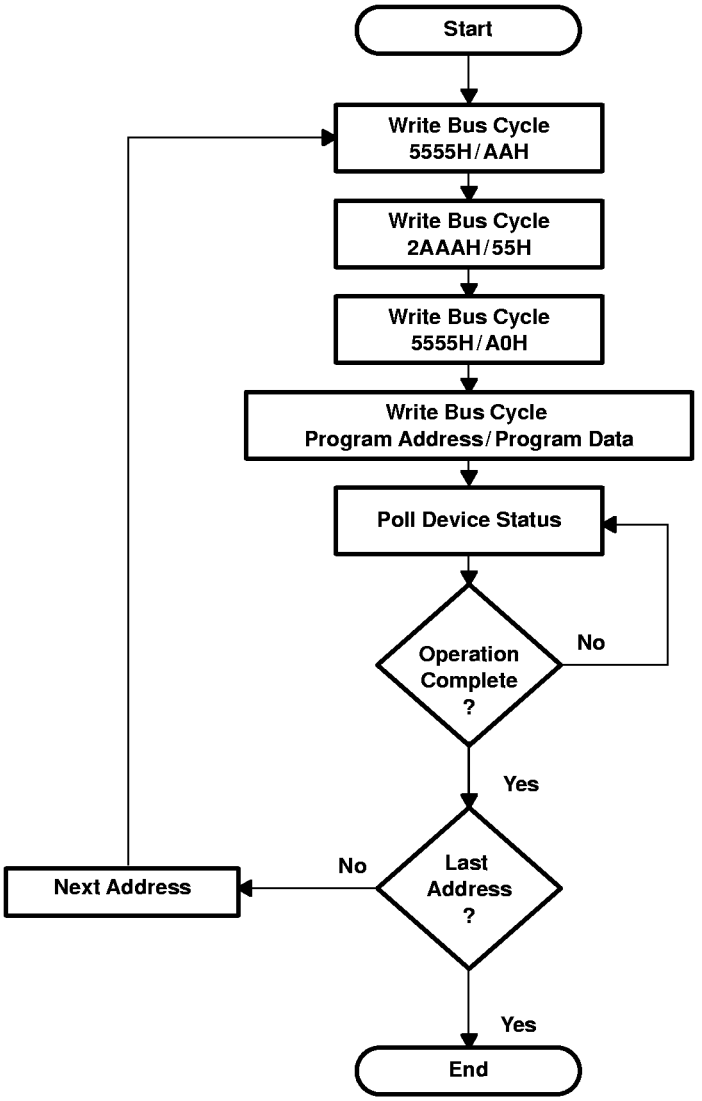
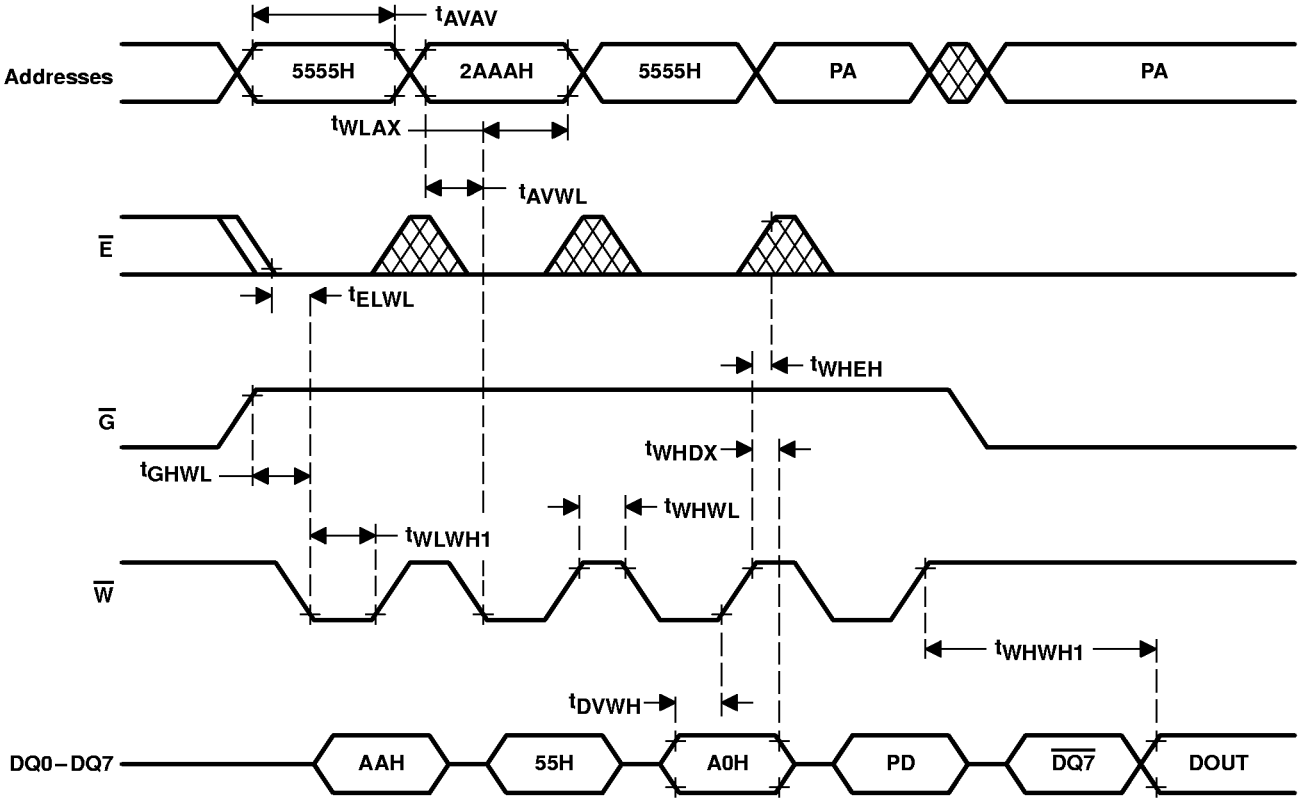


Figure 3. Byte-Program Algorithm

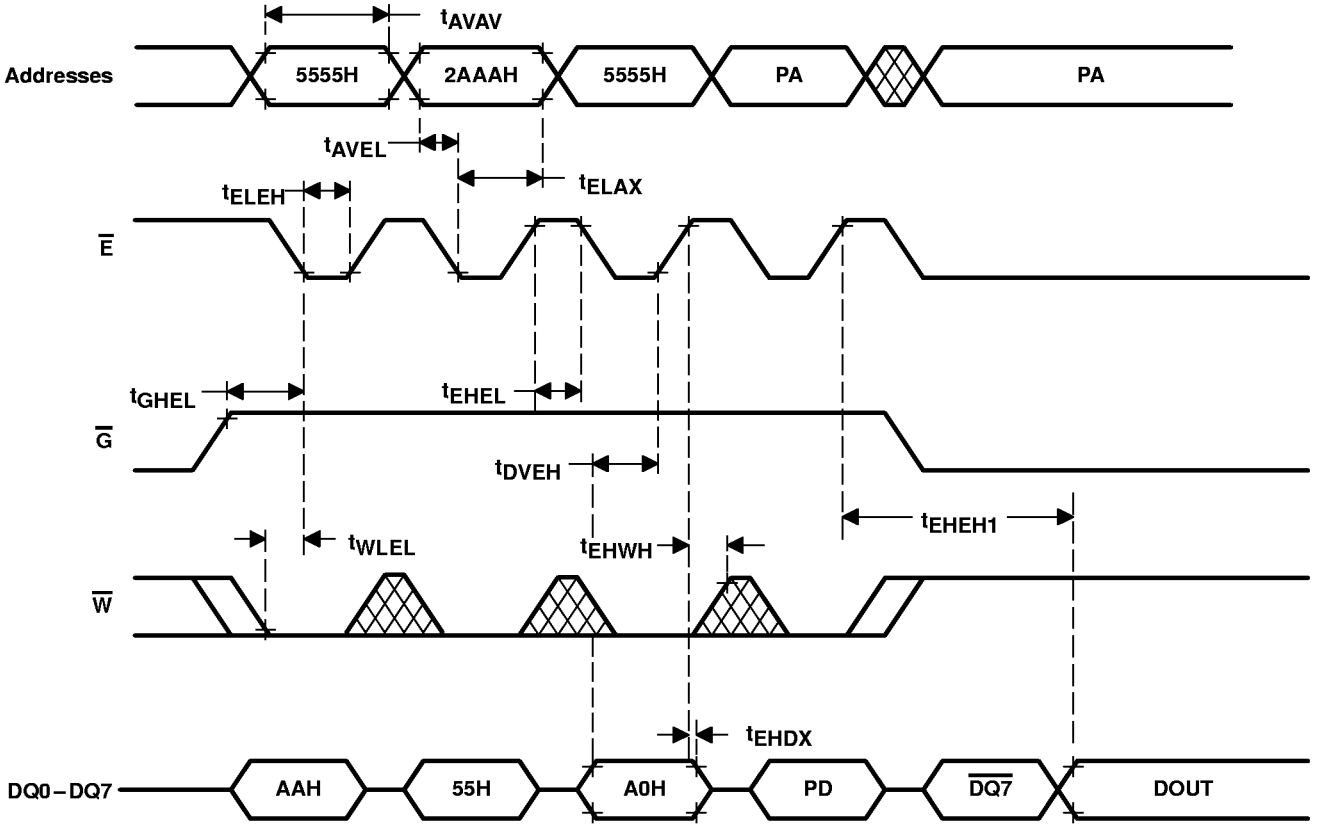
write operation (continued)



NOTES: A. PA = Address of the location to be programmed
B. PD = Data to be programmed
C. $\overline{DQ7}$ = Complement of data written to DQ7

Figure 4. AC Waveform for Byte-Program ($\overline{W}$-Controlled) Operation

write operation (continued)



NOTES: A. PA = Address of the location to be programmed
B. PD = Data to be programmed
C. $\overline{DQ7}$ = Complement of data written to DQ7

Figure 5. AC Waveform for Byte-Program (Alternate $\overline{E}$-Controlled) Operation

chip-erase operation

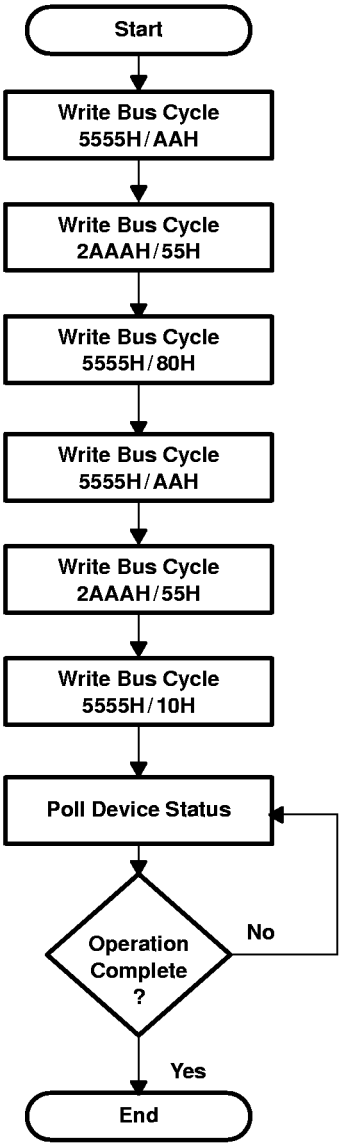
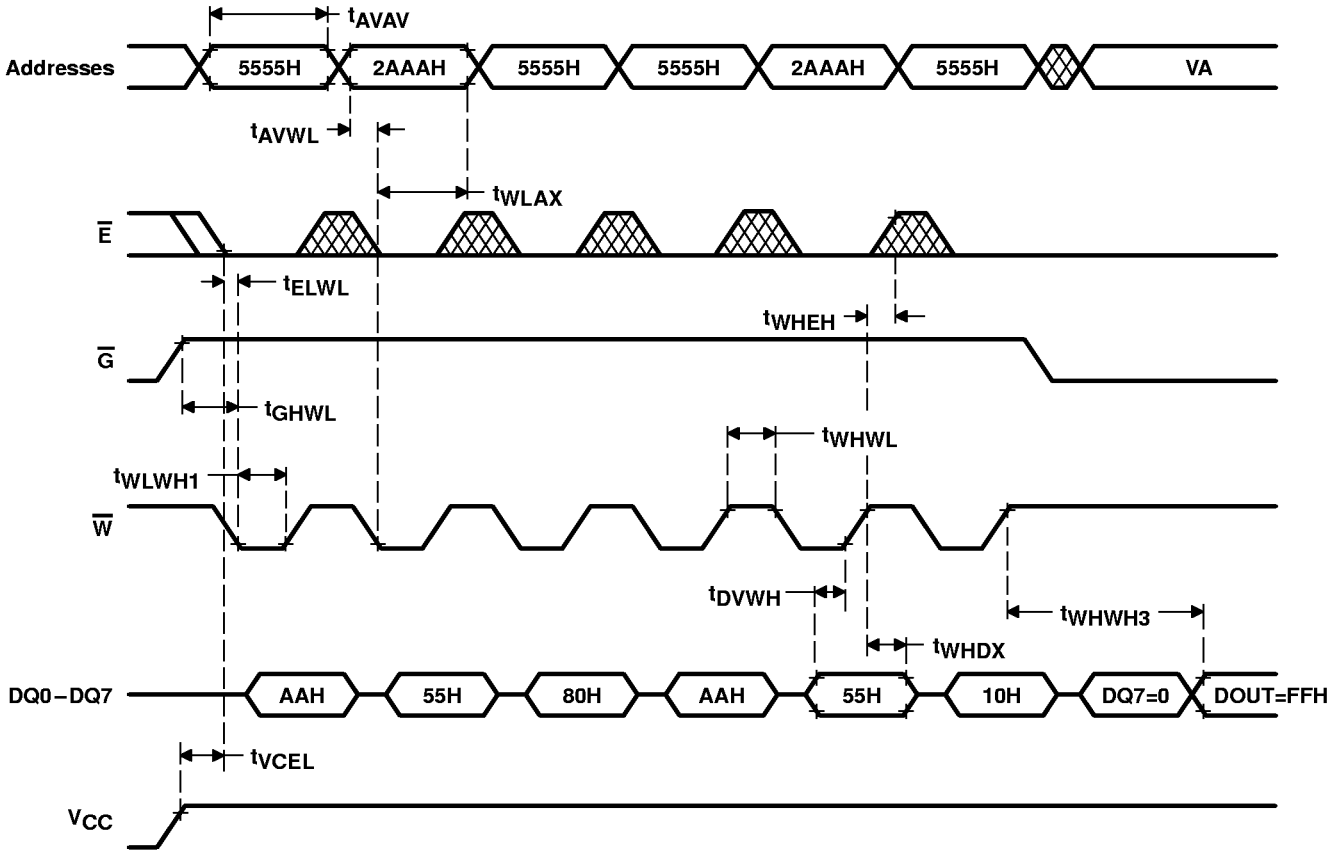


Figure 6. Chip-Erase Algorithm

chip-erase operation (continued)



NOTE A: VA = any valid address

Figure 7. AC Waveform for Chip-Erase Operation

sector-erase operation

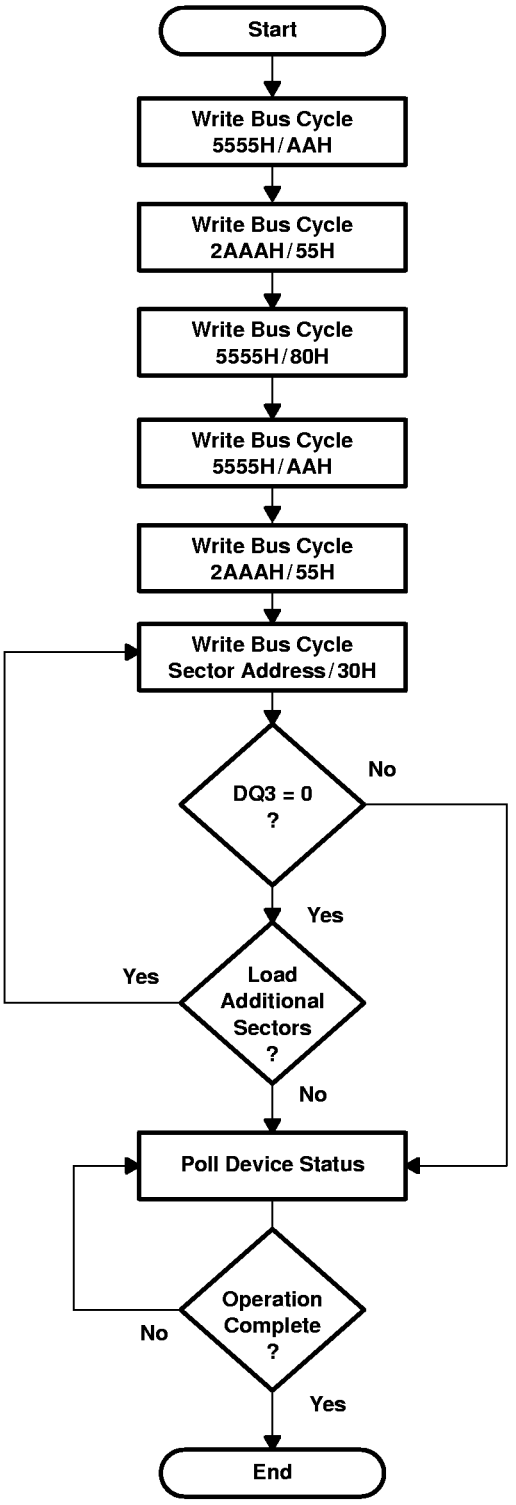
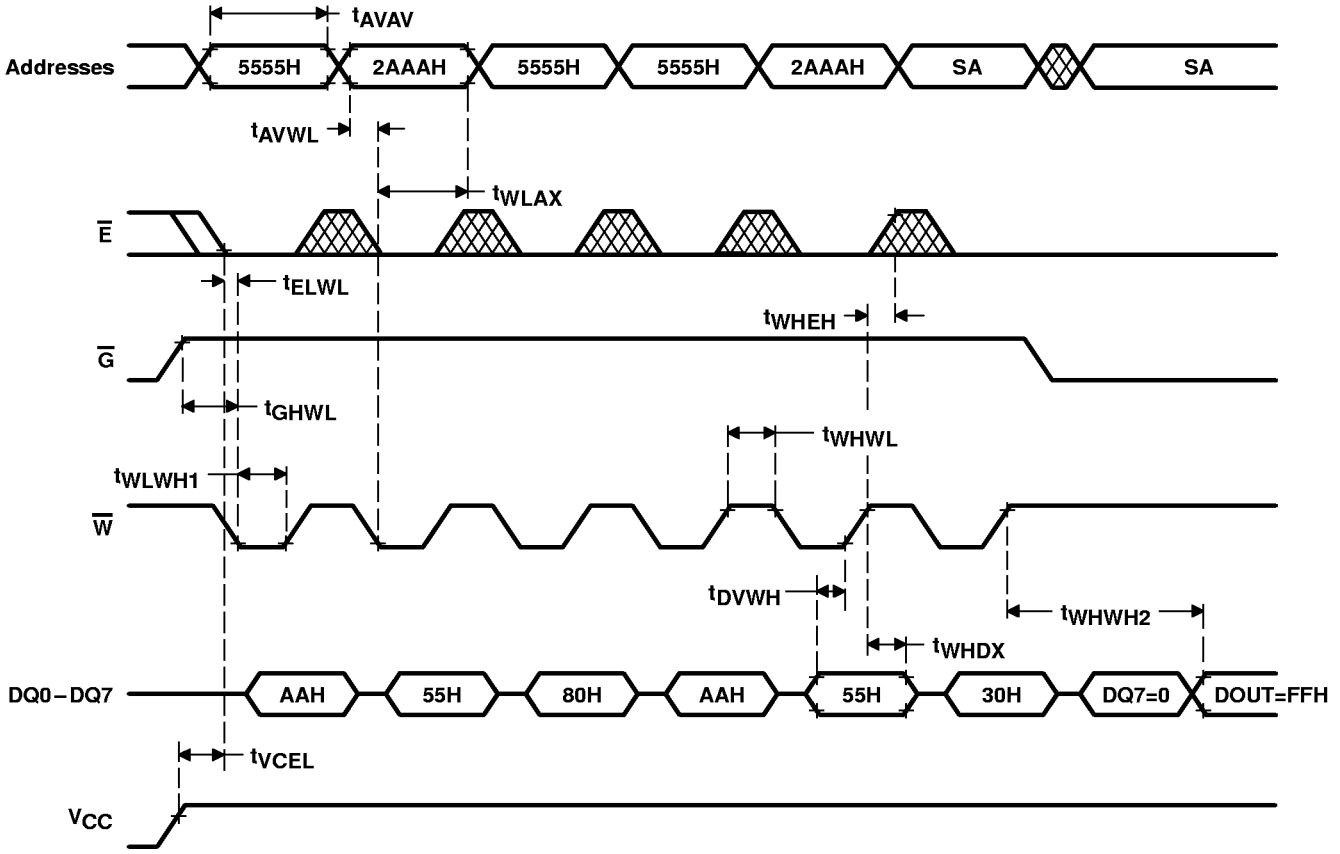


Figure 8. Sector-Erase Algorithm

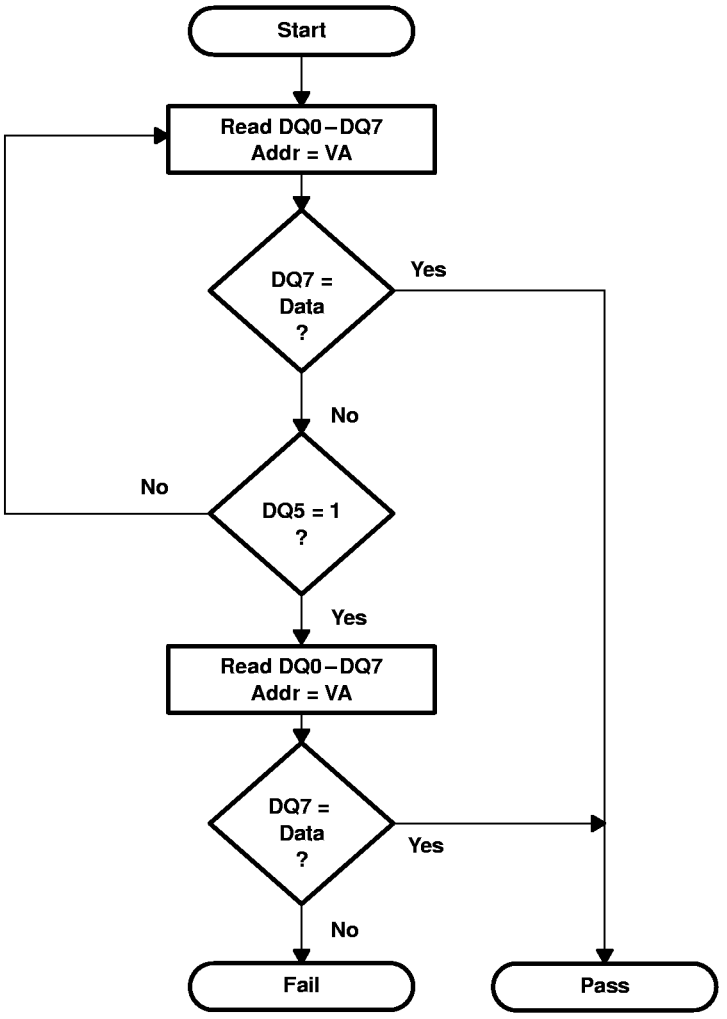
sector-erase operation (continued)



NOTE A: SA = Sector address to be erased

Figure 9. AC Waveform for Sector-Erase Operation

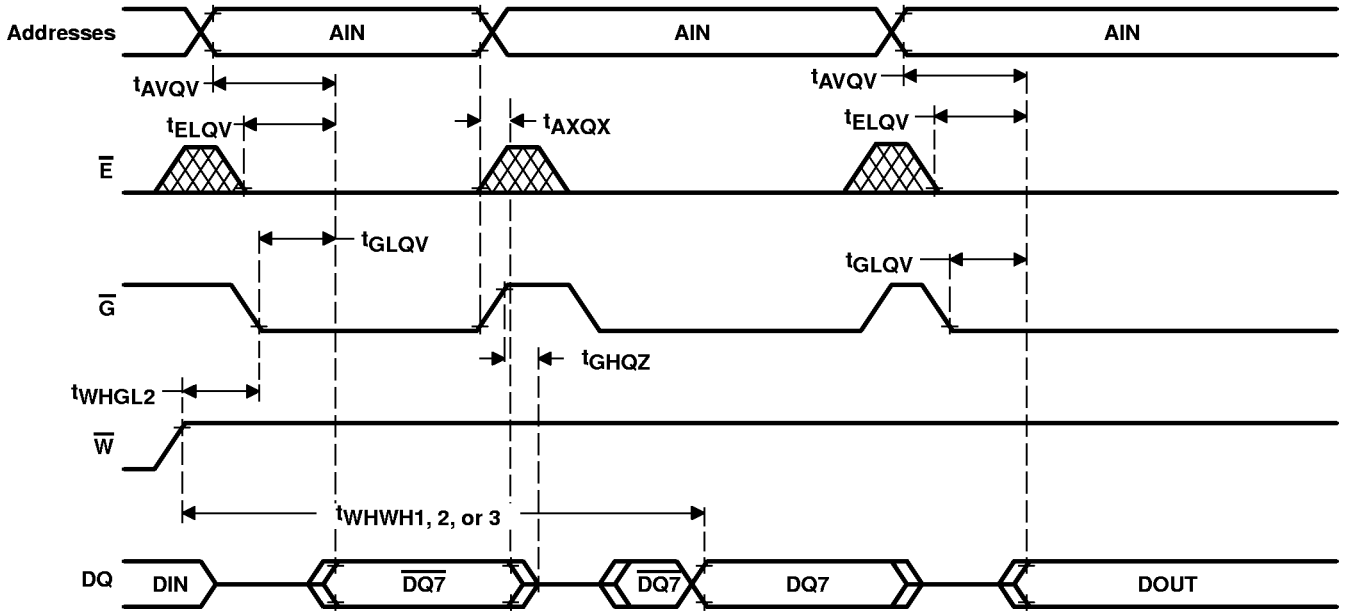
data-polling operation



NOTES: A. DQ7 is checked again after DQ5 is checked, even if DQ5 = 1.
B. VA = Program address for byte-programming
= Selected sector address for sector-erase
= Any valid address for chip-erase

Figure 10. Data-Polling Algorithm

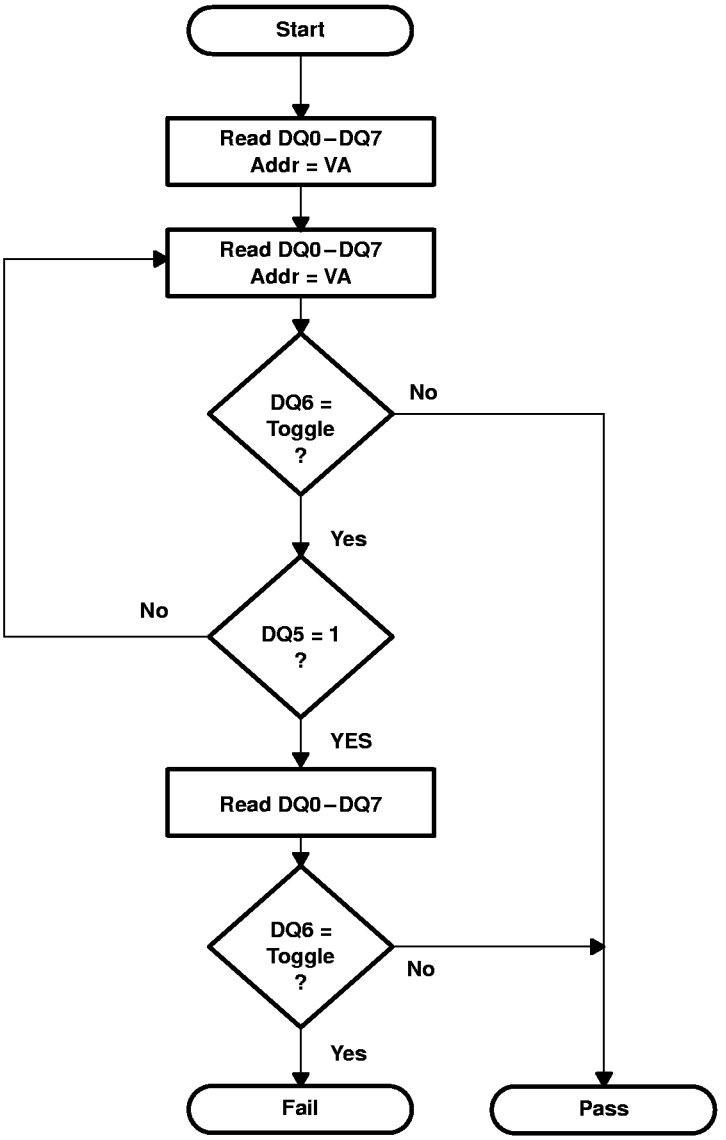
data-polling operation (continued)



NOTES: A. DIN = Last command data written to the device
B. $\overline{DQ7}$ = Complement of data written to DQ7
C. DOUT = Valid data output
D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation
E. The data-polling operation is valid for both $\overline{W}$- and $\overline{E}$-controlled byte-program, sector-erase, and chip-erase operations.

Figure 11. AC Waveform for Data-Polling Operation

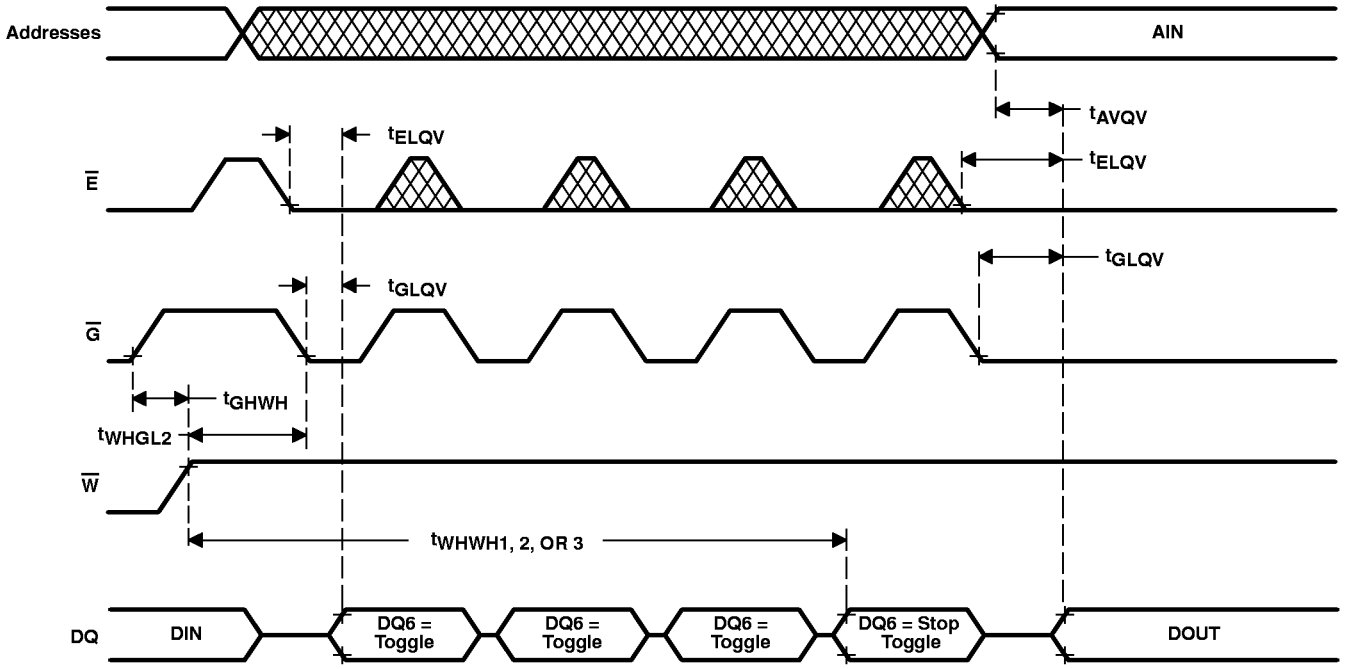
toggle-bit operation



NOTE A: DQ6 is checked again after DQ5 is checked, even if DQ5 = 1.

Figure 12. Toggle-Bit Algorithm

toggle-bit operation (continued)



NOTES: A. DIN = Last command data written to the device
B. DQ6 = Toggle bit output
C. DOUT = Valid data output
D. AIN = Valid address for byte-program, sector-erase, or chip-erase operation
E. The toggle-bit operation is valid for both $\overline{W}$- and $\overline{E}$-controlled byte-program, sector-erase, and chip-erase operations.

Figure 13. AC Waveform for Toggle-Bit Operation

sector-protect operation

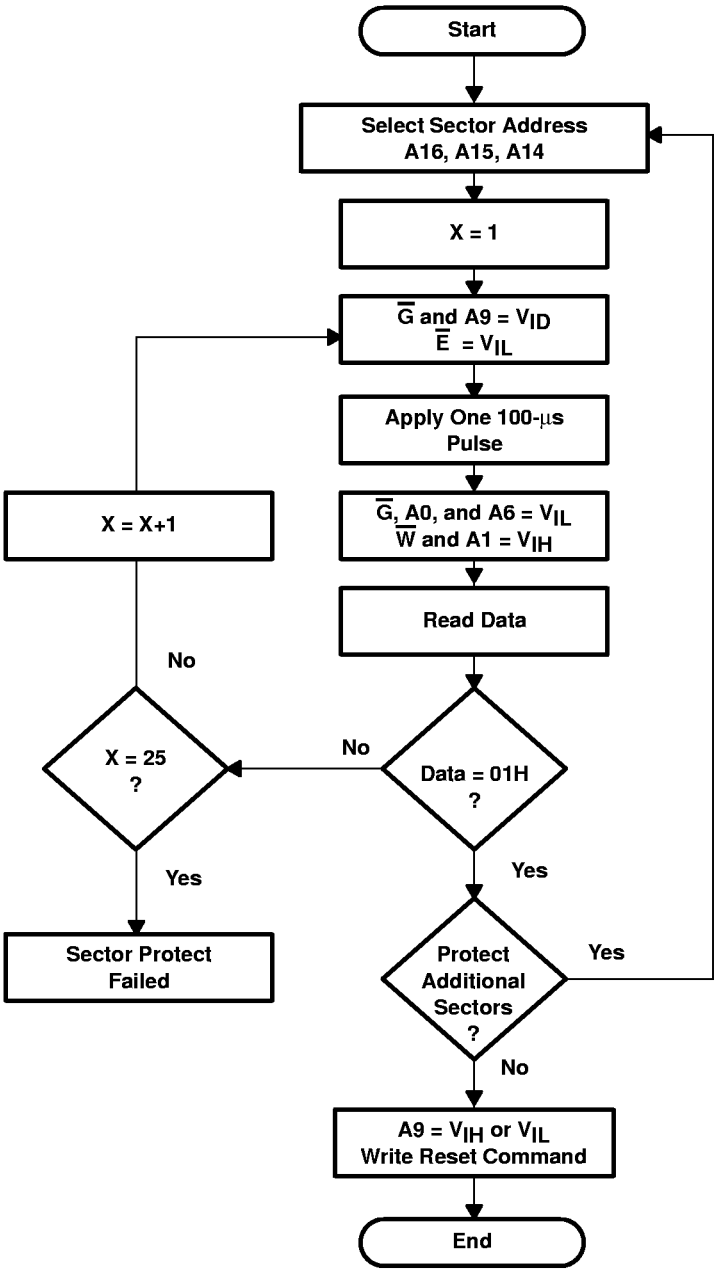
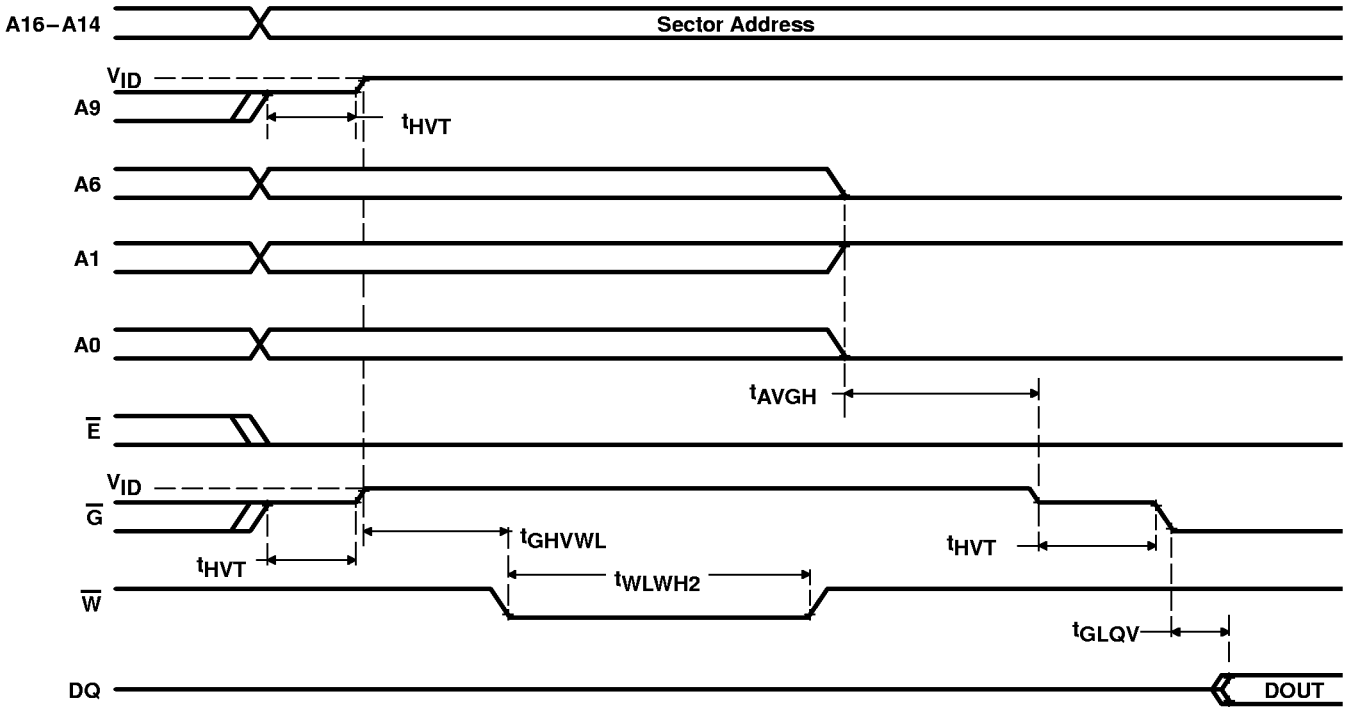


Figure 14. Sector-Protect Algorithm

sector-protect operation (continued)



NOTE A: DOUT = 00H if selected sector is not protected,
01H if the sector is protected

Figure 15. AC Waveform for Sector-Protect Operation

sector-unprotect operation

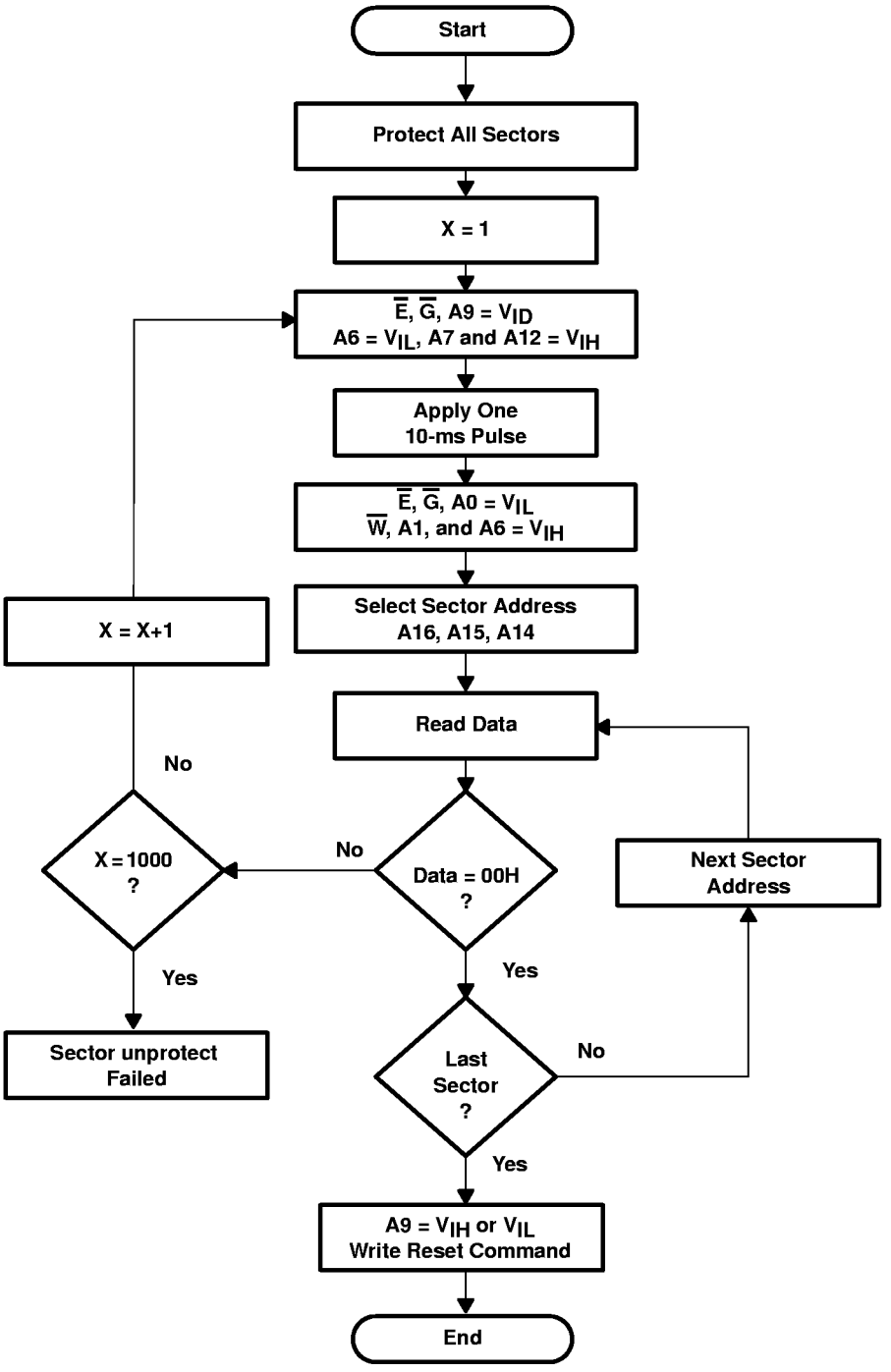
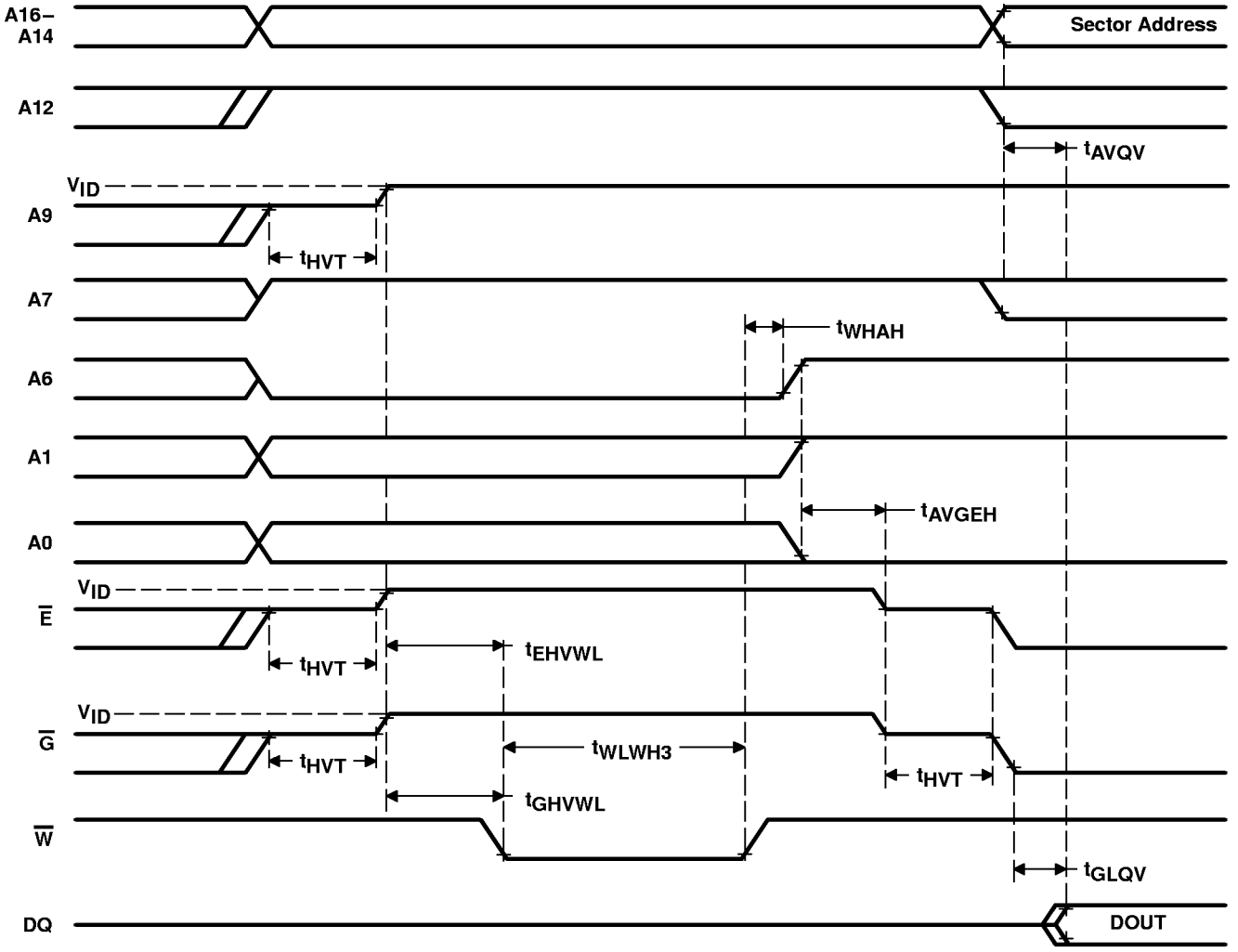


Figure 16. Sector-Unprotect Algorithm

sector-unprotect operation (continued)

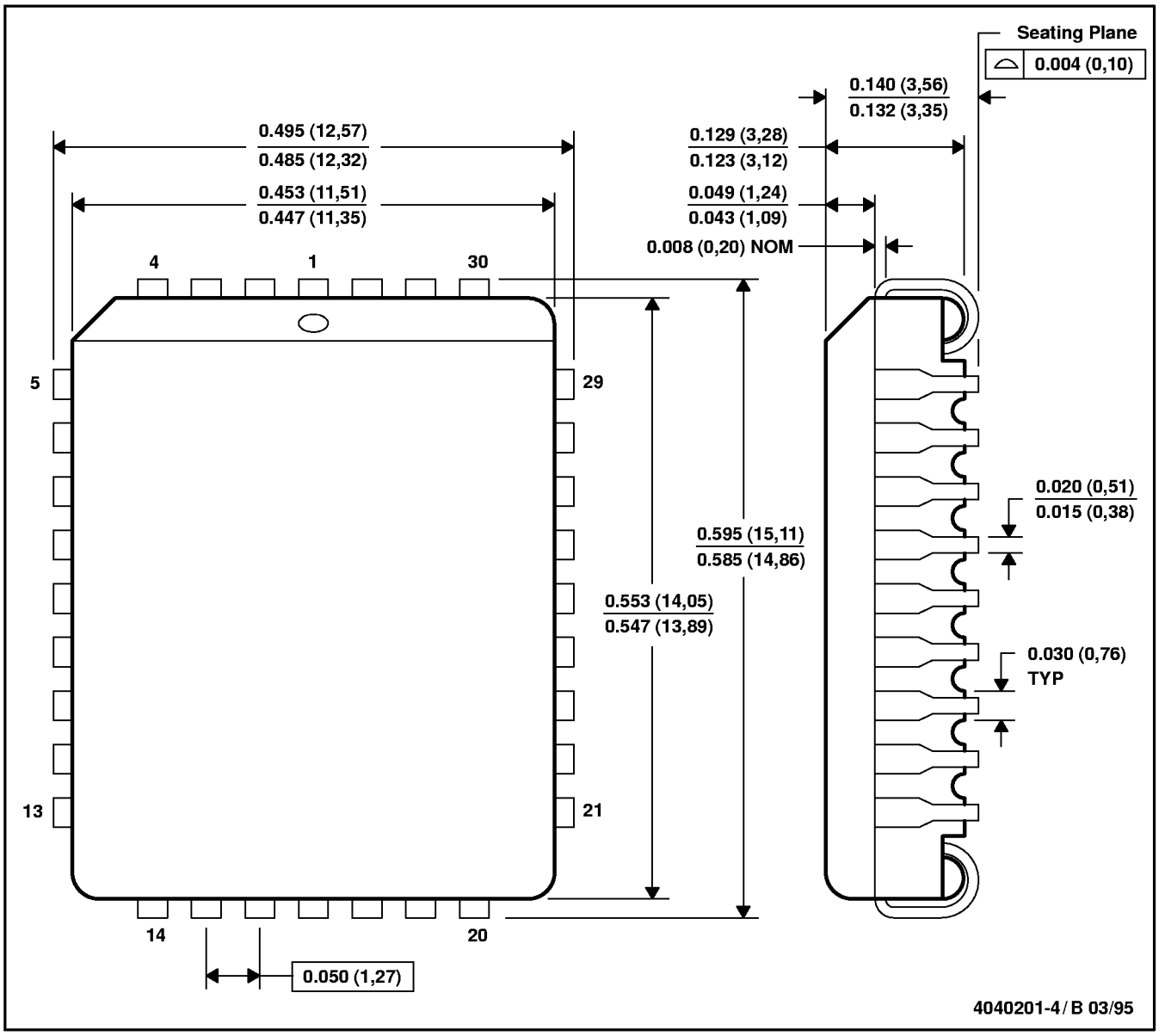


NOTE A: DOUT = 00H if selected sector is not protected,
01H if the sector is protected

Figure 17. AC Waveform for Sector-Unprotect Operation

MECHANICAL DATA

FM (R-PQCC-J32) **PLASTIC J-LEADED CHIP CARRIER**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-016

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