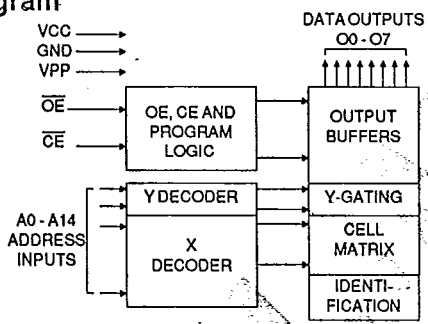


Features

- Wide Power Supply Range, 3.0 VDC to 5.5 VDC
- Compatible with JEDEC Standard AT27C256R
- Low Power 3-Volt CMOS Operation
  - 100  $\mu$ A max. Standby
  - 26mW max. Active at 3.3 MHz for Vcc = 3.3 VDC
  - 110mW max. Active at 5 MHz for Vcc = 5.5 VDC
- Read Access Time - 300ns
- Wide Selection of JEDEC Standard Packages Including OTP
  - 28-Lead 600 mil Cerdip and OTP Plastic DIP or SOIC
  - 32-Pad LCC and OTP PLCC
- High Reliability CMOS Technology
  - 2000V ESD Protection
  - 200mA Latchup Immunity
- Rapid Programming - 100 $\mu$ s/byte (typical)
- Two-line Control
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Block Diagram



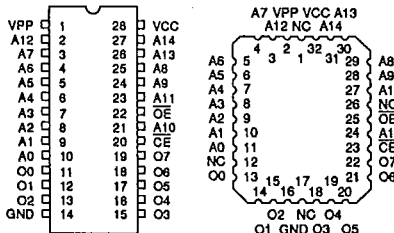
Description

The AT27LV256R chip is a low power, low voltage 262,144 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized as 32K x 8 bits. It requires only one supply in the range of 3.0 to 5.5 VDC in normal read mode operation, making it ideal for battery powered systems.

With a typical power draw of only 18mW at 3.3 MHz and Vcc at 3.3 VDC, the AT27LV256R will draw less than one fifth the power of a standard 5 volt EPROM. Standby mode supply current is typically less than 20 $\mu$ A.

Pin Configurations

Pin Name	Function
A0-A14	Addresses
O0-O7	Outputs
CE	Chip Enable
OE	Output Enable
NC	No Connect



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT



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T-46-13-25

256K (32K x 8)  
Low Voltage  
UV  
Erasable  
CMOS  
EPROM

Preliminary



T-46-13-29

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## Description (Continued)

The AT27LV256R comes in a choice of industry standard JEDEC-approved ceramic packages including; 28-pin DIP ceramic or one time programmable (OTP) plastic, 28-pin OTP plastic small outline (SOIC) and 32-pad leadless chip carrier (LCC) or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to give designers the flexibility to prevent bus contention.

The AT27LV256R operating with  $V_{CC}$  at 3.0 VDC produces TTL level outputs that are compatible with standard TTL logic devices operating at  $V_{CC} = 5.0$  VDC.

Atmel's 27LV256R has additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 $\mu$ s/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages. The AT27LV256R programs identically as an AT27C256R.

## Erase Characteristics

The entire memory array of the AT27LV256R is erased (all outputs read as  $V_{OH}$ ) after exposure to ultraviolet light at a wavelength of 2537 Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu$ W/cm<sup>2</sup> intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W-sec/cm<sup>2</sup>. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

## Absolute Maximum Ratings\*

Temperature Under Bias .....	-40°C to +85°C
Storage Temperature .....	-65°C to +125°C
Voltage on Any Pin with Respect to Ground .....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on A9 with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
V <sub>PP</sub> Supply Voltage with Respect to Ground .....	-2.0V to +14.0V <sup>(1)</sup>
Integrated UV Erase Dose .....	7258 W-sec/cm <sup>2</sup>

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Notes:

1. Minimum voltage is -0.6V dc which may undershoot to -2.0V for pulses of less than 20ns. Maximum output pin voltage is 6.5V dc which may overshoot to +7.0V for pulses of less than 20ns.

## Operating Modes

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	Ai	V <sub>PP</sub>	V <sub>CC</sub>	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	Ai	V <sub>CC</sub>	V <sub>CC</sub>	DOUT
Output Disable	V <sub>IL</sub>	V <sub>IH</sub>	X <sup>(1)</sup>	V <sub>CC</sub>	V <sub>CC</sub>	High Z
Standby	V <sub>IH</sub>	X	X <sup>(5)</sup>	V <sub>CC</sub>	V <sub>CC</sub>	High Z
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>	V <sub>CC</sub>	DIN
PGM Verify <sup>(2)</sup>	X	V <sub>IL</sub>	Ai	V <sub>PP</sub>	V <sub>CC</sub> <sup>(2)</sup>	DOUT
Optional PGM Verify <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	Ai	V <sub>CC</sub>	V <sub>CC</sub> <sup>(2)</sup>	DOUT
PGM Inhibit <sup>(2)</sup>	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	V <sub>CC</sub> <sup>(2)</sup>	High Z
Product Identification <sup>(2),(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A9=V <sub>IH</sub> <sup>(3)</sup> A0=V <sub>IH</sub> or V <sub>IL</sub> A1-A14=V <sub>IL</sub>	V <sub>CC</sub>	V <sub>CC</sub> <sup>(2)</sup>	Identification Code

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Refer to Programming characteristics. Programming modes require  $V_{CC} > 4.5$  V.
  3. V<sub>IH</sub> = 12.0  $\pm$  0.5V.
  4. Two identifier bytes may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A9 which is set to V<sub>IH</sub> and

A0 which is toggled low (V<sub>IL</sub>) to select the Manufacturer's Identification byte and high (V<sub>IH</sub>) to select the Device Code byte.

5. Standby V<sub>CC</sub> Current (I<sub>SB</sub>) is specified with V<sub>PP</sub>=V<sub>CC</sub>. V<sub>CC</sub> > V<sub>PP</sub> will cause a slight increase in I<sub>SB</sub>.

## AT27LV256R

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## D.C. and A.C. Operating Conditions for Read Operation

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AT27LV256R		
-30		
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
Vcc Power Supply		3.0V to 5.5V

D.C. and Operating Characteristics for Read Operation  
(VCC = 3.0V to 5.5V unless otherwise specified)

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = -0.1V to V <sub>CC</sub> +1V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = -0.1V to V <sub>CC</sub> +0.1V		10	μA
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub> -0.7V to V <sub>CC</sub> +0.3V		10	μA
I <sub>SB</sub>	V <sub>CC</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), CE = V <sub>CC</sub> -0.3 to V <sub>CC</sub> +1.0V		100	μA
		I <sub>SB2</sub> (TTL), CE = 2.0 to V <sub>CC</sub> +1.0V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	I <sub>CC1</sub> f = 5MHz, I <sub>OUT</sub> = 0mA, CE = V <sub>IL</sub> , V <sub>CC</sub> = 5.5V	Com.	20	mA
			Ind.	25	mA
		I <sub>CC2</sub> f = 3.33MHz, I <sub>OUT</sub> = 0mA, CE = V <sub>IL</sub> , V <sub>CC</sub> = 3.3V	Com.	8	mA
			Ind.	10	mA
V <sub>IL</sub>	Input Low Voltage	V <sub>IL1</sub> 4.5 ≤ V <sub>CC</sub> ≤ 5.5V	-0.6	0.8	V
		V <sub>IL2</sub> 3.0 ≤ V <sub>CC</sub> < 4.5V	-0.6	0.6	V
V <sub>IH</sub>	Input High Voltage		2.0	6.5	V
V <sub>OL</sub>	Output Low Voltage	V <sub>OL1</sub> I <sub>OL</sub> = 2.1mA, V <sub>CC</sub> = 4.5V		.45	V
		V <sub>OL2</sub> I <sub>OL</sub> = 1.0mA, V <sub>CC</sub> = 3.0V		0.3	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -100μA	V <sub>CC</sub> -0.3		V
		I <sub>OH</sub> = -400μA	2.4		V

Notes: 1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, and removed simultaneously or after V<sub>PP</sub>.2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP</sub>.

## A.C. Characteristics for Read Operation (VCC = 3.0V to 5.5V)

					AT27LV256R		Units
					-30		
Symbol	Parameter	Condition			Min	Max	
t <sub>ACC</sub> <sup>(3)</sup>	Address to Output Delay	$\overline{CE}=\overline{OE}=V_{IL}$	Com.		270	ns	
			Ind.		270	ns	
t <sub>CE</sub> <sup>(2)</sup>	$\overline{CE}$ to Output Delay	$\overline{OE}=V_{IL}$			300	ns	
t <sub>OE</sub> <sup>(2,3)</sup>	$\overline{OE}$ to Output Delay	$\overline{CE}=V_{IL}$			150	ns	
t <sub>DF</sub> <sup>(4,5)</sup>	$\overline{OE}$ High to Output Float	$\overline{CE}=V_{IL}$			100	ns	
t <sub>OH</sub>	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ , whichever occurred first	$\overline{CE}=\overline{OE}=V_{IL}$			0	ns	

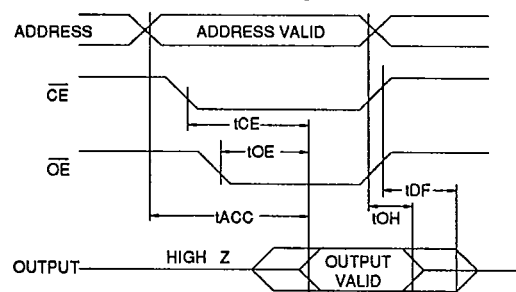
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.





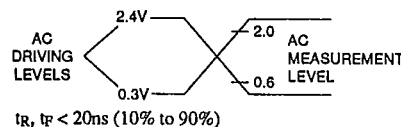
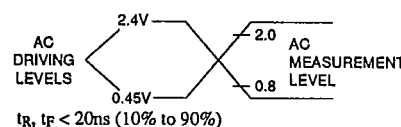
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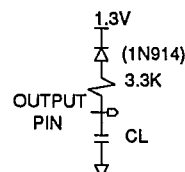
A.C. Waveforms for Read Operation <sup>(1)</sup>

## Notes:

- 3V timing measurement references are 0.6V and 2.0V. Input AC driving levels are 0.3V and 2.4V. See Input Test Waveforms and Measurement Levels.
- $\overline{OE}$  may be delayed up to  $t_{CE-t_{OE}}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
- $\overline{OE}$  may be delayed up to  $t_{ACC-t_{OE}}$  after the address is valid without impact on  $t_{ACC}$ .
- This parameter is only sampled and is not 100% tested.
- Output float is defined as the point when data is no longer driven.

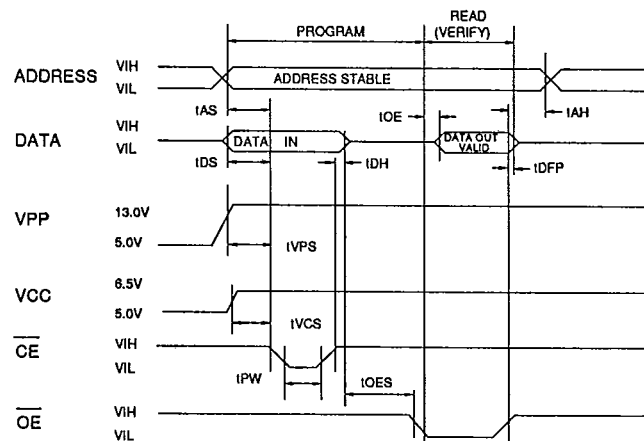
Input Test Waveforms and Measurement Levels  
( $V_{CC} = 3.0V$ )( $V_{CC} = 5.5V$ )

## Output Test Load

Note:  $C_L = 100pF$  including jig capacitance.Pin Capacitance ( $f=1MHz$   $T=25^\circ C$ ) <sup>(1)</sup>

	Typ	Max	Units	Conditions
$C_{IN}$	4	8	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

Notes: 1. Typical values for 5V supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms <sup>(1)</sup>

## Notes:

- The Input Timing Reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
- $t_{OE}$  and  $t_{IDFP}$  are characteristics of the device but must be accommodated by the programmer.
- When programming the AT27LV256R a 0.1 $\mu F$  capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.

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**D.C. Programming Characteristics**  
T<sub>A</sub>=25±5°C, V<sub>CC</sub>=6.5±0.25V, V<sub>PP</sub>=13.0±0.25V

Sym- bol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> =V <sub>IL</sub> , V <sub>IH</sub>		10	μA
V <sub>IL</sub>	Input Low Level	(All Inputs)	-0.6	0.8	V
V <sub>IH</sub>	Input High Level		2.0	V <sub>CC</sub> +1	V
V <sub>OL</sub>	Output Low Volt.	I <sub>OL</sub> =2.1mA		.45	V
V <sub>OH</sub>	Output High Volt.	I <sub>OH</sub> =-400μA	2.4		V
I <sub>CC2</sub>	V <sub>CC</sub> Supply Current (Program and Verify)			25	mA
I <sub>PP2</sub>	V <sub>PP</sub> Current	C <sub>EE</sub> =V <sub>IL</sub>		25	mA
V <sub>ID</sub>	A9 Product Identifi- cation Voltage		11.5	12.5	V

**A.C. Programming Characteristics**  
T<sub>A</sub>=25±5°C, V<sub>CC</sub>=6.5±0.25V, V<sub>PP</sub>=13.0±0.25V

Sym- bol	Parameter	Test Conditions* (see Note 1)	Limits		Units
			Min	Max	
t <sub>AS</sub>	Address Setup Time		2		μs
t <sub>OES</sub>	OE Setup Time		2		μs
t <sub>DS</sub>	Data Setup Time		2		μs
t <sub>AH</sub>	Address Hold Time		0		μs
t <sub>DH</sub>	Data Hold Time		2		μs
t <sub>DFP</sub>	OE High to Out- put Float Delay	(Note 2)	0	130	ns
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time		2		μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time		2		μs
t <sub>PW</sub>	OE Program Pulse Width	(Note 3)	95	105	μs
t <sub>OE</sub>	Data Valid from OE	(Note 2)		150	ns

\*A.C. Conditions of Test:  
Input Rise and Fall Times (10% to 90%) .....20ns  
Input Pulse Levels .....0.45V to 2.4V  
Input Timing Reference Level .....0.8V to 2.0V  
Output Timing Reference Level .....0.8V to 2.0V

- Notes:
1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed si-  
multaneously or after V<sub>PP</sub>.
  2. This parameter is only sampled and is not 100% tested.  
Output Float is defined as the point where data is no longer  
driven — see timing diagram.
  3. Program Pulse width tolerance is 100μsec±5%.

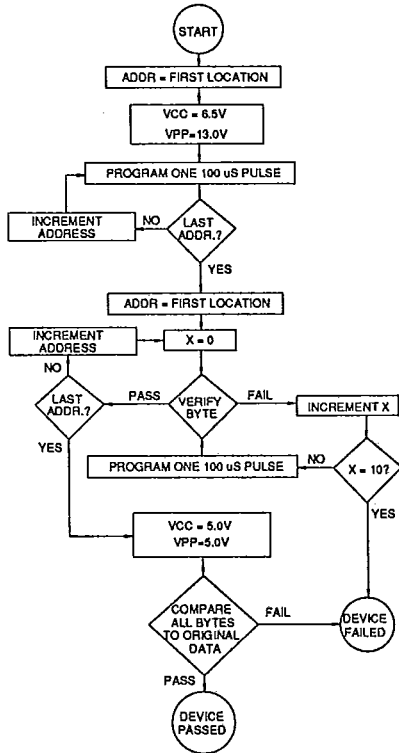
**Atmel's 27LV256R Integrated  
Product Identification Code<sup>(1)</sup>**

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	1	0	0	0	1	1	0	0	8C

Note: 1. The AT27LV256R has the same Product Identification Code as the AT27C256R. Both are programming compatible.

**Rapid Programming Algorithm**

A 100μs  $\overline{CE}$  pulse width is used to program. The address is set to the first location. V<sub>CC</sub> is raised to 6.5V and V<sub>PP</sub> is raised to 13.0V. Each address is first programmed with one 100μs  $\overline{CE}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V<sub>PP</sub> is then lowered to 5.0V and V<sub>CC</sub> to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

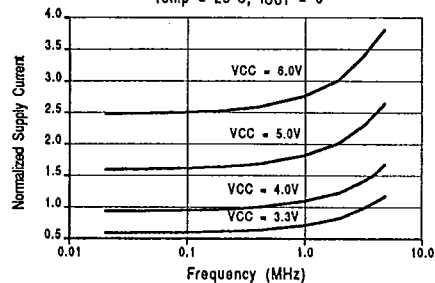




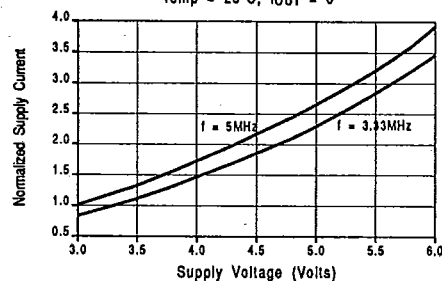
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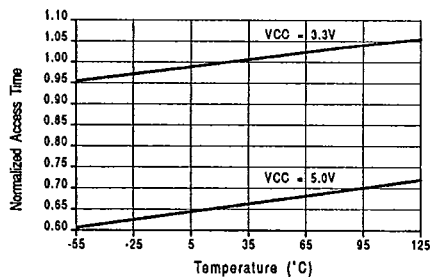
NORMALIZED SUPPLY CURRENT vs. FREQUENCY

Temp = 25°C, I<sub>OUT</sub> = 0

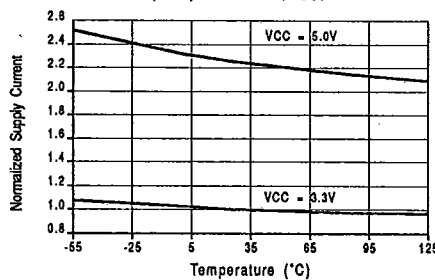
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE

Temp = 25°C, I<sub>OUT</sub> = 0

NORMALIZED ACCESS TIME vs. TEMPERATURE

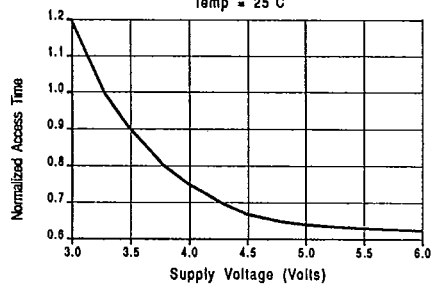


NORMALIZED SUPPLY CURRENT vs. TEMPERATURE

Frequency = 3.33MHz, I<sub>OUT</sub> = 0

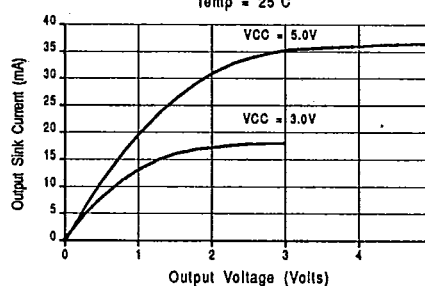
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE

Temp = 25°C



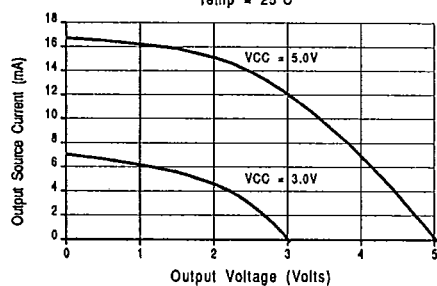
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE

Temp = 25°C



AT27LV256R

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## Ordering Information

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active (3.3)	Standby			
270	8	0.1	AT27LV256R-30DC AT27LV256R-30JC AT27LV256R-30LC AT27LV256R-30PC AT27LV256R-30RC	28DW6 32J 32LW 28P6 28R	Commercial (0°C to 70°C)
270	10	0.1	AT27LV256R-30DI AT27LV256R-30LI	28DW6 32LW	Industrial (-40°C to 85°C)

## Package Type

28DW6	28 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
32LW	32 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package OTP (PDIP)
28R	28 Lead, 0.330" Wide, Plastic Gull Wing Small Outline OTP (SOIC)

**ATMEL**