



128Kx8 Monolithic SRAM, SMD 5962-89598

FEATURES

- Access Times of 15*, 17, 20, 25, 35, 45, 55ns
- Battery Back-up Operation
 - 2V Data Retention (EDI88130LPS)
- $\overline{CS}1$, $CS2$ & $\overline{OE}$ Functions for Bus Control
- Inputs and Outputs Directly TTL Compatible
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Thru-hole and Surface Mount Packages JEDEC Pinout
 - 32 pin Sidebrazed Ceramic DIP, 400 mil (Package 102)
 - 32 pin Sidebrazed Ceramic DIP, 600 mil (Package 9)
 - 32 lead Ceramic SOJ (Package 140)
 - 32 pad Ceramic Quad LCC (Package 12)
 - 32 pad Ceramic LCC (Package 141)
 - 32 lead Ceramic Flatpack (Package 142)
- Single +5V ($\pm 10\%$) Supply Operation

The EDI88130CS is a high speed, high performance, 128Kx8 bits monolithic Static RAM.

An additional chip enable line provides system memory security during power down in non-battery backed up systems and memory banking in high speed battery backed systems where large multiple pages of memory are required.

The EDI88130CS has eight bi-directional input-output lines to provide simultaneous access to all bits in a word.

A low power version, EDI88130LPS, offers a 2V data retention function for battery back-up applications.

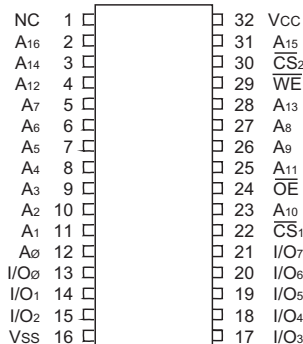
Military product is available compliant to MIL-PRF-38535.

**15ns access time is advanced information, contact factory for availability.*

FIG. 1 PIN CONFIGURATION

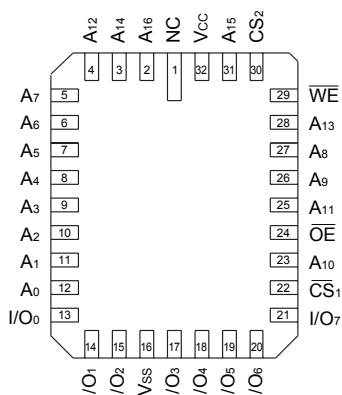
32 DIP 32 SOJ 32 CLCC 32 FLATPACK

TOP VIEW



32 QUAD LCC

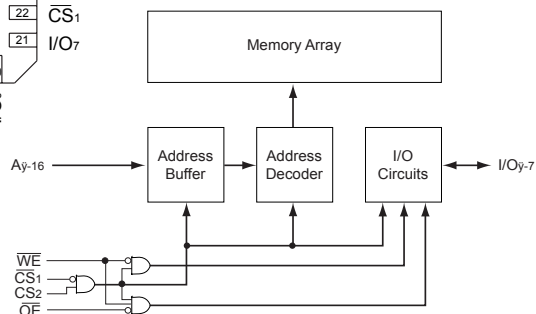
TOP VIEW



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-16	Address Inputs
WE	Write Enable
CS1, CS2	Chip Selects
OE	Output Enable
VCC	Power (+5V $\pm 10\%$)
VSS	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to Vss	-0.2 to 7.0	V
Operating Temperature T _A (Ambient)		
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Ceramic	-65 to +150	°C
Power Dissipation	1.7	W
Output Current	40	mA
Junction Temperature, T _J	175	°C

NOTE:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	—	+0.8	V

TRUTH TABLE

OE	CS ₁	CS ₂	WE	Mode	Output	Power
X	H	X	X	Standby	High Z	I _{CC2} , I _{CC3}
X	X	L	X	Standby	High Z	I _{CC2} , I _{CC3}
H	L	H	H	Output Deselect	High Z	I _{CC1}
L	L	H	H	Read	Data Out	I _{CC1}
X	L	H	L	Write	Data In	I _{CC1}

CAPACITANCE (T_A = +25°C)

Parameter	Symbol	Condition	Max		Unit
			LCC	CSOJ, DIP, Flatpack	
Address Lines	C _i	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	6	12	pF
Data Lines	C _o	V _{OUT} = V _{CC} or V _{SS} , f = 1.0MHz	8	14	pF

These parameters are sampled, not 100% tested.

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{CC}	—	—	±5	μA
Output Leakage Current	I _{LO}	V _{I/O} = 0V to V _{CC}	—	—	±10	μA
Operating Power Supply Current	I _{CC1}	(15-17ns)	—	—	300	mA
		(20ns)	—	—	225	mA
		(25-55ns)	—	—	200	mA
Standby (TTL) Power Supply Current	I _{CC2}	CS ₁ ≥ V _{IH} and/or CS ₂ ≤ V _{IL} , (17-55ns)	—	—	25	mA
		V _{IN} ≥ V _{IH} or ≤ V _{IL} (15ns)	—	—	60	mA
Full Standby Power Supply Current	I _{CC3}	CS ₁ ≥ V _{CC} - 0.2V and/or CS ₂ ≤ 0.2V, CS (17-55ns)	—	3	10	mA
		V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V, CS (15ns)	—	—	15	mA
		LPS	—	—	5	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V

AC TEST CONDITIONS

Figure 1

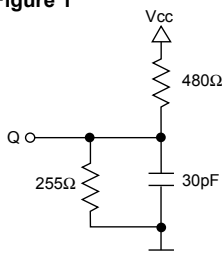
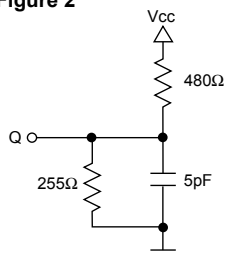


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, C_L = 5pF Figure 2)



AC CHARACTERISTICS – READ CYCLE (15 TO 20ns) (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	15		17		20		ns
Address Access Time	t _{AVQV}	t _{AA}		15		17		20	ns
Chip Enable Access Time	t _{E1LQV}	t _{ACS}		15		17		20	ns
	t _{E2HQV}	t _{ACS}		15		17		20	ns
Chip Enable to Output in Low Z (1)	t _{E1LQX}	t _{CLZ}	5		5		5		ns
	t _{E2HQX}	t _{CLZ}	5		5		5		ns
Chip Disable to Output in Low Z (1)	t _{E1HQZ}	t _{CHZ}		6		7		8	ns
	t _{E2LQZ}	t _{CHZ}		6		7		8	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	3		3		3		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		6		6		7	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}		5		6		8	ns
Chip Enable to Power Up (1)	t _{E1LICCH}	t _{PU}	0		0		0		ns
	t _{E2HICCH}	t _{PU}	0		0		0		ns
Chip Enable to Power Down (1)	t _{E1HICCL}	t _{PD}		15		17		20	ns
	t _{E2LICCL}	t _{PD}		15		17		20	ns

1. This parameter is guaranteed by design but not tested.

* 15ns access time is advanced information, contact factory for availability.

AC CHARACTERISTICS – READ CYCLE (25 TO 55ns) (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	25		35		45		55		ns
Address Access Time	t _{AVQV}	t _{AA}		25		35		45		55	ns
Chip Enable Access Time	t _{E1LQV}	t _{ACS}		25		35		45		55	ns
Chip Enable Access Time	t _{E2HQV}	t _{ACS}		25		35		45		55	ns
Chip Enable to Output in Low Z (1)	t _{E1LQX}	t _{CLZ}	5		5		5		5		ns
	t _{E2HQX}	t _{CLZ}	5		5		5		5		ns
Chip Disable to Output in Low Z (1)	t _{E1HQZ}	t _{CHZ}		10		15		20		20	ns
	t _{E2LQZ}	t _{CHZ}		10		15		20		20	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	0		0		0		0		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		10		15		20		25	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		0		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}		10		15		20		20	ns
Chip Enable to Power Up (1)	t _{E1LICCH}	t _{PU}	0		0		0		0		ns
	t _{E2HICCH}	t _{PU}	0		0		0		0		ns
Chip Enable to Power Down (1)	t _{E1HICCL}	t _{PD}		25		35		45		55	ns
	t _{E2LICCL}	t _{PD}		25		35		45		55	ns

1. This parameter is guaranteed by design but not tested.



AC CHARACTERISTICS – WRITE CYCLE (15 TO 20NS) (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		15ns*		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	15		17		20		ns
Chip Enable to End of Write	t _{E1LWH}	t _{CW}	12		13		15		ns
	t _{E1LE1H}	t _{CW}	12		13		15		ns
	t _{E2HWH}	t _{CW}	12		13		15		ns
	t _{E2HE2L}	t _{CW}	12		13		15		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
	t _{AVE1L}	t _{AS}	0		0		0		ns
	t _{AVE2H}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	12		13		15		ns
Write Pulse Width	t _{WLWH}	t _{WP}	12		13		15		ns
	t _{WLE1H}	t _{WP}	12		13		15		ns
	t _{WLE2L}	t _{WP}	12		13		15		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		ns
	t _{E1HAX}	t _{WR}	0		0		0		ns
	t _{E2LAX}	t _{WR}	0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
	t _{E1HDX}	t _{DH}	0		0		0		ns
	t _{E2LDX}	t _{DH}	0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	7	0	8	0	8	ns
Data to Write Time	t _{DVWH}	t _{DW}	7		8		10		ns
	t _{DVE1H}	t _{DW}	7		8		10		ns
	t _{DVE2L}	t _{DW}	7		8		10		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	3		3		3		ns

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE (25 TO 55NS) (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		25ns		35ns		45ns		55ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	25		35		45		55		ns
Chip Enable to End of Write	t _{E1LWH}	t _{CW}	20		25		35		45		ns
	t _{E1LE1H}	t _{CW}		16		20		25		40	ns
	t _{E2HWH}	t _{CW}	16		20		25		40		ns
	t _{E2HE2L}	t _{CW}		16		20		25		40	ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		0		ns
	t _{AVE1L}	t _{AS}	0		0		0		0		ns
	t _{AVE2H}	t _{AS}	0		0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	20		25		35		45		ns
	t _{AVEH}	t _{AW}	20		25		35		45		ns
Write Pulse Width	t _{WLWH}	t _{WP}	20		30		30		35		ns
	t _{WLE1H}	t _{WP}	20		30		30		35		ns
	t _{WLE2L}	t _{WP}	20		30		30		35		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		5		5		ns
	t _{E1HAX}	t _{WR}	0		0		5		5		ns
	t _{E2LAX}	t _{WR}	0		0		5		5		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		ns
	t _{E1HDX}	t _{DH}	0		0		0		0		ns
	t _{E2LDX}	t _{DH}	0		0		0		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	10	0	13	0	15	0	20	ns
Data to Write Time	t _{DVWH}	t _{DW}	15		20		20		25		ns
	t _{DVE1H}	t _{DW}	15		20		20		25		ns
	t _{DVE2L}	t _{DW}	15		20		20		25		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.



FIG. 2 TIMING WAVEFORM - READ CYCLES

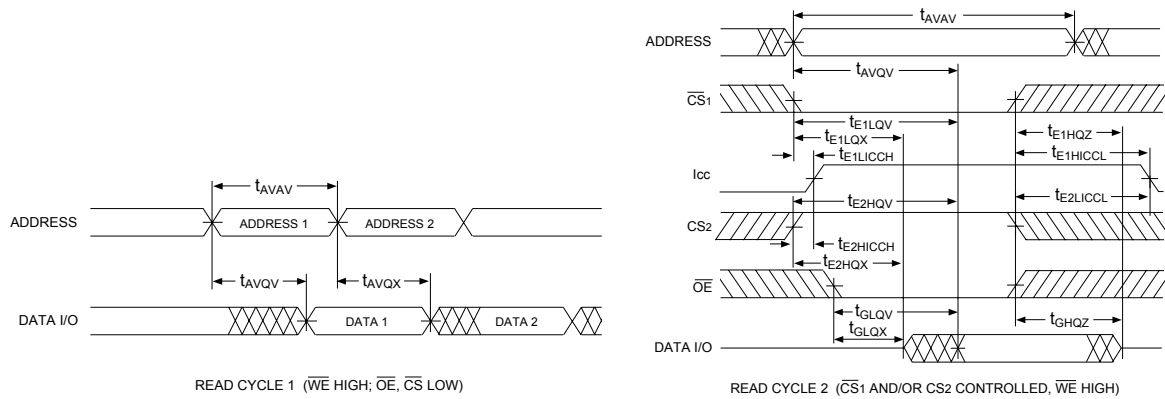


FIG. 3 WRITE CYCLE 1

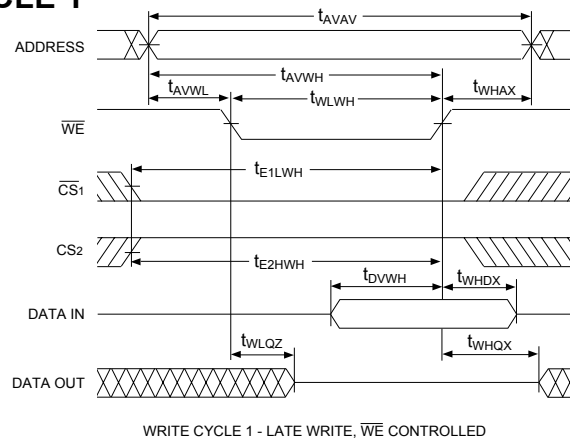
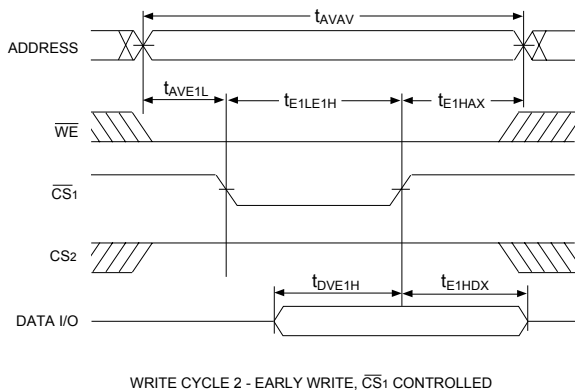
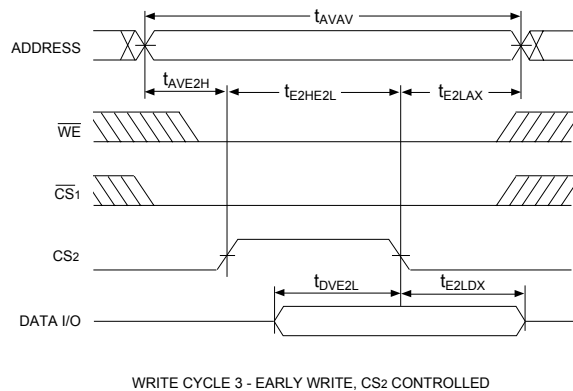


FIG. 4 WRITE CYCLES 2



WRITE CYCLES 3



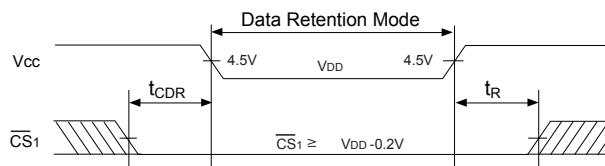
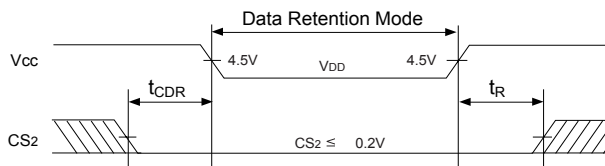
**DATA RETENTION CHARACTERISTICS (EDI88130LPS ONLY)**
($T_A = -55^{\circ}\text{C}$ TO $+125^{\circ}\text{C}$)

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Low Power Version only						
Data Retention Voltage	V_{DD}	$V_{DD} = 2.0\text{V}$	2	–	–	V
Data Retention Quiescent Current	I_{CCDR}	$\overline{CS}_1 \geq V_{DD} - 0.2\text{V}$ and/or $CS_2 \geq V_{SS} + 0.2\text{V}$	–	0.5	2	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	$V_{IN} \geq V_{DD} - 0.2\text{V}$	0	–	–	ns
Operation Recovery Time (1)	T_R	or $V_{IN} \leq 0.2\text{V}$	T_{AVAV}^*	–	–	ns

NOTE:

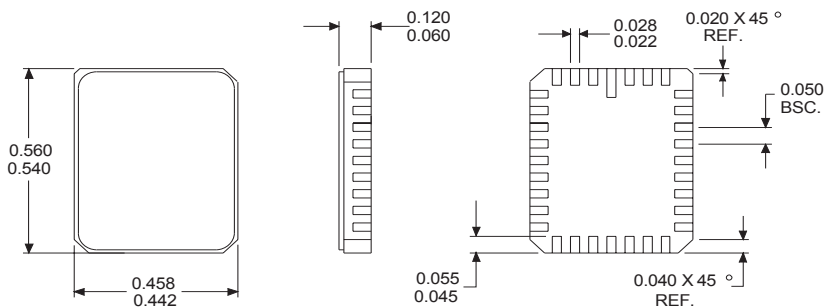
1. Parameter guaranteed by design, but not tested.

* Read Cycle Time

FIG. 5 DATA RETENTION - $\overline{CS}_1$ CONTROLLEDDATA RETENTION, $\overline{CS}_1$ CONTROLLED**FIG. 6 DATA RETENTION - CS_2 CONTROLLED**DATA RETENTION, CS_2 CONTROLLED

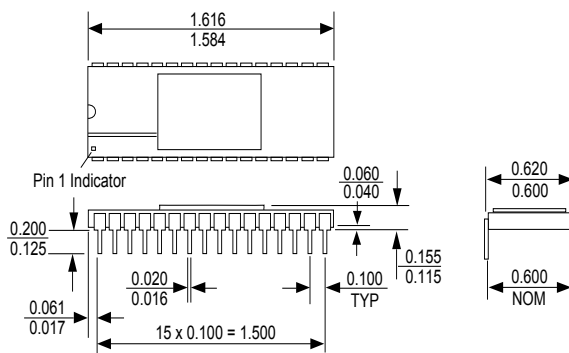


PACKAGE 12: 32 PIN CERAMIC QUAD LCC



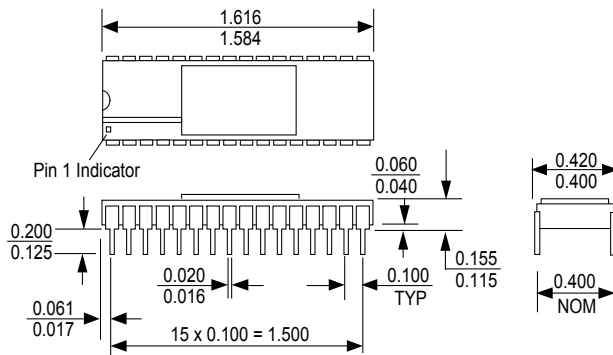
ALL DIMENSIONS ARE IN INCHES

PACKAGE 9: 32 PIN SIDEBRAZED CERAMIC DIP (600 MILS WIDE)



ALL DIMENSIONS ARE IN INCHES

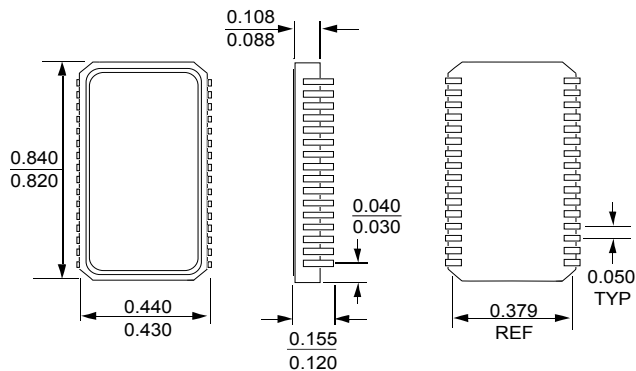
PACKAGE 102: 32 PIN SIDEBRAZED CERAMIC DIP (400 MILS WIDE)



ALL DIMENSIONS ARE IN INCHES

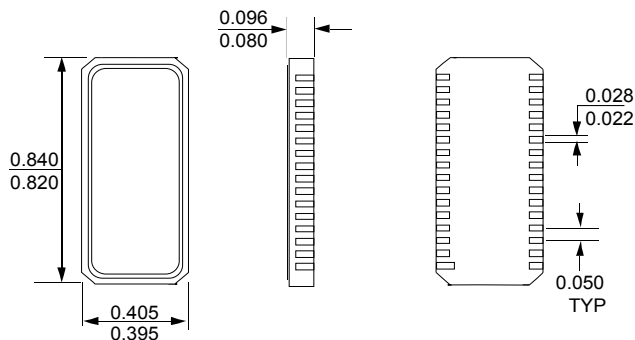


PACKAGE 140: 32 LEAD CERAMIC SOJ



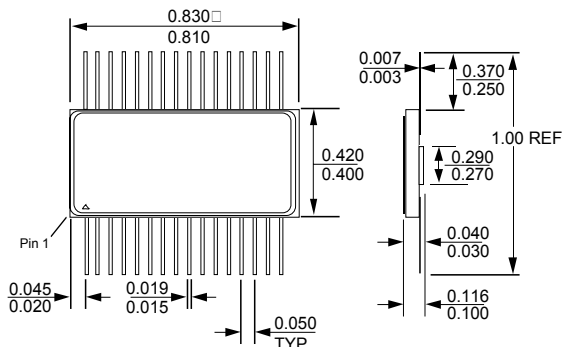
ALL DIMENSIONS ARE IN INCHES

PACKAGE 141: 32 PAD CERAMIC LCC



ALL DIMENSIONS ARE IN INCHES

PACKAGE 142: 32 PIN CERAMIC FLATPACK



ALL DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 8 130 CS X X X

WHITE ELECTRONIC DESIGNS

SRAM

ORGANIZATION, 128Kx8

(130 = Dual CS)

TECHNOLOGY:

CS = CMOS Standard Power (5V)

LPS = Low Power

ACCESS TIME (ns)

PACKAGE TYPE:

C = 32 lead Sidebrazed DIP, 600 mil (Package 9)

F = 32 lead Ceramic Flatpack (Package 142)

L = 32 pad Ceramic LCC (Package 141)

L32 = 32 pad Ceramic Quad LCC (Package 12)

N = 32 lead Ceramic SOJ (Package 140)

T = 32 lead Sidebrazed DIP, 400 mil (Package 102)

DEVICE GRADE:

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C