F75125

Serial VID, Parallel VID Translator for AMD AM2 and AM2+

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Version: 0.16P

F75125 Datasheet Revision History

Version	Date	Page	Revision History
0.10P	Jun, 2007		Preliminary version
0.11P	Jul, 2007	17	Add register description
		22	Company address
0.12P	Jul, 2007	8	Add Electrical Characteristics
0.13P	Sep, 2007	1	Correct over voltage max a\value:2.325V
		16	Add VSI/VSO illustration
		19	Revise register description
0.14P	Oct, 2007	27	Remove “G” from ordering information
0.15P	Feb, 2008	4	Add SVI output and PSI description in General Description
			Add SVI output in Features
		5	Add PSI in Features
		6	Revise Pin Configuration
		7	Add SVI output related pin descriptions in NB related pins
		8	Set VID_OUT[2] and VID_OUT[3] to multi-function pins with SVC_OUT and SVD_OUT
		17	Add NB OFF code and power saving mode description
		25	Add VDD and VDD_NB follow mode register
		26	Add VDD0,1 and VDD_NB SVID value monitor function register
		27	Add VDD timeout set register
		32	Add Serial VID output application circuit
0.16P	Mar, 2008	25	Register 0x08 renamed to VSI/VSO 1
		26	Register 0x09 renamed to VSI/VSO 2
		27	Add register 0x10 description
		27	Add register 0x11 description
		28	Add register 0x12 description

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Table of Contents

1 General Description

The Serial VID interface (SVI)/ Parallel VID interface (PVI) translator,F75125, which can translate PVI to PVI and SVI to PVI for AMD AM2 or AM2+ platform and output a programmable reference voltage of North Bridge voltage (V_{NB}) to an external single phase PWM by decoding serial VID. Or, it can translate SVI to SVI and PVI to SVI for AMD AM2 or AM2+ platform.

In the PVI output application, the F75125 can replace the hybrid (PVI+SVI) or SVI voltage regulator by the original PVI voltage regulator controller to save the extra cost. The F75125 supports VDDIO, VDDA, and CPU power good input, CPU_PG_IN, such as from the south bridge, SB600, to control the signal, VR_EN to enable the VR controller. F75125 supports all AM2+ new features including CORE_TYPE and VFIXEN. The CORE_TYPE is used to indicate AM2 or AM2+ placed, and the VFIXEN paired with SVC and SVD let voltage regulator output a fixed voltage. In this application of the F75125, VID[5] is recommended to pull low ,so the VID output [4:0] is corresponding to output from 0.775 to 1.550V. In concern of mapping SVI to PVI, VID table on-the-fly tuning is constrained in 0.800V to 1.550V. The Voltage Sense Input (VSI)/Voltage Sense Output (VSO) also provide the similar function, but the tuning range up to 2.325V.

In the SVI output application, the F75125 will issue SVI OFF code to VDD_NB to avoid VDD_NB mis-action when AM2 is implemented. In SVI output mode, the F75125 also supports PSI (bit7 of SVI command).

The F75125 is SSOP-28 package and powered by 3.3VSB.

2 Feature

- Serial VID Input to Parallel VID Output or Parallel VID Input to Parallel VID Output Translation for Parallel VID Interface Voltage Regulator Controller
- Serial VID Input to Serial VID Output or Parallel VID Input to Serial VID Output Translation for Hybrid/Serial VID Interface Voltage Regulator Controller
- Serial or Parallel VID Mapping Table Is Adjustable to Tune Voltage Regulator Controller Output.
- Programmable Reference Voltage Output for North Bridge Voltage for Over or Under Voltage in PVI Output Mode
- VFIXEN, SVC, SCD Translation to PVI Voltage Regulator Realizes AM2+ Fixed Voltage Output to CPU Function
- Support CORE_TYPE Input to Indicate AMD Processor Family 0Fh,AM2 or 10h,AM2+
- Support VDDIO, VDDA, CPU Power Good, CPU_PG_IN, Input to Generate Voltage Regulator Controller Enable Signal, VR_EN, and CPU Power Good Output, CPU_PG_OUT, to CPU and Voltage Regulator.

- 2 Sets of Voltage Sense Input (VSI) and Voltage Sense Output (VSO) for Over Voltage Vcore and V_{NB} beyond Maximum of VID Table, 1.55V.
- I2C Interface Is Built-in to Fine Tune Vcore and V_{NB} output.
- Power Saving Mode Supported in Both AM2+ Platform
- Powered by 3.3VSB and SSOP-28 Package

3 Pin Configuration

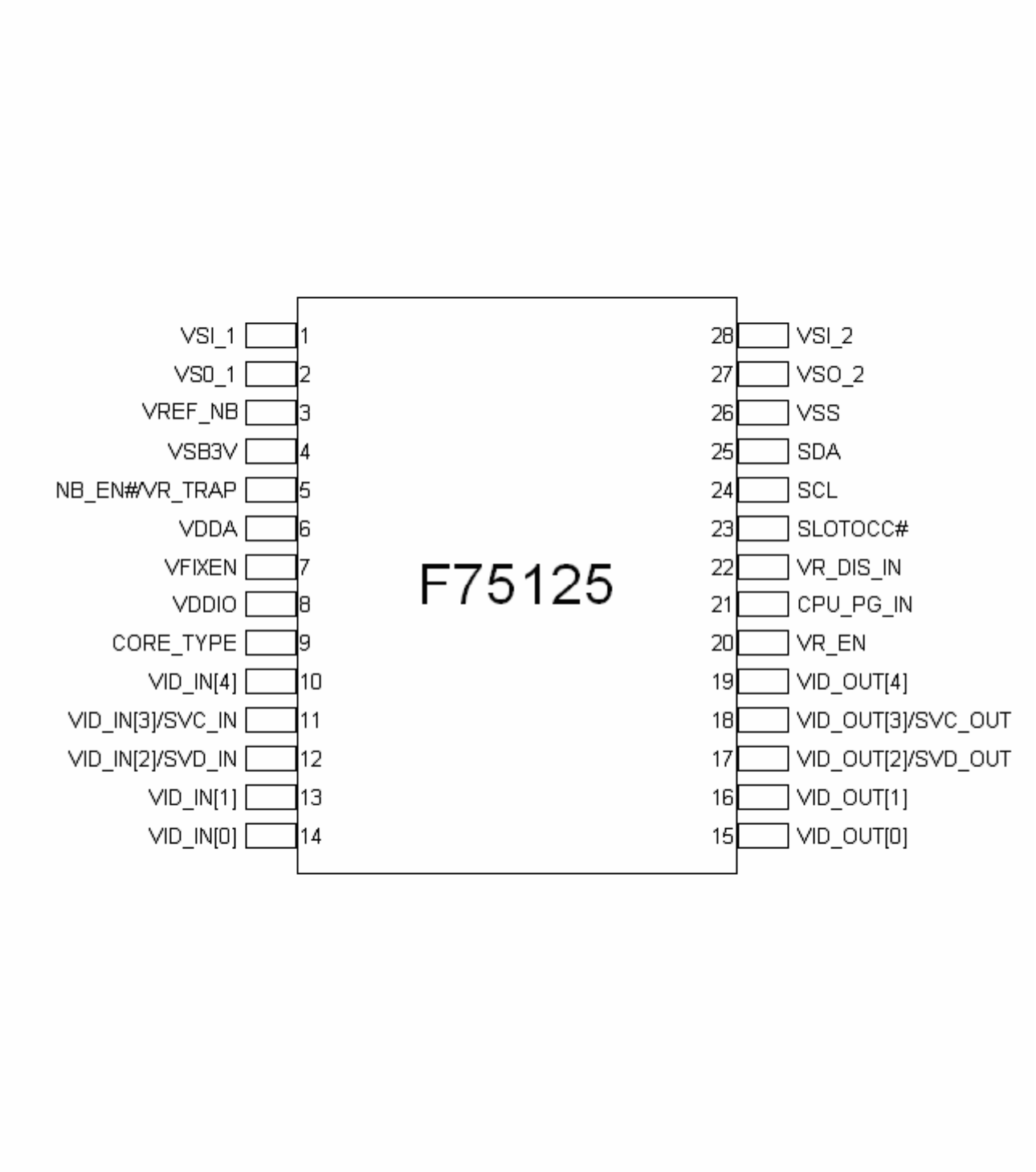


Figure1. F75125 pin configuration

4 Pin Description

P - Power pins

IN_{st} - TTL level input pin with schmitt trigger

IN_{LV} - Low level input, transient point at 0.9V

I/OD_{12st5V} - TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability, 5V tolerance

I/OD_{12st} - TTL level bi-directional pin with schmitt trigger, Open-drain output with 12 mA sink capability.

I/OD_{12LV} - Low level input, transient point at 0.9V , Open-drain output with 12 mA sink capability

O_{12} - Output pin with 12mA sink/driving capability.

OD_{12} - Open-Drain output pin with 12mA sink capability.

AIN - Input pin (Analog).

AOUT - Output pin (Analog).

4.1. Power Pin

Pin No.	Pin Name	Type	Description
4	VSB3V	P	3.3V stand by power
6	VDDA	P	VDDA input
8	VDDIO	P	VDDIO power
26	VSS	P	Ground

4.2. North Bridge Voltage Pin/ Voltage Regulator Set Trap Pin

Pin No.	Pin Name	Type	PWR	Description
3	VREF_NB	AOUT	VSB3V	In PVI output mode, reference voltage output to external single phase PWM to supply V_{NB}.
5	NB_EN#/VR_TRAP	O_{12}	VSB3V	Pull high to 3,3VSB before POK, the F75125 will enter SVI output mode, or the F75125 is set to PVI output mode. In PVI output mode, NB_EN# is an external single phase PWM enable signal.

4.3. VID Pin

Pin No.	Pin Name	Type	PWR	Description
10	VID_IN[4]	IN_{LV}	VSB3V	CPU VID input pin. Special level input VIH→ 0.9, VIL → 0.6
11	VID_IN[3]	IN_{LV}	VSB3V	CPU VID input pin. Special level input VIH→ 0.9, VIL → 0.6
	SVC_IN			SVC (Serial VID Clock)-open drain output of the processor. Connect to this pin to the processor.
12	VID_IN[2]	I/OD_{12LV}	VSB3V	CPU VID input pin. Special level input VIH→ 0.9, VIL → 0.6
	SVD_IN			SVD (Serial VID Data)-bidirectional signal that is an input and open drain output for both master and slave devices. Connect to this pin to the processor.
13	VID_IN[1]	IN_{LV}	VSB3V	CPU VID input pin. Special level input VIH→ 0.9, VIL → 0.6
14	VID_IN[0]	IN_{LV}	VSB3V	CPU VID input pin. Special level input VIH→ 0.9, VIL → 0.6
15	VID_OUT[0]	OD_{12}	VSB3V	CPU VID output pin. Special level input VIH→ 0.9, VIL → 0.6
16	VID_OUT[1]	OD_{12}	VSB3V	CPU VID output pin. Special level input VIH→ 0.9, VIL → 0.6
17	VID_OUT[2]	OD_{12}	VSB3V	CPU VID output pin. Special level input VIH→ 0.9, VIL → 0.6
	SVC_OUT			SVC(Serial VID Clock)-open drain output of the F75125. Connect to this pin to the voltage regulator.
18	VID_OUT[3]	I/OD_{12}	VSB3V	CPU VID output pin. Special level input VIH→ 0.9, VIL → 0.6
	SVD_OUT			SVD (Serial VID Data)-bidirectional signal that is an input and open drain output for both master and slave devices. Connect to this pin to the voltage regulator.
19	VID_OUT[4]	OD_{12}	VSB3V	CPU VID output pin. Special level input VIH→ 0.9, VIL → 0.6

4.4. Power Good Pin

Pin No.	Pin Name	Type	PWR	Description
21	VR_DIS_IN	IN_{LV}	VSB3V	VR disable signal input. The source is NOR S3# and VLDT. VR_DIS_IN < 0.6V, VR_EN goes high. VR_DIS_IN > 0.9V, VR_REN goes low.

22	CPU_PG_IN	IN_{st}	VSB3V	CPU power good signal input, usually from the south bridge

4.5. Voltage Sense Input/Voltage Sense Output Pin

Pin No.	Pin Name	Type	PWR	Description
1	VSI_1	AIN	VSB3V	Voltage sensor channel 1 input for Vcore or V_{NB} change use.
2	VSO_1	AOUT	VSB3V	Voltage sensor channel 1 output for Vcore or V_{NB} change use.
27	VSO_2	AOUT	VSB3V	Voltage sensor channel 2 output for Vcore or V_{NB} change use.
28	VSO_1	AIN	VSB3V	Voltage sensor channel 2 input for Vcore or V_{NB} change use.

4.6. I2C Interface Pin

Pin No.	Pin Name	Type	PWR	Description
24	SCL	IN_{st}	VSB3V	I2C interface, serial clock input pin.
25	SDA	I/OD_{12st}	VSB3V	I2C interface, serial data pin.

4.7. Miscellaneous Pin

Pin No.	Pin Name	Type	PWR	Description
7	VFIXEN	IN_{LV}	VSB3V	Hardware jumper input that selects normal operation mode or VFIX mode. When VFIXEN inserts, the voltage regulator will enter VFIX mode.
9	CORE_TYPE	IN_{LV}	VSB3V	Processor CORE_TYPE input. In AMD NPT Family 0Fh, CORE_TYPE is floating In AMD NPT Family 10h, CORE_TYPE is tied to VSS at package.
20	VR_EN	OD_{12}	VSB3V	Active-high signal enables the VID VR
23	SLOTOCC#	IN_{st}	VSB3V	CPU SLOTOCC# input.

5 Electrical Characteristic

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 5.5	V
Input Voltage	-0.5 to VDD+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

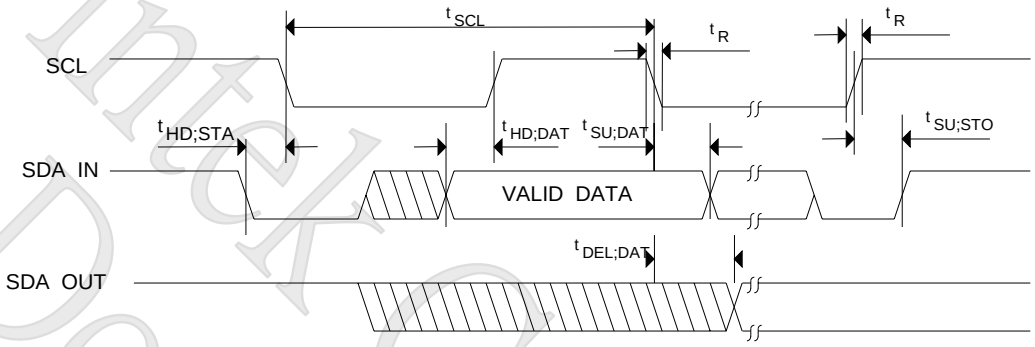
5.2 DC Characteristics

(Ta = 0° C to 70° C, VCC = 3.3V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OD_{12}- Open-drain output with12 mA sink capability.						
Output Low Current	IOL		+12		mA	VOL = 0.4V
Input High Leakage	ILIH			+1	µA	VIN = VCC
Input Low Leakage	ILIL	-1			µA	VIN = 0V
I/OD_{12st}-TTL level bi-directional pin with schmitt trigger, Output pin with 12mA sink capability.						
Input Low Threshold Voltage	Vt-			0.8	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	2.0			V	VCC = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Input High Leakage	ILIH			+1	µA	VIN = VCC
Input Low Leakage	ILIL	-1			µA	VIN = 0V
I/OD_{12lv}-Low voltage bi-directional pin, Open drain output pin with 12mA sink capability.						
Input Low Threshold Voltage	Vt-			0.6	V	VCC = 3.3 V
Input High Threshold Voltage	Vt+	0.9			V	VCC = 3.3 V
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	µA	VIN = 1.2V
Input Low Leakage	ILIL	-1			µA	VIN = 0V
IN_{lv} - Low level input pin						
Input Low Voltage	VIL			0.6	V	
Input High Voltage	VIH	0.9			V	
Input High Leakage	ILIH			+1	µA	VIN = 1.2V

Input Low Leakage	ILIL	-1			μA	VIN = 0 V
O_{12}- Output pin with 12mA source-sink capability.						
Output Low Current	IOL		-12	-9	mA	VOL = 0.4 V
Output High Current	IOH	+9	+12		mA	VOH = 2.4V
Input High Leakage	ILIH			+1	μA	VIN = VCC
Input Low Leakage	ILIL	-1			μA	VIN = 0V

5.3 AC Characteristics

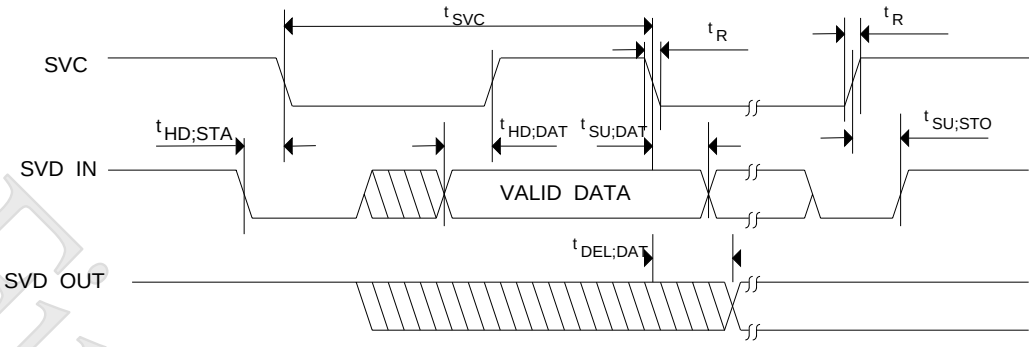


Serial Bus Timing Diagram

Figure2. SMBus timing diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock period	t_{SCL}	3		uS
Start condition hold time	$t_{HD;SDA}$	50		nS
Stop condition setup-up time	$t_{SU;STO}$	50		nS
DATA to SCL setup time	$t_{SU;DAT}$	50		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
DATA OUT to SCL delay time	$t_{DEL:DATA}$	200		ns
SCL and SDA rise time	t_R		200	nS
SCL and SDA fall time	t_F		200	nS



Serial Bus Timing Diagram

Figure3. Serial VID timing diagram

Serial VID interface Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	2		uS
Start condition hold time	$t_{HD;SDA}$	50		nS
Stop condition setup-up time	$t_{SU;STO}$	50		nS
DATA to SCL setup time	$t_{SU;DAT}$	50		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
DATA OUT to SCL delay time	$t_{DEL:DATA}$	200		ns
SCL and SDA rise time	t_R		200	nS
SCL and SDA fall time	t_F		200	nS

6 Functional Description

6.1 Linear Con Parallel VID Interface

The F75125 supports 6-bit Parallel VID Interface (PVI). The 6-bit parallel VID codes and the corresponding reference voltage are shown in Table 1. It is recommended to connect VID[0:4] output of AM2 or AM2+ and VID[0:4] input of voltage regulator (VR) controller with F75125 due to the pin-out constraint and tied VID[5] input of the VR controller to VSS. The connection can correspond to reference voltage from 1.55V to 0.775V. The corresponding reference voltage is from 0.800V to 1.550V in concerns of the translation between Serial VID Interface (SVI) and PVI. The VID output is adjustable according to the Parallel VID table on-the-fly or by VSI/VSO function through I2C interface.

Table 1. 6-bit Parallel VID Codes

VID5	VID4	VID3	VID2	VID1	VID0	VREF
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500

0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625

1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

6.2 Serial VID Interface

The Serial VID Interface (SVI) circuitry allows AM2+ to directly drive the core voltage and Northbridge voltage reference level with the SVI VR controller. The SVC and SVD states are decoded with direction from the PWROK and VFIXEN inputs as described in the following sections. The F75125 is built-in SVI client to translate SVI to PVI. It can help the PVI VR controller keep supporting AM2+ in SVI mode to reduce extra cost to adapt the hybrid VR controller (SVI+PVI) or the SVI VR controller. The VID codes output translated form SVI is also adjustable from 0.800V to 1.550V according to the VID table on-the-fly by I2C interface. If the output is beyond the VID table, it can be tuned by VSI/VSO function, too.

Table 2. Serial VID Codes

SVID[6:0]	VREF	SVID[6:0]	VREF	SVID[6:0]	VREF		SVID[6:0]	VREF	
000_0000	1.5500	010_0000	1.1500	100_0000	0.7500		110_0000	0.3500	*
000_0001	1.5375	010_0001	1.1375	100_0001	0.7375		110_0001	0.3375	*
000_0010	1.5250	010_0010	1.1250	100_0010	0.7250		110_0010	0.3250	*
000_0011	1.5125	010_0011	1.1125	100_0011	0.7125		110_0011	0.3125	*
000_0100	1.5000	010_0100	1.1000	100_0100	0.7000		110_0100	0.3000	*
000_0101	1.4875	010_0101	1.0875	100_0101	0.6875		110_0101	0.2875	*
000_0110	1.4750	010_0110	1.0750	100_0110	0.6750		110_0110	0.2750	*
000_0111	1.4625	010_0111	1.0625	100_0111	0.6625		110_0111	0.2625	*
000_1000	1.4500	010_1000	1.0500	100_1000	0.6500		110_1000	0.2500	*
000_1001	1.4375	010_1001	1.0375	100_1001	0.6375		110_1001	0.2375	*
000_1010	1.4250	010_1010	1.0250	100_1010	0.6250		110_1010	0.2250	*
000_1011	1.4125	010_1011	1.0125	100_1011	0.6125		110_1011	0.2125	*
000_1100	1.4000	010_1100	1.0000	100_1100	0.6000		110_1100	0.2000	*
000_1101	1.3875	010_1101	0.9875	100_1101	0.5875		110_1101	0.1875	*
000_1110	1.3750	010_1110	0.9750	100_1110	0.5750		110_1110	0.1750	*
000_1111	1.3625	010_1111	0.9625	100_1111	0.5625		110_1111	0.1625	*
001_0000	1.3500	011_0000	0.9500	101_0000	0.5500		111_0000	0.1500	*
001_0001	1.3375	011_0001	0.9375	101_0001	0.5375		111_0001	0.1375	*
001_0010	1.3250	011_0010	0.9250	101_0010	0.5250		111_0010	0.1250	*
001_0011	1.3125	011_0011	0.9125	101_0011	0.5125		111_0011	0.1125	*
001_0100	1.3000	011_0100	0.9000	101_0100	0.5000		111_0100	0.1000	*
001_0101	1.2875	011_0101	0.8875	101_0101	0.4875	*	111_0101	0.0875	*
001_0110	1.2750	011_0110	0.8750	101_0110	0.4750	*	111_0110	0.0750	*
001_0111	1.2625	011_0111	0.8625	101_0111	0.4625	*	111_0111	0.0625	*
001_1000	1.2500	011_1000	0.8500	101_1000	0.4500	*	111_1000	0.0500	*
001_1001	1.2375	011_1001	0.8375	101_1001	0.4375	*	111_1001	0.0375	*
001_1010	1.2250	011_1010	0.8250	101_1010	0.4250	*	111_1010	0.0250	*
001_1011	1.2125	011_1011	0.8125	101_1011	0.4125	*	111_1011	0.0125	*
001_1100	1.2000	011_1100	0.8000	101_1100	0.4000	*	111_1100	OFF	
001_1101	1.1875	011_1101	0.7875	101_1101	0.3875	*	111_1101	OFF	
001_1110	1.1750	011_1110	0.7750	101_1110	0.3750	*	111_1110	OFF	
001_1111	1.1625	011_1111	0.7625	101_1111	0.3625	*	111_1111	OFF	

Note: * Indicates a VID not required for AMD Family 10h processors (AM2+).

6.3 2-Bit Boot Code and VFIXEN Mode

VFIXEN is an input signal used to indicate the VR controller in the VFIX mode. If anytime VFIXEN is asserted, the VR controller must enter VFIX mode. When in VFIX mode, all of the VR controller's output voltage will be governed by the information shown in Table 4. However, the PVI VR controller doesn't integrate the VFIXEN input pin, the F75125 can translate the VFIXEN, SVC, and SVD to PVI codes to indicate the PVI VR controller in the VFIX mode.

Pre-PWROK METAL VID, 2-Bit Boot Code

Typical motherboard start-up occurs with the VFIXEN input low. The F75125 decodes the SVC and SVD inputs to determine the Pre-PWROK metal VID setting. After PWROK is asserted, the processor initializes the SVI, and the serial VID codes are used.

Table 3. Pre-PWROK Metal VID Codes

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIX MODE

In VFIX mode, the SVC, SVD, and VFIXEN inputs are fixed external to controller through jumpers to either GND or VDDIO. If VFIXEN is high, the F75125 decodes the SVC and SVD states per Table 4 regardless of the state of PWROK. Once enable, the VR controller and the external single phase PWM begin to soft-start both VDD and VDDNB planes.

Table 4. VFIX Mode VID Codes

SVC	SVD	Output Voltage (V)
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

6.4 North Bridge Reference Voltage and Enable

The PVI VR controller which is designed for AM2 or prior processor doesn't integrate the second precision voltage regulation system for the North Bridge portion of AM2+. In order to forward compatible to AM2+, the F75125

provides the North Bridge reference voltage output, NB_VREF, and North Bridge voltage enable signal, NB_EN#, to the external single phase PWM which provides the North Bridge voltage. The F75125 successfully decodes the information North Bridge voltage determines as the processor in the SVI mode, and then the NB_VREF is in the soft-start process. The NB_EN# will be asserted high to low when the NB_VREF is over 0.3V. Both NB_VREF and NB_EN# will be disabled as the processor in PVI mode. The NB_VREF output is adjustable from 0.3V to 2.04V by I2C interface. Per Step is 12.5mV.

Another application of the F75125 is to support SVI output. Pull high NB_EN# to 3,3VSB before POK, and then the F75125 will switch the output mode to SVI output. In SVI output mode, the F75125 will translate PVID to the corresponding SVID and issue VDD_NB an OFF command (111_1111 in SVID table) to disable VDD_NB output of voltage regulator as AM2 implemented*1.

Note:

*1 The chosen voltage regulator must support SVID OFF command, or VDD_NB keeps outputting as AMD implemented.

6.5 Power Saving Mode

The power saving mode is supported in SVI mode. Serial VID codes are transmitted as part of an 8-bit data phase over the SVI. The bits are allocated as defined in Table 5.

Table 5. Serial VID 8-Bit Data Field Encoding

Bits	Description
7	PSI_L: =0, means the processor is at an optimal load for the regulator(s) to enter power saving mode =1, means the processor is not at an optimal load for the regulator(s) to enter power saving mode
6:0	SVID[6:0] as defined in Table 2.

In AM2+ platform, the truth table of PSI# and SVID_IN[7] is defined in Table 6.

Table 6. SVID_IN[7], SVID_OUT[7] Relationship

SVID_IN[7]*1	SVID_OUT[7]*2	Remark
0	0	AM2+ is at a light load condition for the regulator(s) to enter power saving mode
1	1	AM2+ is not at a light load condition for the regulator(s) to enter power saving mode

Note:

*1 SVID_IN[7] is output by the processor to the F75125

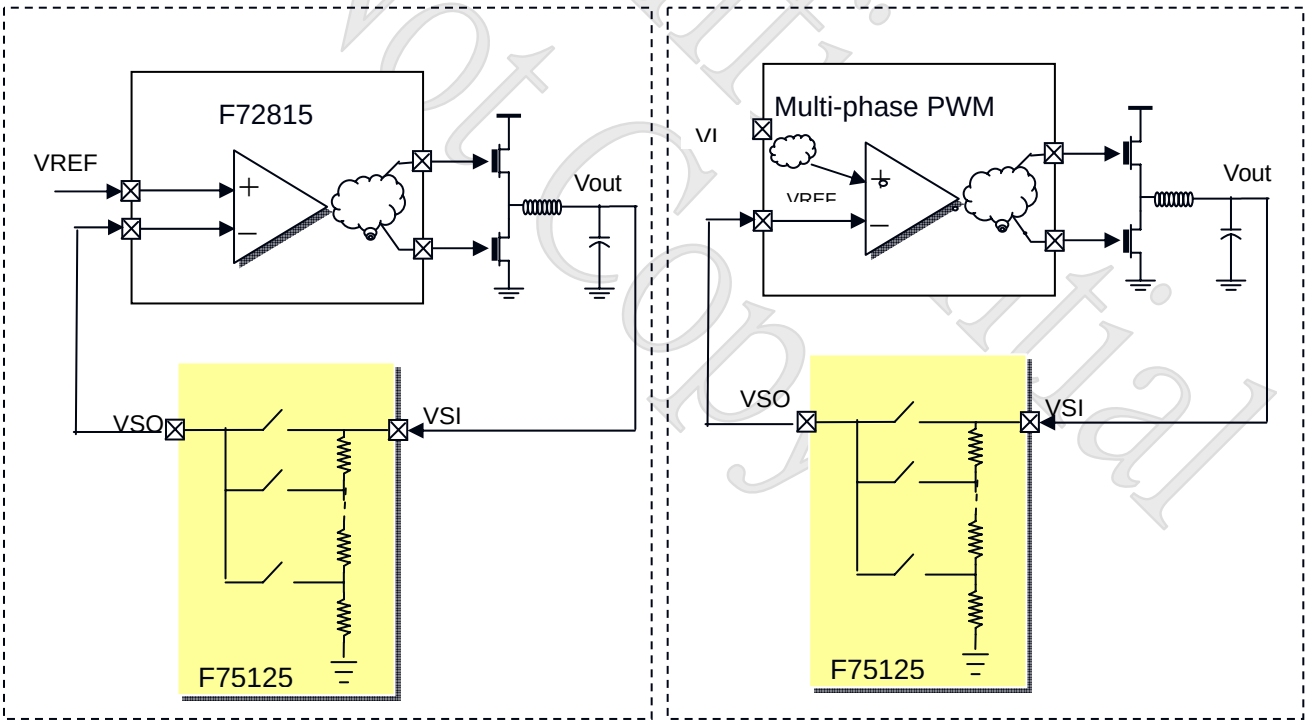
*2 SVID_OUT[7] is output by the F75125 to the Vcore voltage regulator

6.6 CORE_TYPE

The CORE_TYPE is used to indicate which kind of processor placed and which kind of VID codes should be issued by the processor. According to AMD's reference circuit, the VID[1] is recommended tied with CORE_TYPE. In AM2, CORE_TYPE is floating, and VID[1] is driven to VDDIO by the processor. The processor will issue the parallel VID codes. In AM2+, CORE_TYPE is tied to VSS at the package, and VID[1] is driven low via strap to ground. The processor will issue the serial VID codes. CORE_TYPE is also connected to the F75125 to indicate which kind of VID codes will be decoded.

6.7 Voltage Sense Input/ Voltage Sense Output

The Voltage Sense Input (VSI) and Voltage Sense Output (VSO) are designed for another option of over voltage, especially beyond the VID table, 1.55V. Every step of over voltage is 1.5% more of the current voltage. Total tuning steps are 32 steps, so the maximum tuning range up is to 2.325V.



Vout=VREF*(1+n*0.01613) n=0.1.2……31

Figure 4 VSI/VSO function illustration

6.8 I2C Interface

The F75125 can be connected to a compatible 2-wire serial system Management Bus (SMBus) as a slave device under the control of the master device, using two device terminals SCL and SDA. The controller can provide a clock signal to the device SCL pin and read/write data from/to the device through the device SDA pin. The address default is 0x5C(0101_1100) and the operation of device to the bus is described with details in the following sections.

(a) SMBus write to internal address register followed by the data byte

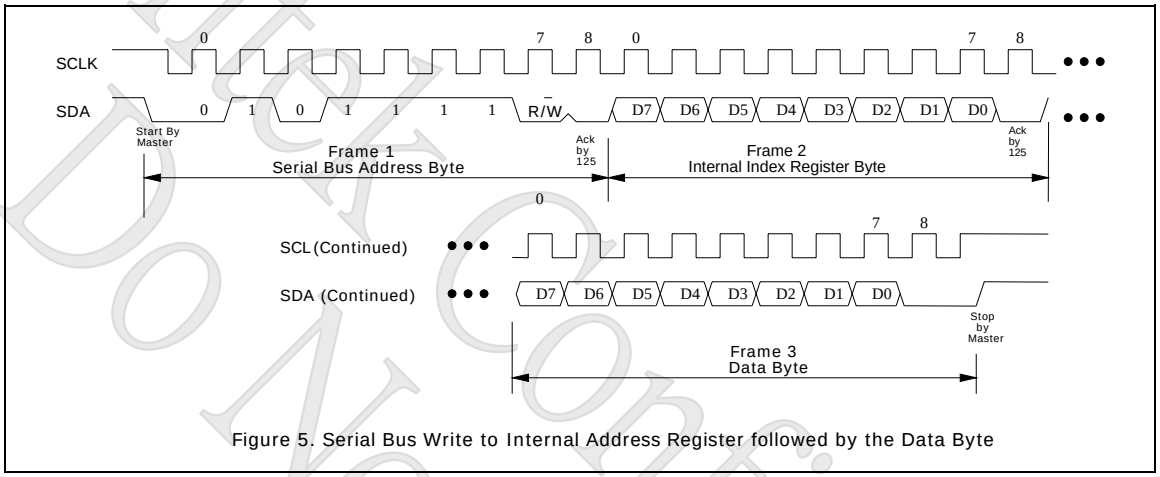


Figure 5. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

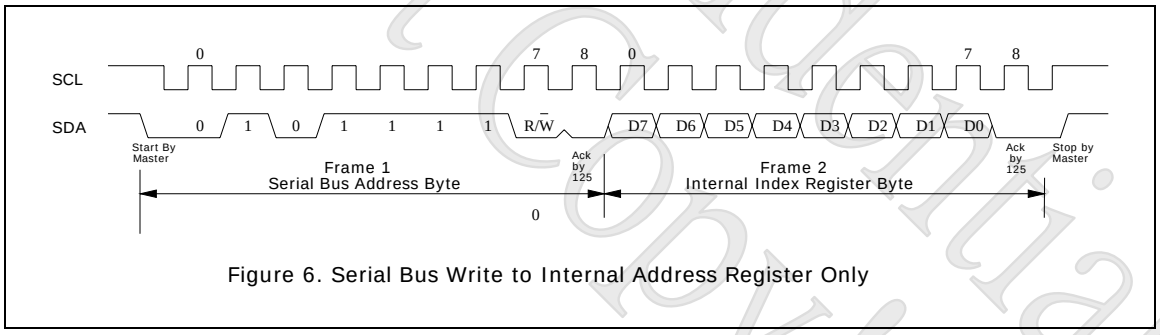


Figure 6. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

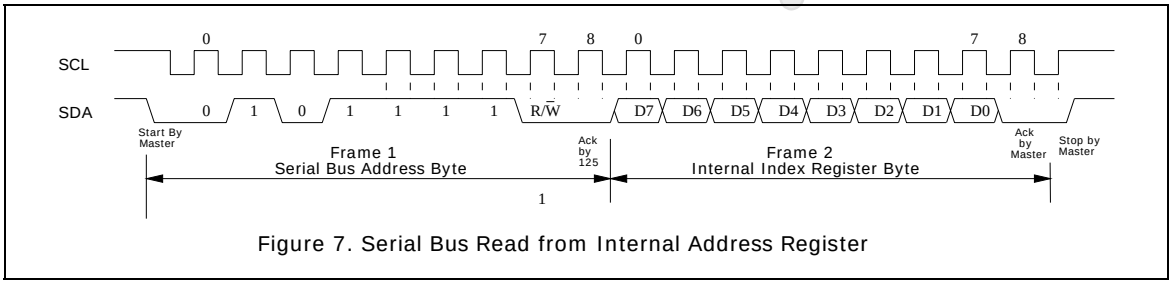


Figure 7. Serial Bus Read from Internal Address Register

7 Register Description (I2C Address = 0x5C)

7.1 VDDNB voltage value Register — Index 00h

Bit	Name	R/W	Default	Description
7-0	VDDNB	R/W	xx	VDDNB value, The default value is latch from SVC and SVD VFIXEN=1 SVC,SVD=0, The VDDNB default is 0x0C (1.4V) SVC,SVD=1, The VDDNB default is 0x1C (1.2V) SVC,SVD=2, The VDDNB default is 0x2C (1.0V) SVC,SVD=3, The VDDNB default is 0x3C (0.8V) VFIXEN=0 SVC,SVD=0, The VDDNB default is 0x24 (1.1V) SVC,SVD=1, The VDDNB default is 0x2C (1.0V) SVC,SVD=2, The VDDNB default is 0x34 (0.9V) SVC,SVD=3, The VDDNB default is 0x3C (0.8V) **Manual disable(CR0A bit0 "0")** This register can program by SVI interface by ID 8'b110x_xx10. **Manual enable(CR0A bit0 "1")** Programming by I2C interface and protect by key CR03 .

7.2 VDD0 voltage value Register — Index 01h

Bit	Name	R/W	Default	Description
7-0	VDD0	R/W	xx	VDD0 value, The default value is latch from SVC and SVD VFIXEN=1 SVC,SVD=0, The VDD0 default is 0x0C (1.4V) SVC,SVD=1, The VDD0 default is 0x1C (1.2V) SVC,SVD=2, The VDD0 default is 0x2C (1.0V) SVC,SVD=3, The VDD0 default is 0x3C (0.8V) VFIXEN=0 SVC,SVD=0, The VDD0 default is 0x24 (1.1V) SVC,SVD=1, The VDD0 default is 0x2C (1.0V) SVC,SVD=2, The VDD0 default is 0x34 (0.9V) SVC,SVD=3, The VDD0 default is 0x3C (0.8V) **Manual disable(CR0A bit0 "0")** This register can program by SVI interface by ID 8'b110x_x1x0 **Manual enable(CR0A bit0 "1")** Programming by I2C interface and protect by key CR03.

7.3 VDD1 voltage value Register — Index 02h

Bit	Name	R/W	Default	Description
7-0	VDD1	R/W	xx	VDD1 value, The default value is latch from SVC and SVD VFIXEN=1 SVC,SVD=0, The VDD0 default is 0x0C (1.4V) SVC,SVD=1, The VDD0 default is 0x1C (1.2V) SVC,SVD=2, The VDD0 default is 0x2C (1.0V) SVC,SVD=3, The VDD0 default is 0x3C (0.8V) VFIXEN=0 SVC,SVD=0, The VDD0 default is 0x24 (1.1V) SVC,SVD=1, The VDD0 default is 0x2C (1.0V) SVC,SVD=2, The VDD0 default is 0x34 (0.9V) SVC,SVD=3, The VDD0 default is 0x3C (0.8V) **Manual disable(CR0A bit0 "0")** This register can program by SVI interface by ID 8'b110x_1xx0 **Manual enable(CR0A bit0 "1")** Programming by I2C interface and protect by key CR03.

7.4 VID Key protect Register — Index 03h

Bit	Name	R/W	Default	Description
7-0	VID_KEY	R/W	0	Enter key by 0x32→0x5d→0x42→0xac When into key the reading value in this register will be 0xff. Exit key by 0x35 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.5 VDDNB voltage offset value Register — Index 04h

Bit	Name	R/W	Default	Description
7-0	NB_OFFSET	R/W	0	0x00: VDDNB voltage = VDDNB value(CR00) 0x01: VDDNB voltage = VDDNB value(CR00) + 1 voltage step(12.5mv) 0x7f: VDDNB voltage = VDDNB value(CR00) + 127 voltage step(12.5mv) but maximum value is 1.55V 0xff: VDDNB voltage = VDDNB value(CR00) - 1 voltage step(12.5mv) 0x80: VDDNB voltage = VDDNB value(CR00) - 128 voltage step(12.5mv) but minimum value is 0.0125V This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.6 VDD0 voltage offset value Register — Index 05h

Bit	Name	R/W	Default	Description
7-0	VDD0_OFFSET	R/W	0	0x00:VDD0 voltage = VDD0 value(CR01) 0x01:VDD0 voltage = VDD0 value(CR01) + 1 step(12.5mv) 0x7F:VDD0 voltage = VDD0 value(CR01) + 127 step(12.5mv) but maximum value is 1.55V 0xFF:VDD0 voltage = VDD0 value(CR01) - 1 step(12.5mv) 0x80:VDD0 voltage = VDD0 value(CR01) - 128 step(12.5mv) but minimum value is 0.0125 (in serial to parallel mode minimum value is 0.7875V) This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.7 VDD1 voltage offset value Register — Index 06h

Bit	Name	R/W	Default	Description
7-0	VDD1_OFFSET	R/W	0	0x00:VDD1 voltage = VDD1 value(CR02) 0x01:VDD1 voltage = VDD1 value(CR02) + 1 step (12.5mv) 0x7f:VDD1 voltage = VDD1 value(CR02) + 127 step (12.5mv) but maximum value is 1.55V 0xff:VDD1 voltage = VDD1 value(CR02) - 1 step(12.5mv) 0x80:VDD1 voltage = VDD1 value(CR02) - 128 step (12.5mv) but minimum value is 0.0125V This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.8 VDDNB STEP TIME Register — Index 07h

Bit	Name	R/W	Default	Description
7-4	Reserved	R	0	
3_0	STEP_TIME_SEL	R/W	2	0: Direct load expect voltage (CR00+CR04) to NB_VREF pin 1: NB_VREF change voltage by step(8mV), each step is 100us 2: NB_VREF change voltage by step(8mV), each step is 200us But in power on NB_VREF soft start the rise time is 8mv per 100us This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.9 VSI/VSO 1 Over Voltage select Reading Register — Index 08h

Bit	Name	R/W	Default	Description
7-5	Reserved	R	0	
4-0	SWITCH_SEL_1	R/W	0	Vout = VREF *(1 + (SWITCH_SEL_0*0.01613)) Please refer Figure 4,P16 This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.10 VSI/VSO 2 Over Voltage select Reading Register — Index 09h

Bit	Name	R/W	Default	Description
7-5	Reserved	R	0	
4-0	SWITCH_SEL_2	R/W	0	Vout = VREF *(1 + (SWITCH_SEL_0*0.01613)) Please refer Figure 4,P16 This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.11 VDD0, VDD1 and VDDNB manual enable Register — Index 0Ah

Bit	Name	R/W	Default	Description
7-6	Reserved	R	0	Reserved,
5	VDD0_MIRROR_EN	R/W	0	In serial VID output mode, if this bit is set to 1, VDD0 will follow VID value of VDDNB.
4	NB_MIRROR_EN	R/W	0	In serial VID output mode, if this bit is set to 1, VDDNB will follow VID value of VDD0.
3-1	Reserved	R	0	Reserved,
0	MANUAL_EN	R/W	0	00: Manual mode is disabled. 01: Serial to parallel manual mode is enabled, but parallel to parallel keep in bypass mode. 10: Reserved. 11: Serial to parallel and parallel to parallel manual mode enabled. When F75125 manual mode enable, user can program CR00 , CR01 and CR02 by i2c interface, and CR00 value will direct to control NB_VREF voltage (each step is 12.5mv) CR01 value + CR05 offset value will output to VID out. This register is write protect by Enter key CR03 It can be reset by watchdog timeout. If CR0F[0] is set to 1, it can be reset by SLOTOCC# pin, too (Default is disabled).

7.12 NB_VREF Voltage Reading Register (LSB) — Index 0Bh

Bit	Name	R/W	Default	Description
7-0	NB_VID_OUT	R	0	{1'b0,VID_OUT_NB} * 8mv

7.13 VDDNB SVI Output Reading Register (LSB) — Index 0Ch

Bit	Name	R/W	Default	Description
7-0	NB _OUT	R	0	SVID_OUT_NB (CR00+CR04)

7.14 VDD0 SVI Output Reading Register (LSB) — Index 0Dh

Bit	Name	R/W	Default	Description
7-0	VDD0_OUT	R	0	SVID_OUT_VDD0 (CR01+CR05)

7.15 VDD1 SVI Output Reading Register (LSB) — Index 0Eh

Bit	Name	R/W	Default	Description
7-0	VDD1_OUT	R	0	SVID_OUT_VDD1(CR02+CR06)

7.16 SLOTOCC Control Enable Reading Register — Index 0Fh

Bit	Name	R/W	Default	Description
7	Reserved	R	1	Reserved
6-1	DUMMY_REG	R/W	0	Dummy registers.
0	SLOTOCC_CLR_EN	R/W	0	Enable SLOTOCC# pin to clear register

7.17 VDD_NB Voltage Value Register — Index 10h

Bit	Name	R/W	Default	Description
7-0	VDDNB	R	xx	This register can read VID value that input from SVI interface. This register presents all the SVID code including bit 7, PSI_L.

7.18 VDD0 Voltage Value Register — Index 11h

Bit	Name	R/W	Default	Description
7-0	VDD0	R	xx	This register can read VID value that input from PVI/SVI interface. In PVI input mode, MSB and LSB will be inserted “0” to complement 8 bit register. For example, PVID code “111_111” will be read as 0x7E. In SVI mode, this register presents all the SVID code including bit 7, PSI_L.

7.19 VDD1 Voltage Value Register — Index 12h

Bit	Name	R/W	Default	Description
7-0	VDD1	R	xx	This register can read VID value that input from SVI interface. This register presents all the SVID code including bit 7, PSI_L.

7.20 VID Timeout Value Select Register — Index 13h

Bit	Name	R/W	Default	Description
7	TIMER_EN	R/W	0	Set to 1 to enable VID watchdog timer..
6-0	COUNT_VALUE	R/W	7'h0	When TIMER_EN is set to 1 and counter value down count to zero, it will generate one reset pulse to clear internal registers and TIMER_EN bit will auto clear to 0.

7.21 CHIP ID1 Register — Index 5Ah

Bit	Name	R/W	Default	Description
7-0	CHIP_ID1	R	07h	Chip ID1

7.22 CHIP ID2 Register — Index 5Bh

Bit	Name	R/W	Default	Description
7-6	CHIP_ID2	R	03h	Chip ID2

7.23 Version ID Register — Index 5Ch

Bit	Name	R/W	Default	Description
7-0	VER_ID	R	30h	Version ID

7.24 Vendor ID1 Register — Index 5Dh

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID1	R	19h	Vendor ID1

7.25 Vendor ID2 Register — Index 5Eh

Bit	Name	R/W	Default	Description
7-0	VENDOR_ID2	R	34h	Vendor ID2

8 Ordering Information

Part Number	Package Type	Production Flow
F75125R	28-SSOP (Green Package)	Commercial, 0°C to +70°C

9 Package Dimensions (28-SSOP)

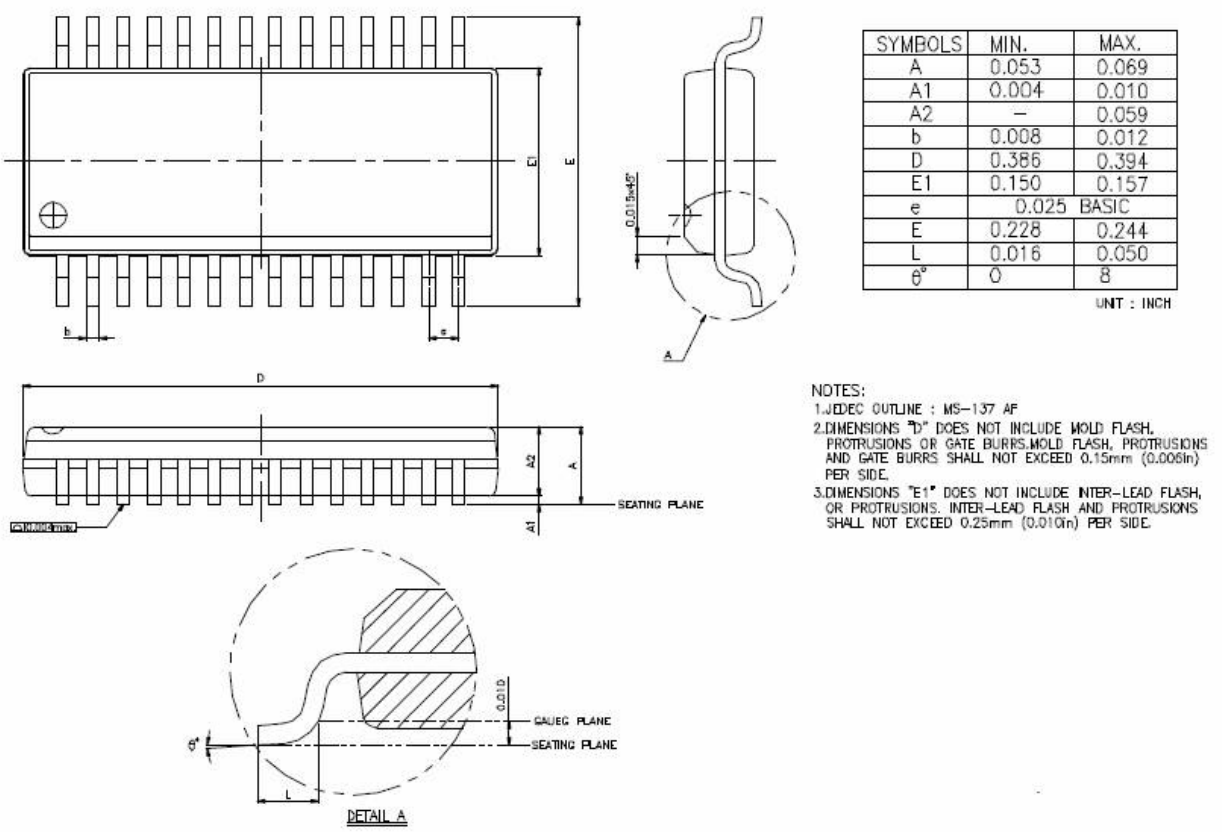


Figure 8. 28 Pin SSOP Package Diagram

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10 Application Circuit

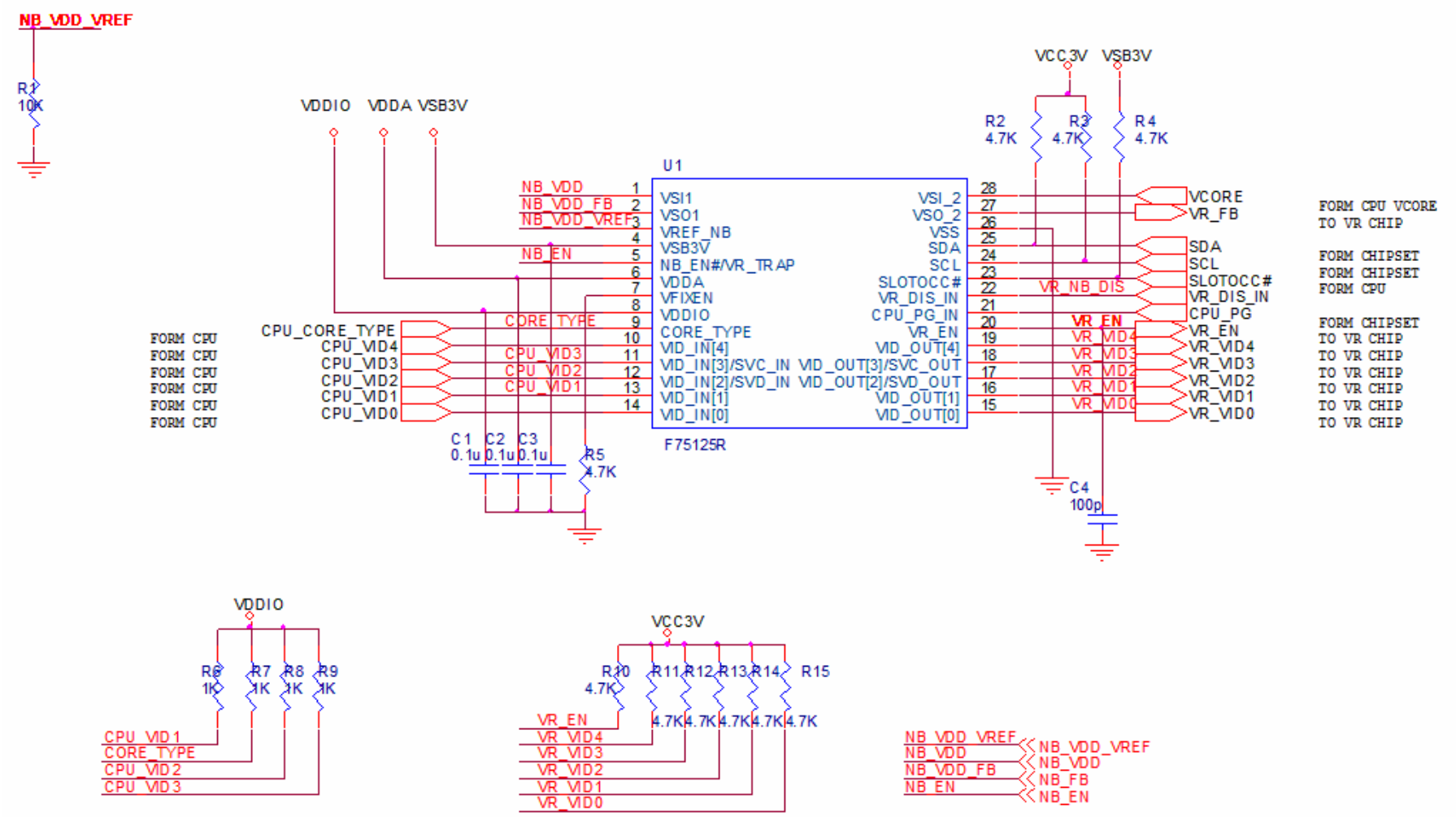

Figure 9. F75125R Parallel VID Output Application Circuit

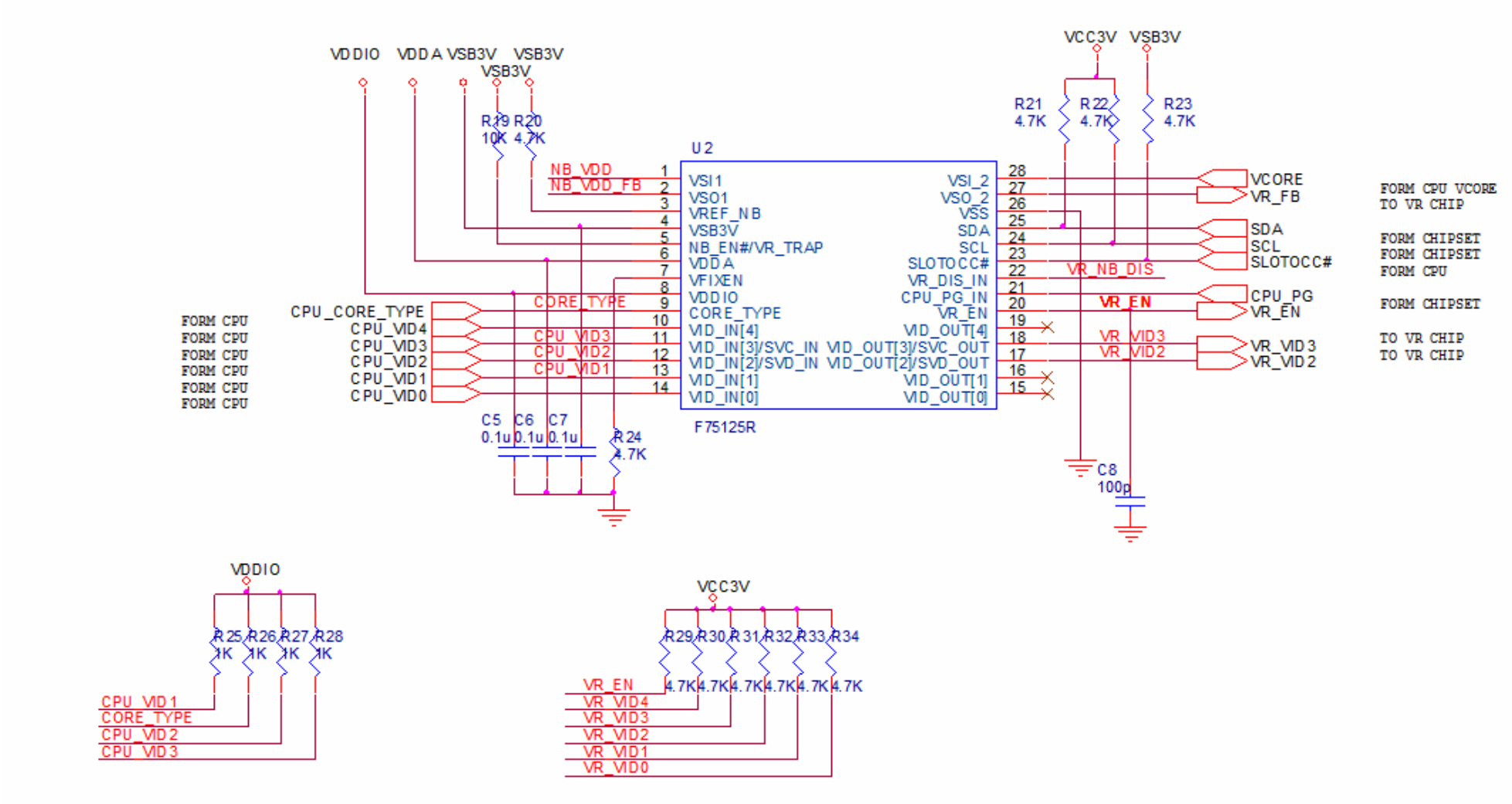

Figure 10. F75125R Serial VID Output Application Circuit