Ordering number : ENA0251

SANYO Semiconductors
DATA SHEET

LA75694M — Monolithic Linear IC For Use in TV/VTR Applications IF Signal Processing (VIF/SIF for Hi-Fi)

Overview

The LA75694M is a PAL/NTSC split Support VIF/SIF for Hi-Fi signal-processing IC that makes the minimum number of adjustments possible. The system is designed so that VCO adjustment makes AFT adjustment unnecessary, thus simplifying the adjustment steps in endproduct manufacturing. PLL detection is adopted in the FM detector, allowing the LA75694M to support multichannel detection for the audio signal. In addition, it also incorporates a buzz canceller that suppresses Nyquist buzz for improved audio quality.

Functions

- VIF Block: VIF Amplifier, Buzz Canceller, BNC, PLL Detector, IF AGC, RF AGC, AFT, Equalizer Amplifier
- 1st SIF Block: 1st SIF Amplifier, 1st SIF Detector, AGC
- SIF Block: HPF, MIX, 500kOSC

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		6	V
Circuit voltage	V_{13}, V_{17}		V_{CC}	V
Circuit current	I_6		-3	mA
	I_{10}		-10	mA
Allowable power dissipation	Pd max	Ta ≤ 50°C, Independent IC	420	mW
		Mounted on a board. *	720	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-55 to +150	°C

* When mounted on a 65×72×1.6mm^3 paper phenol board.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		5	V
Operating voltage	V_{CC} op		4.5 to 5.5	V

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Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, fp = 45.75MHz

VIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current	I_5		38	45	51.8	mA
Maximum RF AGC voltage	$V_{14}H$		V_{CC}-0.5	V_{CC}		V
Minimum RF AGC voltage	$V_{14}L$			0	0.5	V
Input sensitivity	V_i	S1 = OFF	27	33	39	dBμV
AGC range	GR		53	58		dB
Maximum allowable input	V_i max		90	96		dBμV
No-signal video output voltage	V_6		2.1	2.4	2.7	V
Sync. signal tip voltage	V_6 tip		0.7	1.0	1.3	V
Video output level	V_O		0.95	1.1	1.25	Vp-p
Black noise threshold voltage	V_{BTH}		0.5	0.8	1.1	V
Black noise clamp voltage	V_{BCL}		1.2	1.5	1.8	V
Video S/N	S/N		48	52		dB
C-S best	IC-S		38	43		dB
Frequency characteristics	fc	6MHz	-3	-1.5		dB
Differential gain	DG			3	6.5	%
Differential phase	DP			3	5	°C
No-signal AFT voltage	V_{13}		2.0	2.5	3.0	V
Maximum AFT voltage	$V_{13}H$		4.0	4.4	5.0	V
Minimum AFT voltage	$V_{13}L$		0	0.18	1.0	V
AFT detection sensitivity	Sf		14	21	28	mV/kHz
VIF input resistance	R_i	45.75MHz		1.5		kΩ
VIF input capacitance	C_i	45.75MHz		3		pF
APC pull-in range (U)	fpu		0.7	1.5		MHz
APC pull-in range (L)	fpl			-2.0	-1.4	MHz
AFT tolerance frequency 1	ΔFa1		-200	0	200	kHz
VCO1 maximum variable range (U)	dfu		1.0	1.5		MHz
VCO1 maximum variable range (L)	dfl			-2.0	-1.4	MHz
VCO control sensitivity	β		1.2	3.2	5.0	kHz/mV
Synchronization ratio	V_S		25.0	28.5	31.5	%

1st SIF Block

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Conversion gain	V_G		27	33	39	dB
4.5MHz output level	S_O		53	115	180	mVrms
1st SIF maximum input	S_i max		8	16		mVrms
1st SIF input resistance	R_i (SIF)	41.25MHz		2		kΩ
1st SIF input capacitance	C_i (SIF)	41.25MHz		3		pF

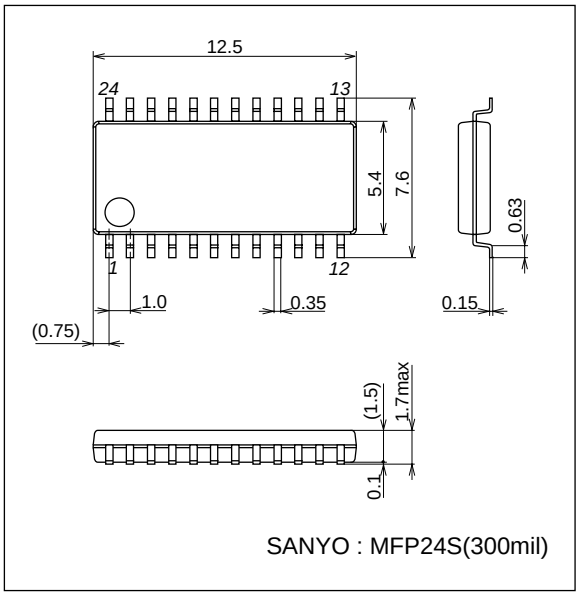
SIF Converter

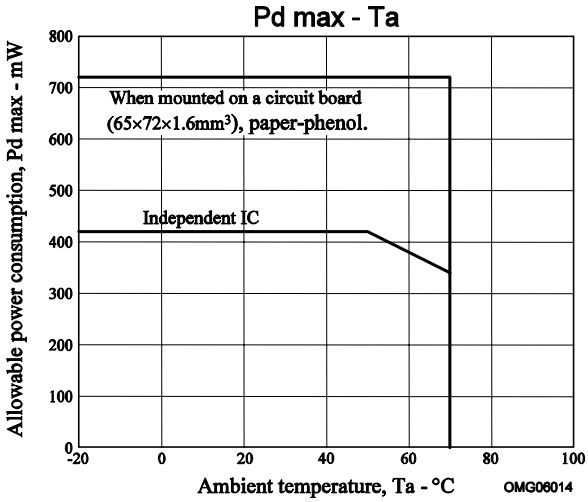
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Conversion gain	V_G (SIF)		8	11	14	dB
Maximum output level	V max		103	109	115	dBμV
Carrier suppression ratio	V_{GR} (4.5)		15	21		dB
Oscillator level	V_{OSC}		35	70		mVp-p
OSC leakage	OSC leak		14	25		dB
Oscillator stop current	I_4				300	μA

Package Dimensions

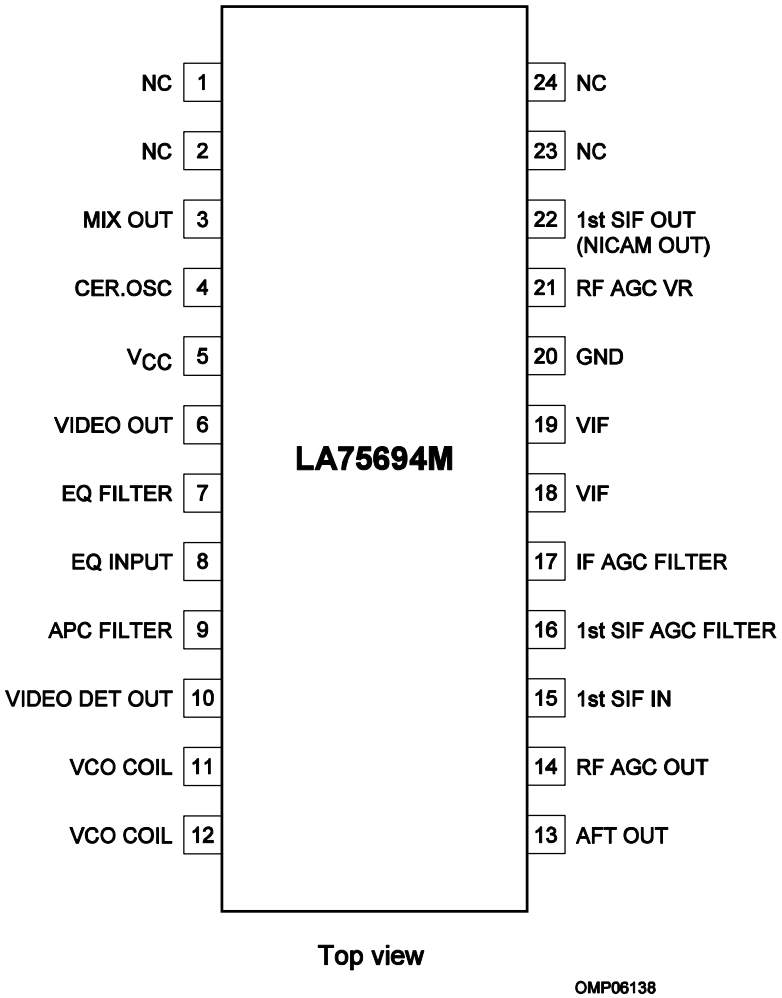
unit : mm

3112B





Pin Assignment



Top view

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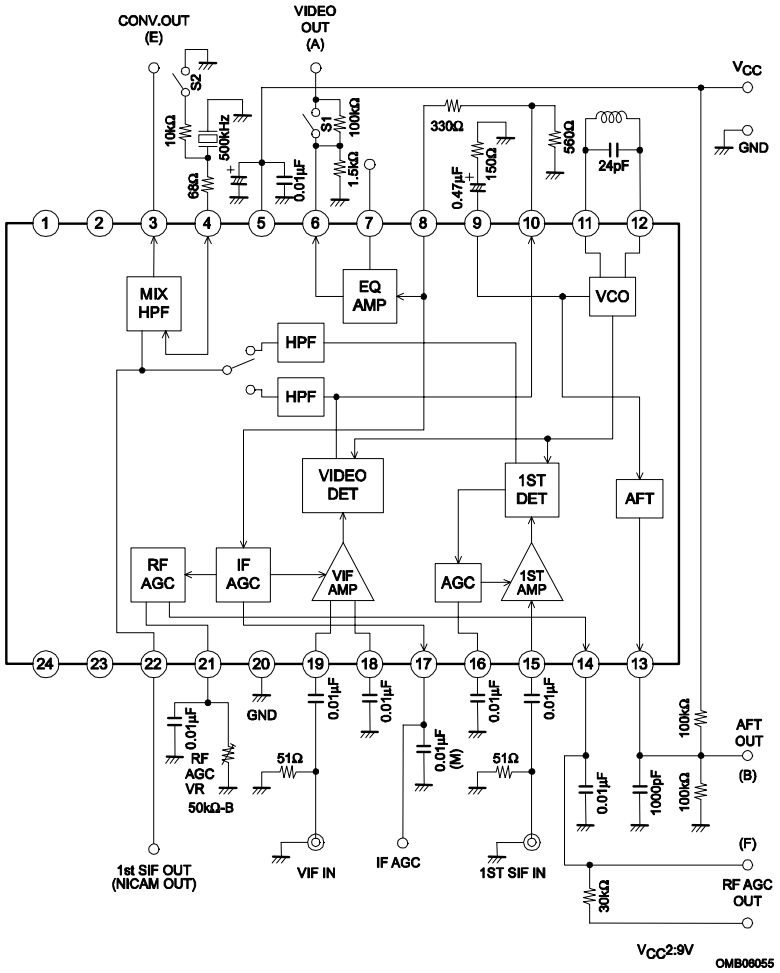
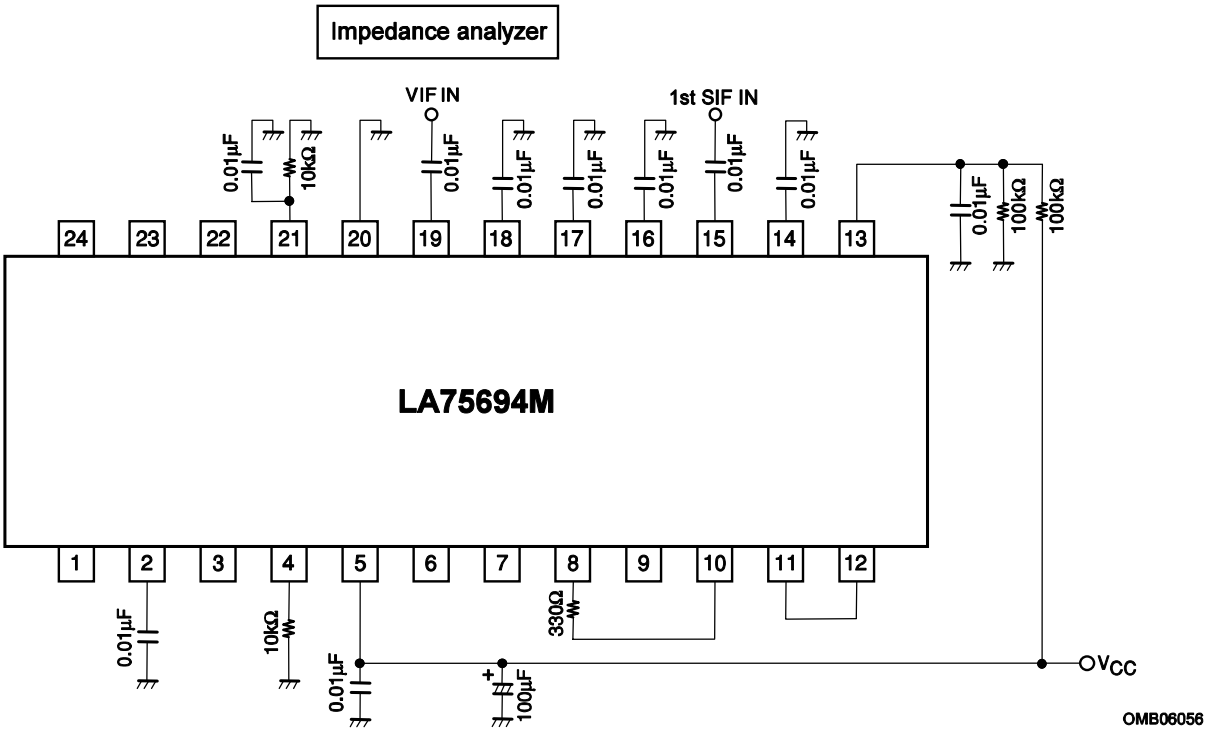
Block Diagram and AC Characteristics Test Circuit



Input Impedance Test Circuit



Test Conditions

V1. Circuit current [I_5]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) RF AGC Vr MAX
(4) Connect an ammeter to the V_{CC} and measure the incoming current.

V2.V3. Maximum RF AGC voltage, Minimum RF AGC voltage [$V_{14}H$, $V_{14}L$]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Adjust the RF AGC Vr (resistor value max.) and measure the maximum RF AGC voltage. ····· F
(4) Adjust the RF AGC Vr (resistor value min.) and measure the minimum RF AGC voltage. ····· F

V4. Input sensitivity [V_i]
(1) Internal AGC
(2) fp = 45.75MHz 400Hz 40% AM (VIF input)
(3) Turn off the S1 and put 100kΩ through.
(4) VIF input level at which the 400Hz detection output level at test point A becomes 0.35Vp-p.

V5. AGC range [GR]
(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) In the same manner as for the V4 (input sensitivity), measure the VIF input level at which the detection output level becomes 0.35Vp-p. ····· Vil
(3) $GR = 20\log \frac{Vil}{V_i}$ dB

V6. Maximum allowable input [V_i max]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM (VIF input)
(3) VIF input level at which the detection output level at test point A is video output (V_O) ±1dB.

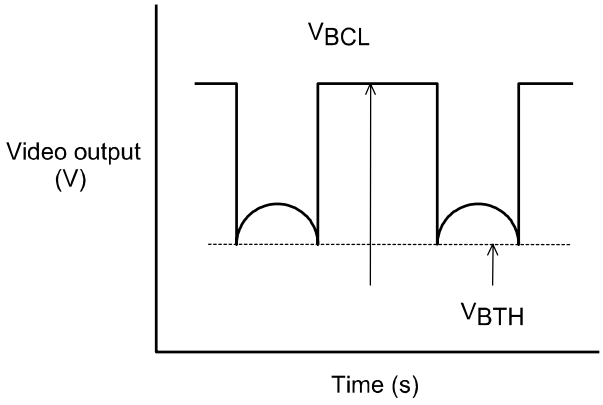
V7. No-signal video output voltage [V_6]
(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Measure the DC voltage of VIDEO output (A).

V8. Sync. signal tip voltage [V_6tip]
(1) Internal AGC
(2) Input a 45.75MHz 10mVrms continuous wave to the VIF input pin.
(3) Measure the DC voltage of VIDEO output (A).

V9. Video output level [V_O]
(1) Internal AGC
(2) fp = 45.75MHz 15kHz 78% AM V_i = 10mVrms (VIF input)
(3) Measure the peak value of the detection output level at test point A. (Vp-p)

V10.V11. Black noise threshold level and clamp voltage [V_{BTH}, V_{BCL}]

(1) Apply DC voltage to the external AGC, IF AGC (pin 17) and adjust the voltage.
(2) fp = 45.75MHz 400Hz 40% AM 10mVrms (VIF input)
(3) Adjust the IF AGC (pin 17) voltage to operate the noise canceller.
Measure the V_{BTH}, V_{BCL} at test point A.



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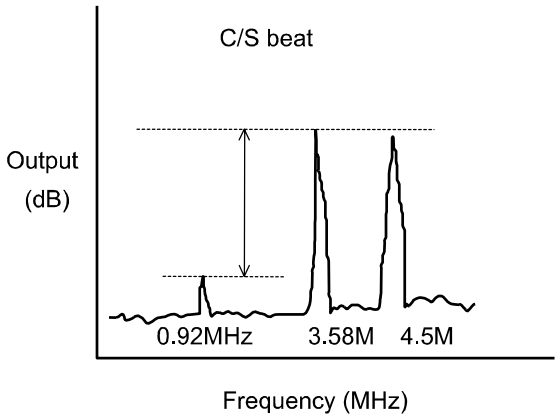
V12. Video S/N [S/N]

(1) Internal AGC
(2) fp = 45.75MHz CW = 10mVrms (VIF input)
(3) Measure the noise voltage at test point A in RMS volts through a 10kHz to 4MHz band-pass filter.
····· Noise voltage (N)

(4) $S/N = 20\log \dfrac{\text{Video portion (Vp-p)}}{\text{Noise voltage (Vrms)}} = 20\log \dfrac{1.12\text{Vp-p}}{\text{Noise voltage (Vrms)}}$ (dB)

V13. C/S beat [IC-S]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) fp = 45.75MHz CW; 10mVrms
fc = 42.17MHz CW; 10mVrms – 10dB
fs = 41.25MHz CW; 10mVrms – 10dB
(3) Adjust the IF AGC (pin 17) voltage so that the output level at test point A becomes 0.72Vp-p.
(4) Measure the difference between the levels for 3.58MHz and 0.92MHz components at test point A.



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V14. Frequency characteristics [fc]

(1) Apply DC voltage to the external AGC IF AGC (pin 17) and adjust the voltage.
(2) SG1 : 45.75MHz continuous wave 10mVrms
SG2 : 45.65MHz to 39.75MHz continuous wave 2mVrms
Add the SG1 and SG2 signals using a T pat and adjust each SG signal level so that the above-mentioned levels are reached and input the added signals to the VIF IN.
(3) First set the SG2 frequency to 45.65MHz, and then adjust the IF AGC voltage (V17) so that the output level at test point A becomes 0.5Vp-p. ····· V1
(4) Set the SG2 frequency to 39.75MHz and measure the output level. ····· V2
(5) Calculate as follows :

$$fc = 20\log \frac{V2}{V1} \text{ (dB)}$$

V15.V16. Differential gain, differential phase [DG, DP]

(1) Internal AGC
(2) fp = 45.75MHz APL50% 87.5% modulation video signal V_i = 10mVrms
(3) Measure the DG and DP at test point A.

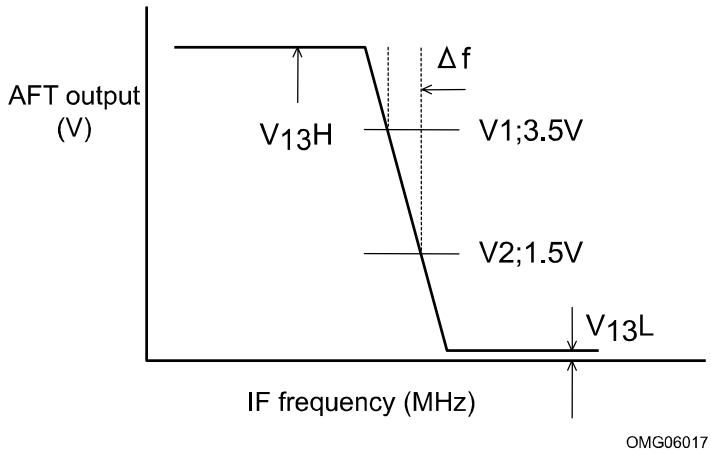
V17. No-signal AFT voltage [V_{13}]

(1) Internal AGC
(2) Measure the DC voltage at the AFT output (B).

V18.V19.V20. Maximum, minimum AFT output voltage, AFT detection sensitivity [V_{13}H, V_{13}L, Sf]

(1) Internal AGC
(2) fp = 45.75MHz ±1.5MHz Sweep = 10mVrms (VIF input)
(3) Maximum voltage : V_{13}H, minimum voltage : V_{13}L.
(4) Measure the frequency deviation at which the voltage at test point B changes from V1 to V2. ····· Δf

$$Sf = \frac{2000(mV)}{\Delta f(kHz)} \text{ mV/kHz}$$



V21.V22. VIF input resistance, Input capacitance [R_i, C_i]

(1) Referring to the Input Impedance Test Circuit, measure R_i and C_i with an impedance analyzer.

V23.V24. APC pull-in range [fpu, fpl]

(1) Internal AGC
(2) fp = 39MHz to 51MHz continuous wave; 10mVrms
(3) Adjust the SG signal frequency to be higher than fp = 45.75MHz to bring the PLL to unlocked state.
Note : The PLL is assumed to be in unlocked state when a beat signal appears at test point A.
(4) When the SG signal frequency is lowered, the PLL is brought to locked state again. ····· f1
(5) Lower the SG signal frequency to bring the PLL to unlock state.
(6) When the SG signal frequency is raised, the PLL is brought to locked state again. ····· f2
(7) Calculate as follows :

fpu = f1 – 45.75MHz
fpl = f2 – 45.75MHz

V25. AFT tolerance frequency 1 [ΔFa1]

(1) Internal AGC
(2) SG1 : 43.75MHz to 47.75MHz variable continuous wave 10mVrmns
(3) Adjust the SG1 signal frequency so that the AFT output DC voltage (test point B) becomes 2.5V; that SG1 signal frequency is f1.
(4) External AGC (Adjust the V17.)
(5)Apply 5V to the IF AGC (pin 17) and then pick up the VCO oscillation frequency from GND, etc.; and measure the frequency ····· f2
(6) Calculate as follows :

AFT tolerance frequency : ΔFa1 = f2 – f1 (kHz)

V26.V27. VCO maximum variable range (U, L) [dfu, dfl]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(3) fl is taken as the frequency when 1V is applied to the APC pin (pin 9).
In the same manner, fu is taken as the frequency when 5V is applied to the APC pin (pin 9).

dfu = fl–45.75MHz
dfl = fl–45.75MHz

V28. VCO control sensitivity [β]

(1) Apply the V_{CC} voltage to the external AGC, IF AGC (pin 17).
(2) Pick up the VCO oscillation frequency from the VIDEO output (A), GND, etc. and adjust the VCO coil so that the frequency becomes 45.75MHz.
(4) f1 is taken as the frequency when 3.0V is applied to the APC pin (pin 9).
In the same manner, f2 is taken as the frequency when 3.4V is applied to the APC pin (pin 9).

$$\beta = \frac{f2-f1}{400} \text{ (kHz/mV)}$$

V29. Synchronization ratio [V_S]

(1) Internal AGC
(2) fp = 45.75MHz 87.5% 10STEP B/W
V_i = 10mVrms
(3) Measure the output amplitude at the measuring point A. ····· Vvideo
(4) Measure the pedestal voltage (DC) at the measuring point A. ····· Vped

V_S = (Vped–V_6tip) / Vvideo×100 (%)

F1. 1st SIF conversion gain [V_G]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 500μV (1st SIF input) ····· V1
(3) Detection output level at test point C (Vrms) ····· V2 (4.5MHz)

(4) $VG = 20\log \frac{V2}{V1}$ dB

F2. 4.5MHz output level [S_O]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (1st SIF input) ····· V1
(3) Detection output level at test point C (4.5MHz) ····· S_O (mVrms)

F3. 1st SIF maximum input [Si max]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; variable (1st SIF input)
(3) Input level at which the detection output at test point C (4.5MHz) becomes S_O ±2dB. ····· Si max

F4.F5. 1st SIF input resistance, Input capacitance [R_i (SIF), C_i (SIF)]

(1) Using an input analyzer, measure R_i and C_i in the input impedance measuring circuit.

C1. Converter conversion gain [V_G (SIF)]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 316μV (1st SIF input)
(3) Measure the 6MHz component at test point E (MIX output) ····· V1
(4) Measure the 4.5MHz component at test point F (NICAM output). ····· V2

(5) $V_G(SIF) = 20\log \frac{V1}{V2}$ dB

C2. SIF converter maximum output level [V max]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 10mV (1st SIF input)
(3) Measure the 6MHz component at test point E (MIX output). ····· V max (dBμV)

C3. Carrier suppression ratio [V_{GR} (4.5)]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 316μV (1st SIF input)
(3) Measure the 6MHz component at test point E (MIX output). ····· V_6 (dBμV)
(4) Measure the 4.5MHz component at test point E (MIX output). ····· $V_{4.5}$ (dBμV)
(5) Perform the following calculation.
Carrier suppression ratio V_{GR} (4.5) (dB) = $V_6 - V_{4.5}$

C5. OSC leakage [OSC leak]

(1) Internal AGC
(2) fp = 45.75MHz CW; 10mV (VIF input)
fs = 41.25MHz CW; 316μV (1st SIF input)
(3) Measure the 6MHz component at test point E (MIX output). ····· V_6 (dBμV)
(4) Measure the 500kHz component at test point E (MIX output). ····· $V_{0.5}$ (dBμV)
(5) Perform the following calculation.
Carrier suppression ratio OSC leak (dB) = $V_6 - V_{0.5}$

Note 1) Unless otherwise specified for VIF test, apply the V_{CC} voltage to the IF AGC and adjust the VCO coil so that oscillation occurs at 45.75MHz.

2) Unless otherwise specified, the SW1 must be ON.

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