QLUX2108-PT280C Device Data Sheet

Utopia Level 2 Slave to Utopia Level 1 Master Bridge

1.0 Utopia Level 2/1 Bridge Core Features

- Implements an Utopia L2 Slave and Utopia L1 Master providing a solution to bridge Utopia Level 1 Slave devices to a Level 2 Master
- Compliant with ATM-Forum af-phy-0039.000 (Level 2) and af-phy-0017.000 (Level 1)
- Implements 8-bit data busses
- Level 2 interface implements a single PHY using MPHY mode with direct status indication
- Level 2 interface meets 50MHz performance offering up to 400Mbps cell rate transfers
- Level 1 interface meets 25MHz performance offering up to 200Mbps cell rate transfers
- Single chip solution for improved system integration
- Supports cell level transfer mode
- Cell and clock rate decoupling with on chip FIFOs
- Up to 2 KByte of on chip FIFO per data direction
- Integrated management interface and built-in errored cell discard
- ATM Cell size programmable via external pins from 16 to 128 bytes
- Level 2 MPHY address programmable via external pins
- Optional Utopia parity generation/checking enable/disable via external pin
- Built in JTAG port (IEEE1149 compliant)
- Simulation model available for system level verification (Contact Quicklogic for details)
- Solution also available as flexible Soft-IP core, delivered with a full device modelization and verification testbenches

QUICKLOGIC

2.0 Utopia Overview

The Utopia (Universal Test & Operations PHY Interface for ATM) interface is defined by the ATM Forum to provide a standard interface between ATM devices and ATM PHY or SAR (Segmentation And Re-assembly) devices.

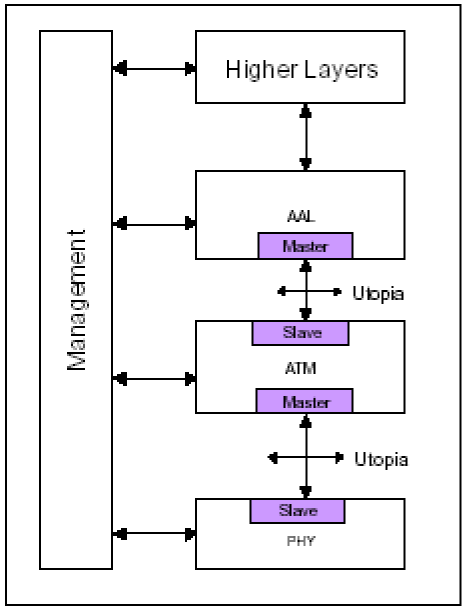

Figure 1: Utopia Reference Model

The Utopia Standard defines a full duplex bus interface with a Master/Slave paradigm. The Slave interface responds to the requests from the Master. The Master performs PHY arbitration and initiates data transfers to and from the Slave device.

The ATM forum has standardized the Utopia Levels 1 (L1) to 3 (L3). Each level extends the maximum supported interface speed from OC3, 155Mbps (L1) over OC12, 622Mbps (L2) to 3.2Gbit/s (L3).

The following Table 1 gives an overview of the main differences in these three levels.

Table 1: Utopia Level Differences

Utopia Level	Interface Width	Max. Interface Speed	Theoretic (typical) Throughput
1	8-bit	25 MHz	200 Mbps (typ. OC3 155 Mbps)
2	8-bit, 16-bit	50 MHz	800 Mbps (typ. OC12 622 Mbps)
3	8-bit, 32-bit	104 MHz	3.2 Gbps (typ. OC48 2.5 Gbps)

Utopia Level 1 implements an 8-bit interface running at up to 25MHz. Level 2 adds a 16 Bit interface and increases the speed to 50MHz. Level 3 extends the interface further by a 32 Bit word-size and speeds up to 104MHz providing rates up to 3.2 Gbit/s over the interface.

In addition to the differences in throughput, Utopia Level 2 uses a shared bus offering to physically share a single interface bus between one master and up to 31 slave devices (Multi-PHY or MPHY operation). This allows the implementation of aggregation units that multiplex several slave devices to a single Master device. The Level 1 and Level 3 are point-to-point only, whereas Level 1 has no notion of multiple slaves. Level 3 still has the notion of multiple slaves, but they must be implemented in a single physical device connected to the Utopia Interface.

3.0 Utopia L2 Slave to L1 Master Bridge Application

Utopia Level 2 offers the notion of multiple PHYs (MPHY) and a shared bus topology to connect several PHY devices to an ATM Layer device.

The L2 Slave to L1 Master bridge implements the necessary interfaces enabling to connect Level 1 PHY devices to such a Level 2 topology. Each Bridge still implements a single Port, but it can be addressed individually using the Level 2 MPHY protocol.

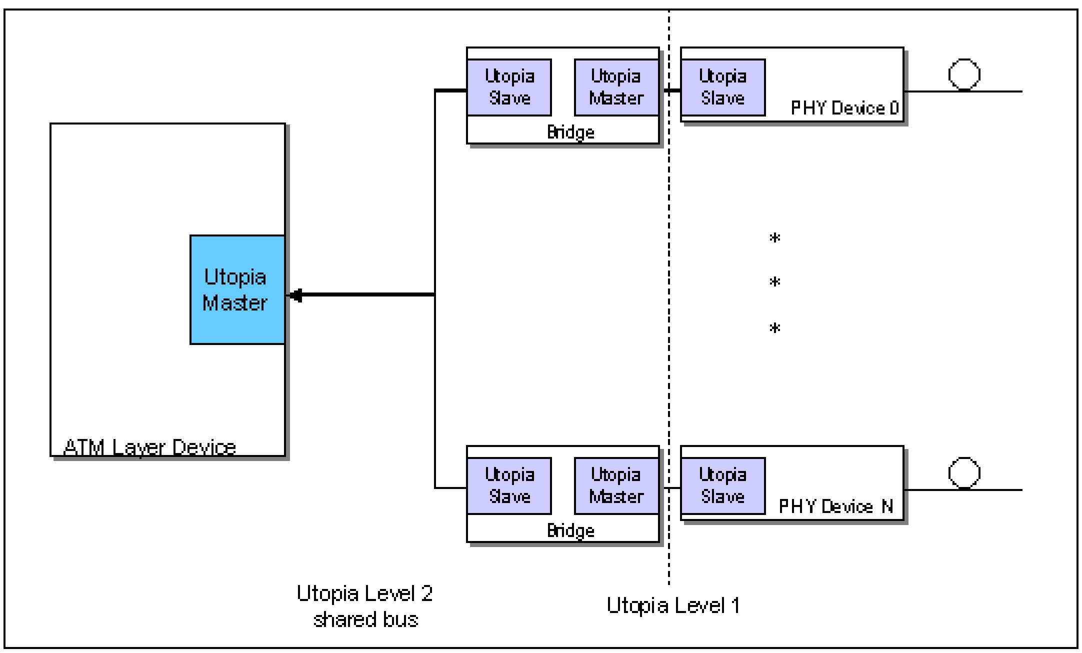

Figure 2: Utopia Shared Bus Topology

4.0 Application

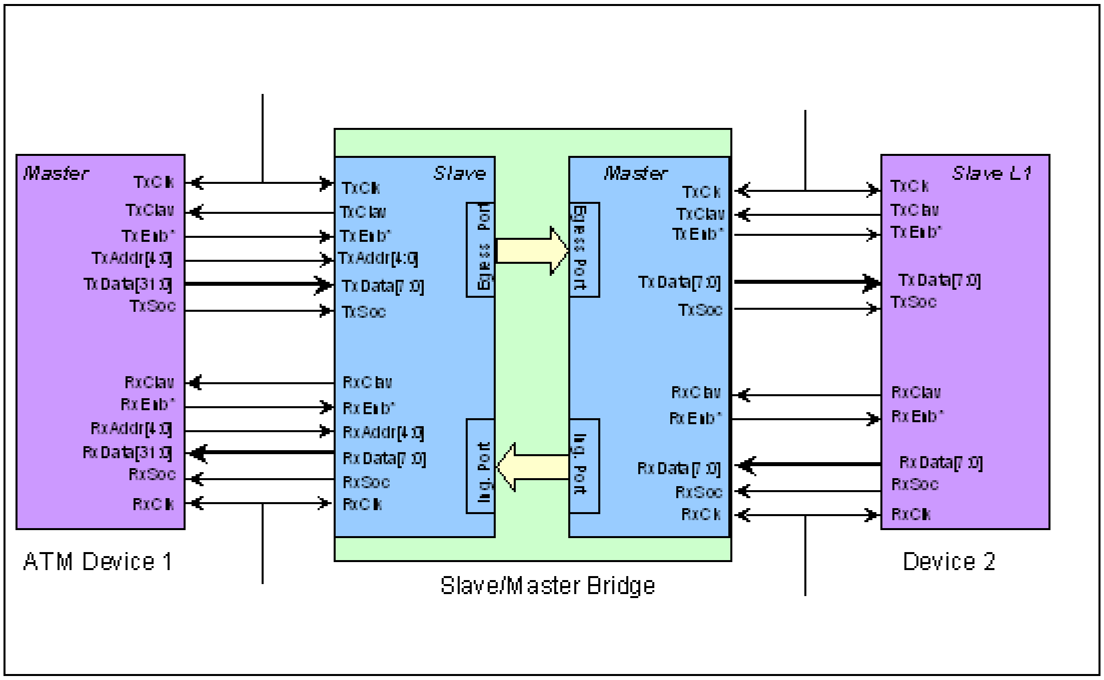

Figure 3: Slave/Master Bridge converting Utopia Levels

Data flows from the Bridge's TX Ports to the corresponding TX Port on the other side of the bridge and the RX Port to the RX Port accordingly.

The following figure shows an application using two bridges to connect two PHY devices to a single, dual-PHY master device. The cell-available signals of the two slaves are connected to the according ports of the master (direct status indication). The two bridges would usually have the addresses 0 and 1 set to each other.

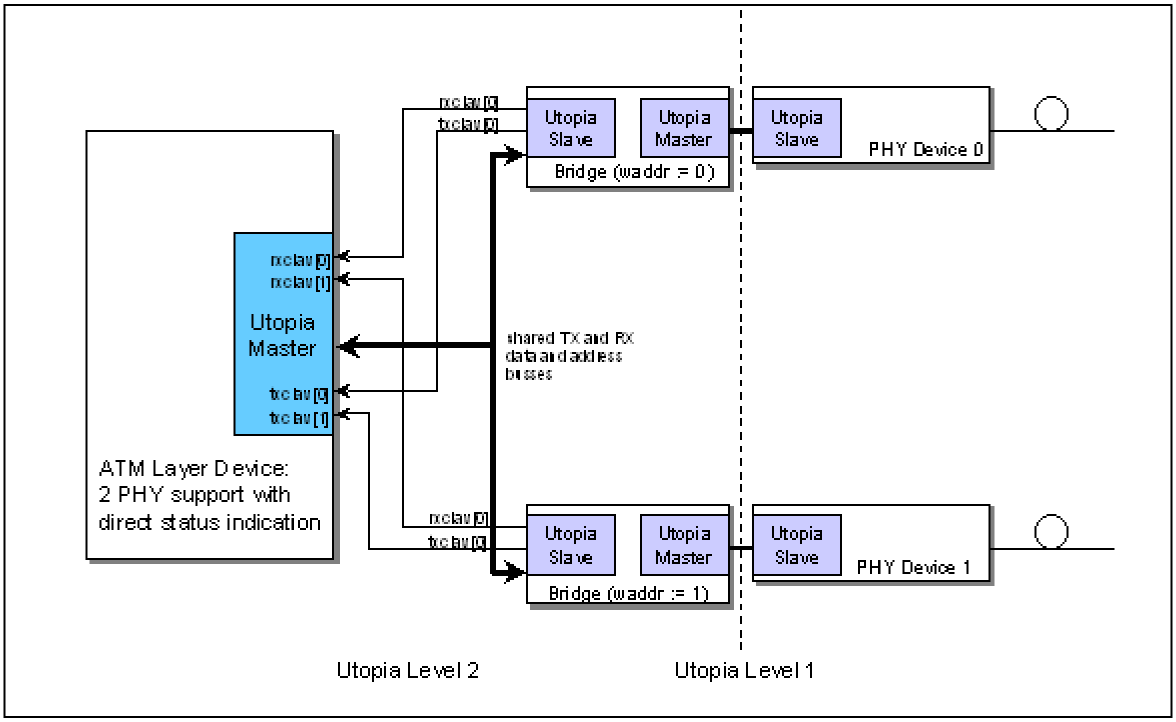

Figure 4: Dual PHY application

5.0 Core Pinout

On the Utopia interfaces, the Core implements all the required Utopia signals and provides all the Utopia optional signals (Indicated by an 'O' in the following tables). The optional Utopia signals are activated during the Core configuration and inactive Utopia signals should be left unconnected (Outputs) or tied to a zero logic level (inputs) as specified in the following Tables.

In addition to the Utopia Interface signals, error indication signals are available for error monitoring or statistics. An error indication always shows that a cell has been discarded by the bridge. Possible errors are parity or cell-length errors on the receive interface of the corresponding Utopia Interfaces.

All Utopia interfaces work in the same transfer mode (cell level). A mix is not possible.

To identify the sides of the core the notion "WEST" and "EAST" for the corresponding interfaces will be used.

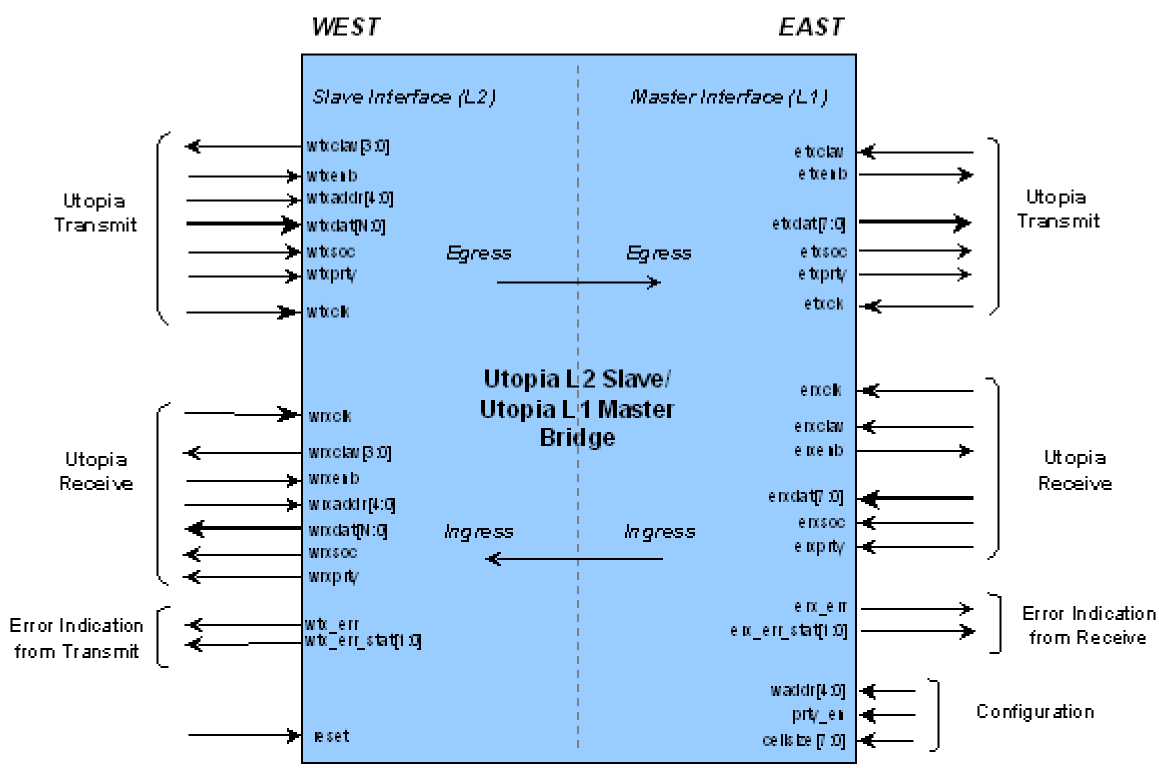

Figure 5: Utopia Level 2 Slave to Level 1 Master Bridge Top Entity

5.1 Signal Descriptions

Table 2: Global Signal

Pin	Mode	Description
reset	In	Active high chip reset

Table 3: Device Management Interface

Pin	Mode	Description
wtx_err	Out	Transmit error indication on west interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the west interface and is discarded.
wtx_err_stat(1:0)	Out	Transmit error status information for west interface. When wtx_err is driven, indicates the error status of the discarded cell: • wtx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • wtx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).
erx_err(n)	Out	Receive error indication on east interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the east interface side.
erx_err_stat(n) (1:0)	Out	Receive error status information for east receive interface. When etx_err is driven, indicates the error status of the discarded cell: • etx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • etx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).

NOTE: *wtx_.. signals are sampled with west transmit clock (wtxclk). etx_.. signals are sampled with west receive clock (wrxclk).*

Table 4: West Utopia Level 2 Slave Transmit Interface

Pin	Mode	Description
wtxclk	In	50MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
wtxdata[7:0]	In	Transmit data bus. The width of the data bus is be 8 Bit. N is the MSB.
wtxprty(O)	In	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be tied to '0'.
wtxsoc	In	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
wtxenb	In	Active low transmit data transfer enable.
wtxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
wtxclav[3:1] (O)	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four. Not used and not available.
wtxaddr[4:0]	In	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB.

NOTE: *(O) indicates optional signals.*

Table 5: West Utopia Level 2 Slave Receive Interface

Pin	Mode	Description
wrxclk	In	50MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
wrxdata[7:0]	Out	Receive data bus.
wrxprty (O)	Out	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
wrxsoc	Out	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
wrxenb	In	Active low transmit data transfer enable.
wrxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
wrxclav[3:1] (O)	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four. Not used and not available.
wrxaddr(4:0)	In	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB.

Table 6: East Utopia Level 1 Master Transmit Interface

Pin	Mode	Description
etxclk	In	25MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
etxdata[7:0]	Out	Transmit data bus.
erxprty (O)	Out	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be left open.
erxsoc	Out	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
etxenb	Out	Active low transmit data transfer enable.
etxclav	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.

NOTE: *(O) indicates optional signals.*

Table 7: East Utopia Level 1 Master Receive Interface

Pin	Mode	Description
erxclk	In	25MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
erxdata[7:0]	In	Receive data bus.
erxprty (O)	In	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
erxsoc	In	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
erxenb	Out	Active low transmit data transfer enable.
erxclav	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.

Table 8: Device Configuration Pins

Pin	Mode	Description
waddr[4:0]	In	Programs the Utopia L2 Slave address used on the west interfaces (tx and rx).
prty_en	In	Enable parity checking on the Utopia interface. If disabled (tied to 0), the wrx_err_stat(0) signal can be ignored and left open and the rx parity input should be tied to 0. Also the tx parity pins can be left open.
cellsize[7:0]	In	Define cellsize: sets the size in bytes of a cell. Binary value to be set usually by board wiring

The configuration pins are not intended for change during operation. They are usually board wired to configure the device for operation.

6.0 Global Signal Distribution

The externally provided Utopia Transmit and Receive clocks are connected to global resources to provide low skew and fast chip level distribution. In both data directions, the two corresponding Utopia Interfaces are decoupled by asynchronous FIFOs.

Therefore each interface runs completely independently each at its own tx and rx clocks which typically are up to 50 MHz on the WEST and up to 25 MHz on the EAST interface.

The Error indications of the two receive interfaces are always sampled within the west clock domains. The errors of the east rx interface is available on the erx_err signal, which is handled using the west clock domain (wrxclk). The west tx (receiving) error is directly derived from the west tx block (wtxclk).

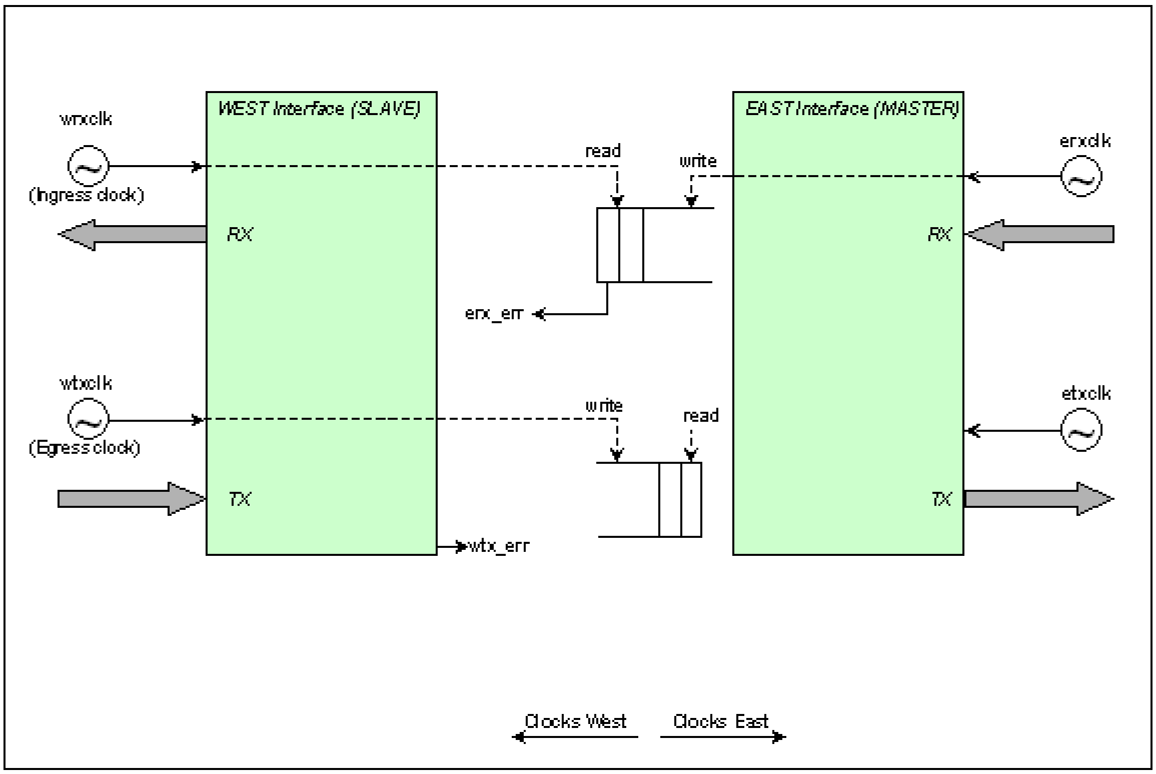

Figure 6: Slave/Master Bridge Clock Distribution

7.0 Functional Description – Utopia Interface

The Utopia Bridge implements a single port. The West Interface (Utopia L2) operates in MPHY mode with direct status indication. This offers to connect up to 4 bridges to a single Master (exceeding the Utopia L2 bus bandwidth). It implements a single clav signal per direction (clav[0]) and the address bus to select the device within a shared bus topology.

The East Interface (L1) has no notion of MPHY. It has a single clav signal and no address bus.

7.1 Utopia Interface Single PHY Transmit Interface (L1)

The Transmit interface is controlled by the Master.

The transmit interface has data flowing in the same direction as the ATM enable `ut_tx_enb`. The ATM transmit block generates all output signals on the rising edge of the `ut_txclk`.

Transmit data is transferred from the Master to Slave via the following procedure. The Slave indicates it can accept data using the `ut_txclav` signal, then the Master drives data onto `ut_txdat` and asserts `ut_txenb`. The Slave controls the flow of data via the `ut_txclav` signal.

7.1.1 Cell Level Transfer - Single Cell

The Slave asserts `ut_txclav` **1** when it is capable of accepting the transfer of a whole cell. The Master asserts `ut_txenb` (Low) to indicates that it drives valid data to the Slave **2**. Together with the first octet of a cell, the Master device asserts `ut_txsoc` for one clock cycle **3**.

To ensure that the Master does not cause transmit overrun, the Slave deasserts `ut_txclav` at least 4 cycles before the end of a cell if it cannot accept the immediate transfer of the subsequent cell **4**.

The Master can pause the cell transfer by de-asserting `ut_txenb` **5**. To complete the transfer to the Slave, the Master de-asserts `ut_tx_enb` **6**.

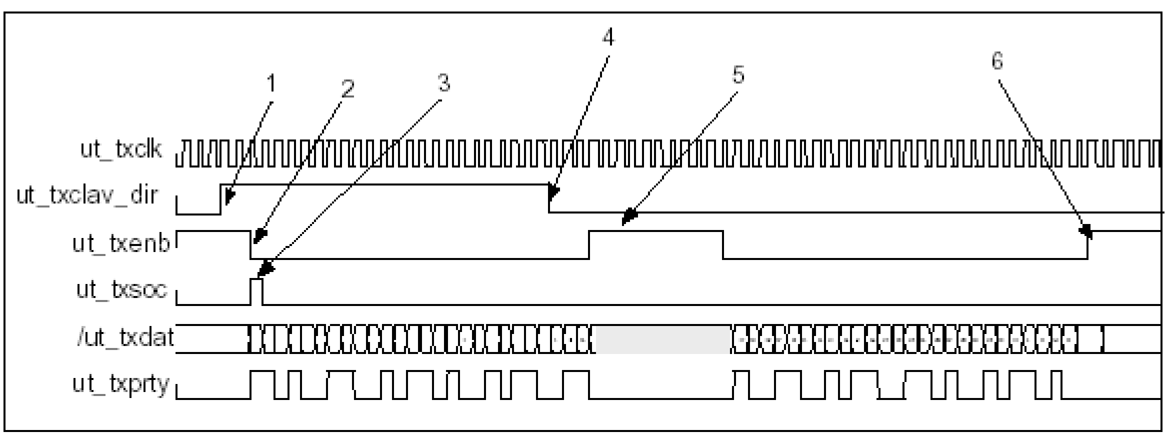

Figure 7: Single Cell Transfer – Cell Level Transfer

7.1.2 Cell Level Transfer – Back to Back Cells

When, during a cell transfer, the Slave is able to receive a subsequent cell, the Master can keep `ut_txenb` asserted between two cells **1** and asserts `ut_txsoc`, to start a new cell transfer, immediately after the last octet of the previous cell **2**.

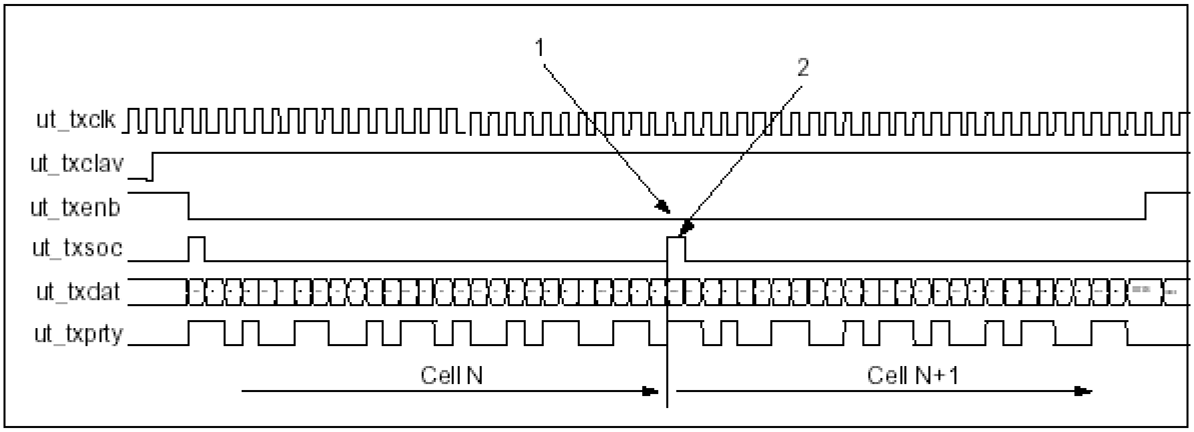

Figure 8: Back to Back Cell Transfer – Cell Level Transfer

7.2 Utopia Interface Single PHY Receive Interface (L1)

The Receive interface is controlled by the Master. The receive interface has data flowing in the opposite direction to the Master enable `ut_rxenb`.

Receive data is transferred from the Slave to Master via the following procedure. The Slave indicates it has valid data, then the Master asserts `ut_rxenb` to read this data from the Slave. The Slave indicates valid data (thereby controlling the data flow) via the `ut_rxclav` signal.

7.2.1 Cell Level Transfer - Single Cell

The Slave asserts `ut_rx_clav` when it is ready to send a complete cell to the Master device **1**. The Master interface asserts `ut_rxenb` to start the cell transfer. The Slave samples `ut_rxenb` and starts driving data **2**. The Slave asserts `ut_rxsoc` together with the cell first word to indicate the start of a cell **3**.

The Master can pause a transfer by de-asserting `ut_rxenb` **4**. The Slave samples high `ut_rxenb` and stops driving data **5**. To resume the transfer, the Master re-asserts `ut_rxenb` **6**. The Slave samples low `ut_rxenb` and starts driving valid data **7**.

The Master drives `ut_txenb` high one before the expected end of the current cell if the Slave has no more cell to transfer **8**. The Slave de-asserts `ut_rxclav` to indicate that no new cell is available **9**.

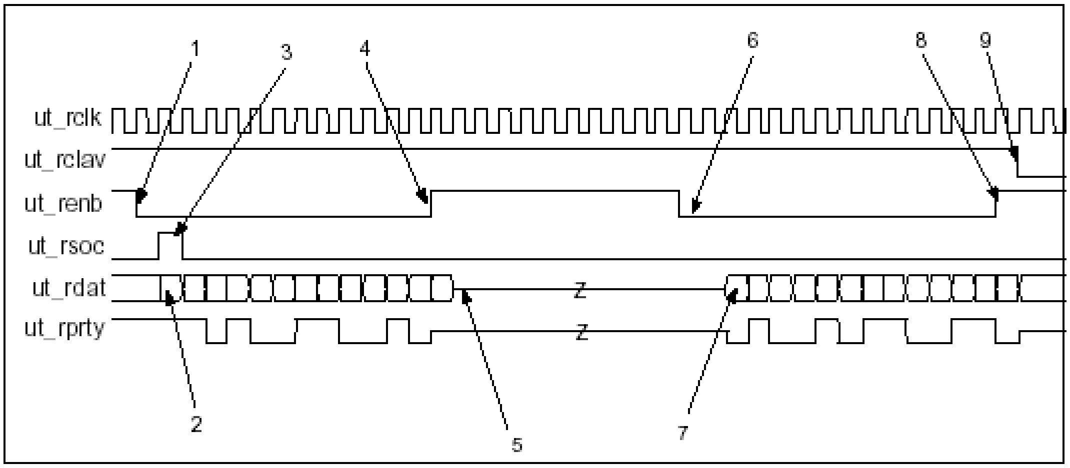

Figure 9: Single Cell Transfer - Cell Level Transfer

7.2.2 Cell Level Transfer - Back to Back Cells

If the Master keeps `ut_rxenb` asserted at the end of a cell transfer **1** and if the Slave has a new cell to send, the Slave keeps `ut_rxclav` asserted **2** and immediately drives the new cell asserting `ut_rxsoc` to indicate the start of a new cell **3**.

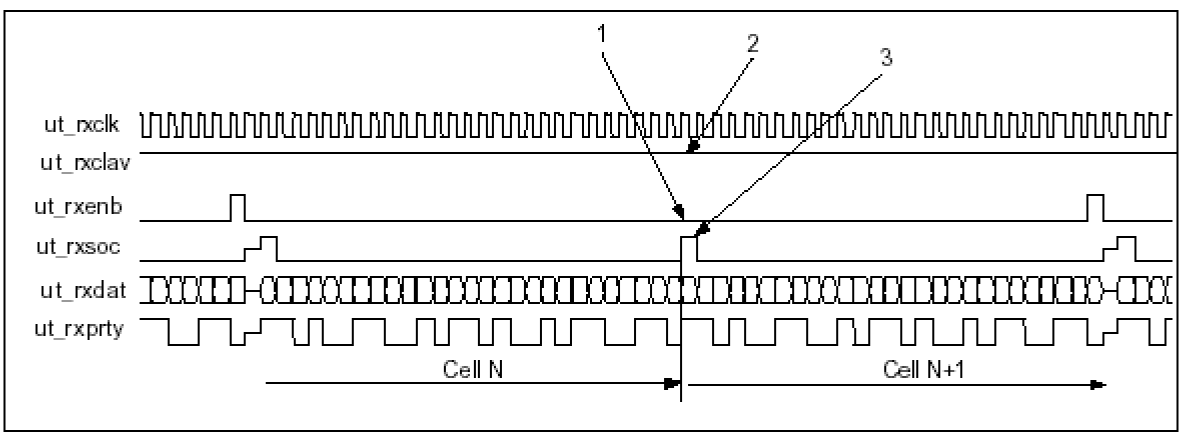

Figure 10: Back to Back Cells Transfer - Cell Level Transfer

NOTE: *If the Master keeps `ut_rxenb` asserted at the end of a packet and if the Slave does not have a new cell available, the Slave de-asserts `ut_rxclav` and the data of the bus `ut_rxdat` are invalid.*

7.3 Utopia Interface MPHY Transmit (L2)

When operating in MPHY mode, the Master checks, (Typically in a round robin fashion) the status of all the Slave ports. Two options are defined by the Utopia standard:

- Polled status indication with all the PHY ports using a shared single CLAV signal to report their status to the Master
- Direct status indication with one CLAV implemented per PHY port or per Utopia group.

In MPHY mode only one transmit PHY port is selected at a time for data transfers but the Master continuously polls the status of the Slave's other PHY ports.

The Bridge implements the second approach, using direct status indication.

7.3.1 MPHY Operation with Direct Status

For each PHY port, a status signal `ut_txclav` is permanently available. The Utopia Bus then supports up to four PHY ports, each using one CLAV signal (Slave port `ut_txclav_dir(n)`).

For each port independently, `ut_txclav_dir(n)` is asserted when enough space is available for a complete cell in the port FIFO 1 and `ut_txclav_dir(n)` is de-asserted when the corresponding port FIFO cannot receive the subsequent cell **2**.

Status signals and cell transfers are independent of each other for each port. No address information is needed to obtain status information. Address information must be valid only for selecting a PHY port prior to one or multiple cell transfers. To select a port, the Master de-asserts `ut_txenb` **3**, puts address port on `ut_txaddr(4:0)` **4**, the port is selected by the Slave when `ut_txenb` goes low (Re-asserted by the Master) **5**.

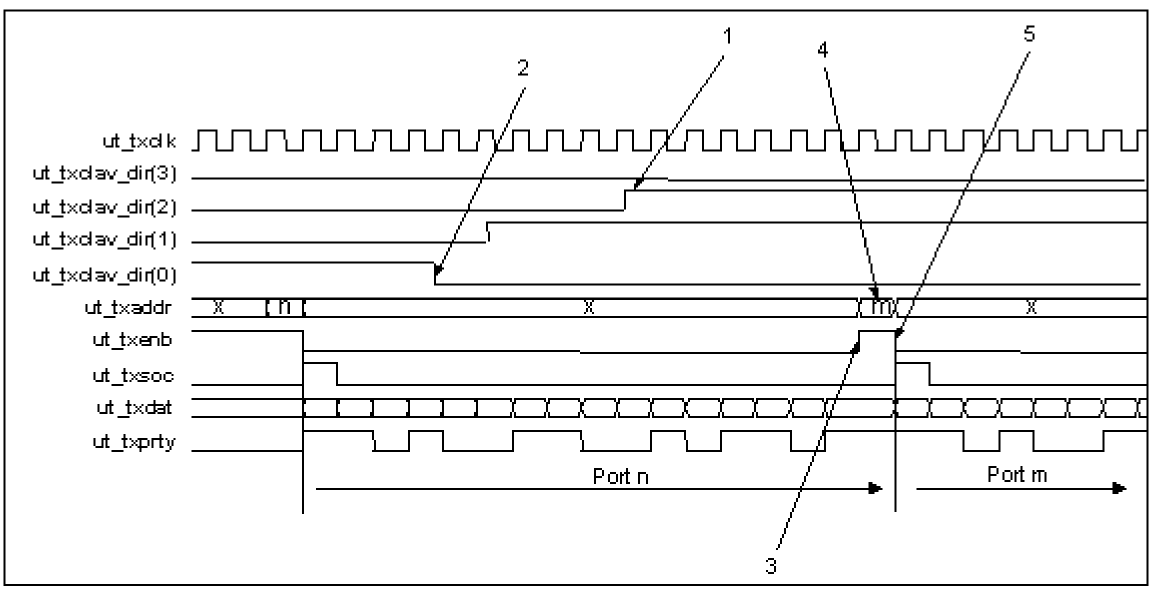

Figure 11: MPHY Transmit - Direct Status Indication

As defined for single CLAV Utopia Transmit, the Master can pause a transfer and implicitly re-select a PHY port.

7.4 Utopia Interface MPHY Receive (L2)

When operating in MPHY mode, the Master checks, (Typically in a round robin fashion) the status of all the Slave ports. Two options are defined by the Utopia standard:

- Polled status indication with all the PHY ports using a signal CLAV signal to report their status to the Master
- Direct status indication with one CLAV implemented per PHY port or per Utopia group.

In MPHY mode only one receive PHY port is selected at a time for data transfers but the Master can continuously polls the status of the Slave PHY ports.

7.4.1 MPHY Operation with Direct Status

For each PHY port, a status signal `ut_rxclav_dir(n)` is permanently available. For each port independently, `ut_rxclav_dir(n)` is asserted when the corresponding PHY port has a cell available in its FIFO 1 and `ut_rxclav_dir(n)` is de-asserted when the corresponding port FIFO cannot transmit a complete cell to the Master **2**.

Status signals and cell transfers are independent of each other for each port. No address information is needed to obtain status information. Address information must be valid only for selecting a PHY port prior to one or multiple cell transfers. To select a port, the Master de-asserts `ut_rxenb` **3**, puts address port on `ut_rxaddr(4:0)` **4**, the port is selected by the Slave when `ut_rxenb` goes low (Re-asserted by the Master) **5**.

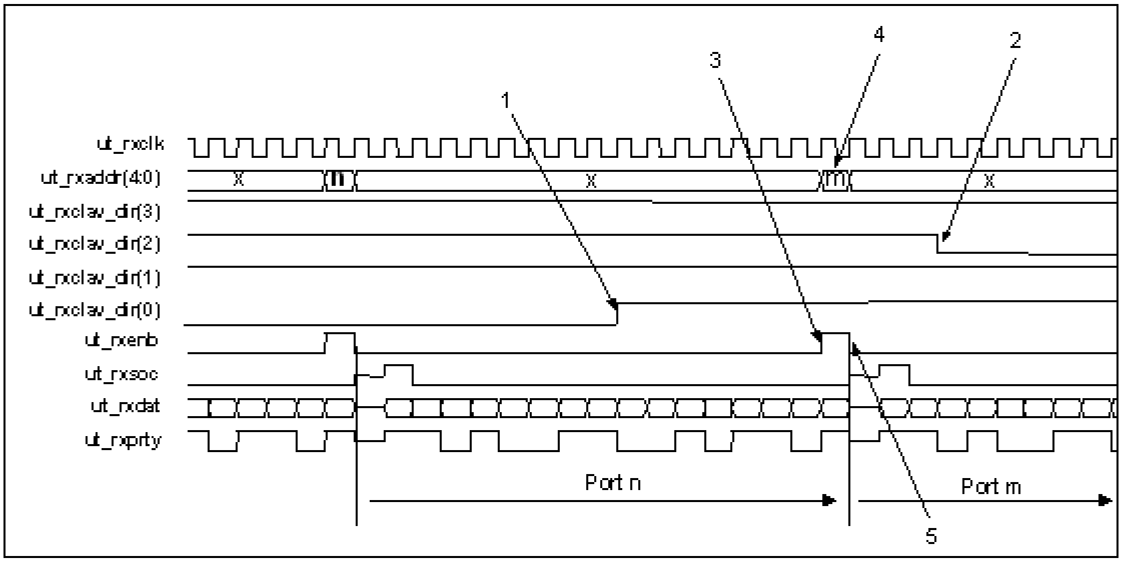

Figure 12: MPHY Receive - Direct Status Indication

8.0 Core Management and Error Handling

On Egress, the Core is designed to handle and report Utopia errors such as Parity error or wrong cell length. Errored cells are discarded with an error status indication provided to the user PHY application.

When an errored cell is received on the Utopia interface, the Core discards the complete cell and provides a cell discard indication to the User PHY application (Signal `eg_err(n)` asserted) **1** together with a cell discard status (Signal `eg_err_stat(1:0)`) **2**.

NOTE: *eg_err is routed to the corresponding `wtx_err` and `etx_err` respectively (see Figure 5).*

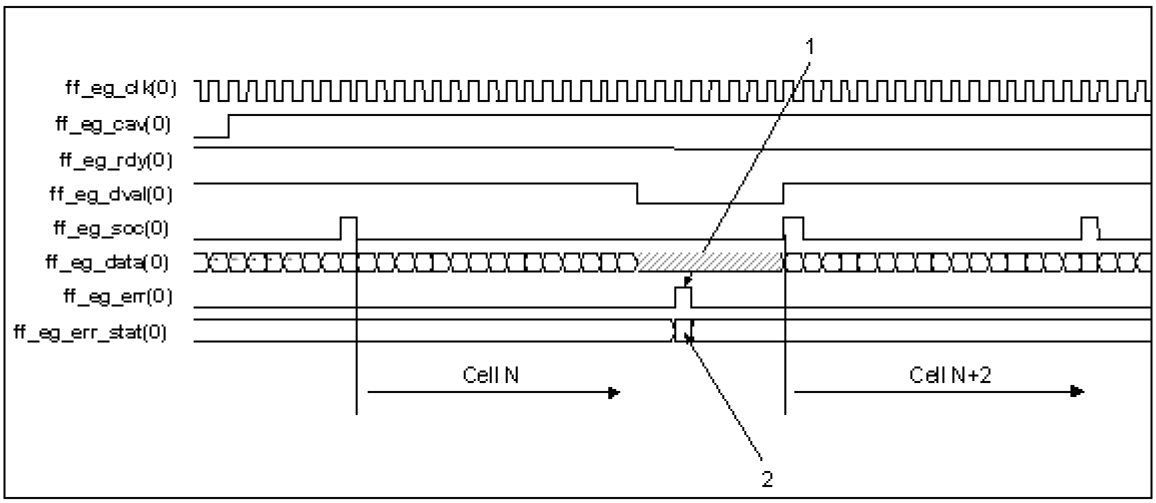

Figure 13: Cell Discard Indication

Table 9: Error Status Word Bit Coding

Error Status Bit	Name	Description
0	PARITY_ERR	Valid when wtx/etx_err is asserted. If set to one indicates that a cell is discarded with a parity error decoded by the Core.
1	LENGTH_ERR	Valid when wtx/etx_err is asserted. If set to one indicates that a cell is discarded with a cell length error detected on the Utopia interface.

The signals are sampled on the corresponding clocks from the west interface:

- erx_... sampled with wrxclk (west receive clock)
- wtx_... sampled with wtxclk (west transmit clock)

9.0 Complexity and Performance Summary

9.1 Timing Parameters Definition

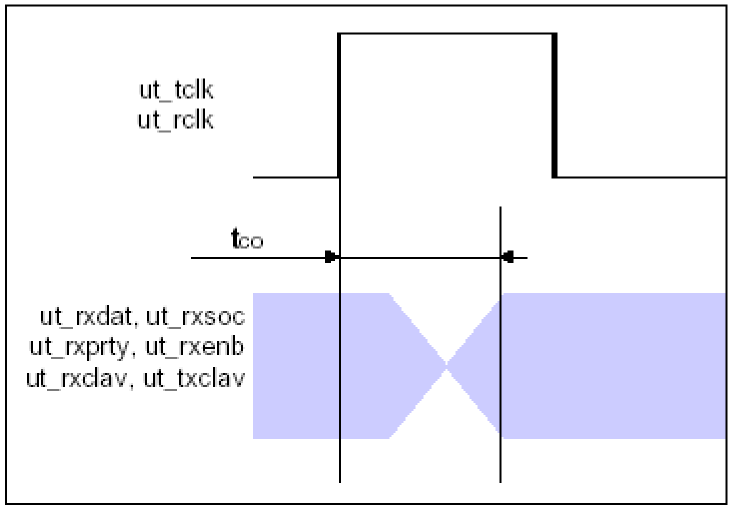

Figure 14: Tco Timing Parameter Definition

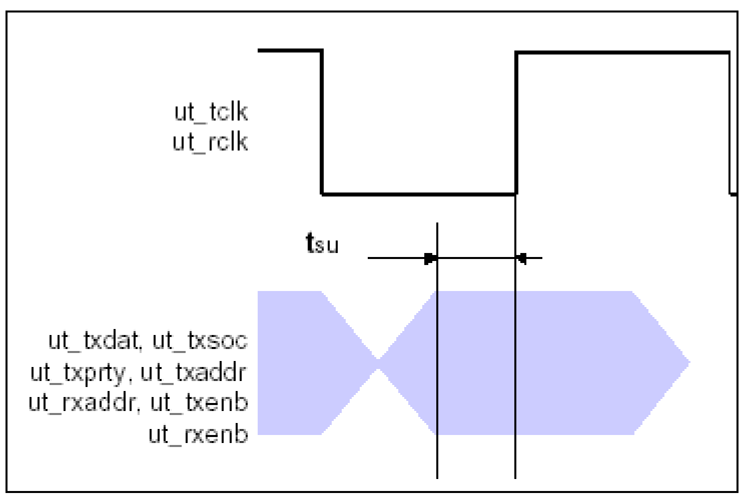

Figure 15: Tsu Timing Parameter Definition

Table 10: 8-Bit Utopia Interface Timing Characteristics

Parameter	typ	Max	Unit
tco	7.5	7.0	ns
tsu	2.5	2.4	ns
wrxclk		70	MHz
wtxclk		76	MHz
erxclk		61	MHz
etxclk		74	MHz
minimum reset time	50		ns

NOTE: *Timing model "worst" case is used.*

10.0 Device Pinout

10.1 Signals Overview

Table 11: Signal Overview Table

Signals	Description
wrxclk, wrxclav, wrxenb*, wrxdat, wrxsoc, wrxaddr	West Utopia L2 Receive Interface.
wtxclk, wtxclav, wtxenb*, wtxdata, wtxsoc, wtxaddr	West Utopia L2 Transmit Interface.
wtx_err, wtx_err_stat	West Interface error indication (sampled with wtxclk).
erxclk, erxclav, erxenb*, erxdata, erxsoc	East Utopia L1 Receive Interface.
etxclk, etxclav, etxenb*, etxdata, etxsoc	East Utopia L1 Transmit Interface.
erx_err, erx_err_stat	East Interface error indication (sampled with wrxclk).
prty_en, cellsize, waddr	Configuration Pins to be board wired.Usual values for waddr are between 0 and 3.
reset	Active high device reset
GND	Ground
VCC	Device Power 2.5 V
clk(x)	unused clock inputs should be tied to GND
IOCTRL(x)	
VCCIO(x)	IO Power 3.0 V
INREF(x)	connect to GND
PLLRST(x)	connect to GND or VCC
PLLOUT(x)	connect to GND or VCC
VCCPLL(x)	
GNDPLL(x)	
TCK, TRSTB	JTAG signals. connect to GND
TMS, TDI	JTAG signals. connect to VCC
TDO	JTAG signal. leave open
iov	
nc	not connected. should be left open

*: active low signal

10.2 PT280 Device Diagram

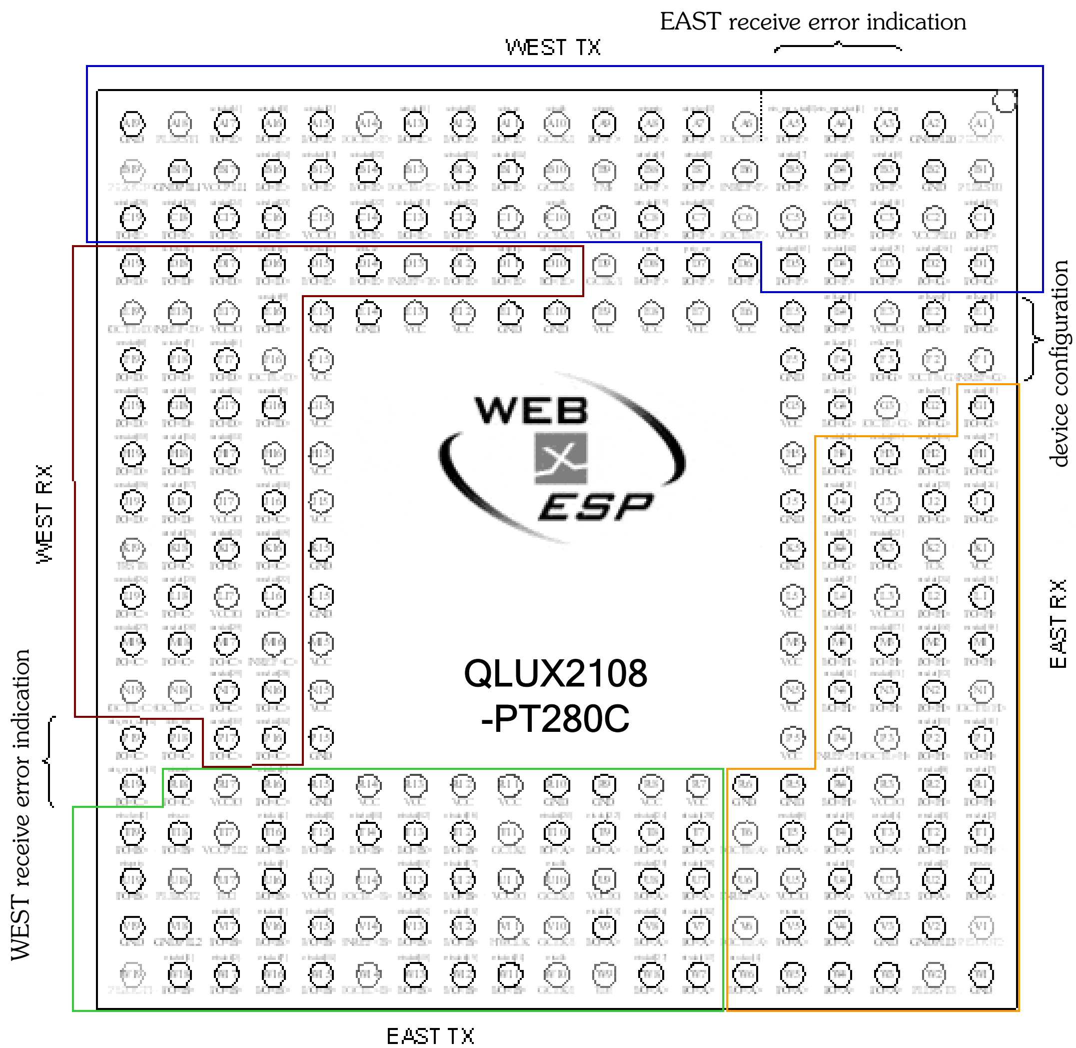

Figure 16: PT280 bottom view

10.3 280 Pin FPBGA Pinout Table

Table 12: 280 Pin FPBGA Pinout Table

PIN	Function	PIN	Function	PIN	Function	PIN	Function	PIN	Function
A1	pllout(3)	D1	nc	G19	nc	N16	nc	U6	inref(a)
A2	gndpll(0)	D2	nc	H1	waddr[3]	N17	nc	U7	nc
A3	erx_err	D3	nc	H2	waddr[2]	N18	ioctrl(c)	U8	nc
A4	erx_err_stat[0]	D4	nc	H3	waddr[1]	N19	ioctrl(c)	U9	vccio(a)
A5	erx_err_stat[1]	D5	nc	H4	waddr[0]	P1	nc	U10	erxclk
A6	ioctrl(f)	D6	cellsize[0]	H5	vcc	P2	nc	U11	vccio(b)
A7	wtxclav[0]	D7	prty_en	H15	vcc	P3	ioctrl(h)	U12	nc
A8	wtxprty	D8	reset	H16	vcc	P4	inref(h)	U13	nc
A9	wtxenb	D9	clk(8)	H17	nc	P5	vcc	U14	ioctrl(b)
A10	wtxclk	D10	wrxclav[0]	H18	nc	P15	gnd	U15	vccio(b)
A11	wtxsoc	D11	wrxprty	H19	nc	P16	nc	U16	etxdat[5]
A12	wtxdat[0]	D12	wrxenb	J1	nc	P17	nc	U17	tdo
A13	wtxdat[1]	D13	inref(e)	J2	nc	P18	wtx_err	U18	pllrst(2)
A14	ioctrl(e)	D14	wrxsoc	J3	vccio(g)	P19	wtx_err_stat[0]	U19	etxprty
A15	wtxdat[2]	D15	wrxdat[0]	J4	nc	R1	erxdat[7]	V1	pllout(2)
A16	wtxdat[3]	D16	wrxdat[1]	J5	gnd	R2	nc	V2	gndpll(3)
A17	wtxdat[4]	D17	wrxdat[2]	J15	vcc	R3	vccio(h)	V3	gnd
A18	pllrst(1)	D18	wrxdat[3]	J16	nc	R4	nc	V4	erxprty
A19	gnd	D19	wrxdat[4]	J17	vccio(d)	R5	gnd	V5	erxenb
B1	pllrst(0)	E1	cellsize[3]	J18	wrxaddr[4]	R6	gnd	V6	ioctrl(a)
B2	gnd	E2	cellsize[2]	J19	wrxaddr[3]	R7	vcc	V7	nc
B3	wtxdat[5]	E3	vccio(g)	K1	vcc	R8	vcc	V8	nc
B4	wtxdat[6]	E4	cellsize[1]	K2	tck	R9	gnd	V9	nc
B5	wtxdat[7]	E5	gnd	K3	nc	R10	gnd	V10	clk(1)
B6	inref(f)	E6	vcc	K4	nc	R11	vcc	V11	clk(4)
B7	nc	E7	vcc	K5	gnd	R12	vcc	V12	nc
B8	nc	E8	vcc	K15	gnd	R13	vcc	V13	nc
B9	tms	E9	vcc	K16	wrxaddr[2]	R14	vcc	V14	inref(b)
B10	clk(6)	E10	gnd	K17	wrxaddr[1]	R15	gnd	V15	nc
B11	nc	E11	gnd	K18	wrxaddr[0]	R16	etxdat[3]	V16	etxdat[6]
B12	nc	E12	vcc	K19	trstb	R17	vccio(c)	V17	etxdat[1]
B13	ioctrl(e)	E13	vcc	L1	nc	R18	etxenb	V18	gndpll(2)
B14	nc	E14	gnd	L2	nc	R19	wtx_err_stat[1]	V19	gnd
B15	nc	E15	gnd	L3	vccio(h)	T1	erxdat[2]	W1	gnd
B16	nc	E16	wrxdat[5]	L4	nc	T2	erxdat[3]	W2	pllrst(3)
B17	vccpll(1)	E17	vccio(d)	L5	vcc	T3	erxdat[4]	W3	nc
B18	gndpll(1)	E18	inref(d)	L15	gnd	T4	erxdat[5]	W4	nc
B19	pllout(0)	E19	ioctrl(d)	L16	nc	T5	erxdat[6]	W5	nc
C1	nc	F1	inref(g)	L17	vccio(c)	T6	ioctrl(a)	W6	erxclav[0]
C2	vccpll(0)	F2	ioctrl(g)	L18	nc	T7	nc	W7	nc
C3	nc	F3	cellsize[5]	L19	nc	T8	nc	W8	nc
C4	nc	F4	cellsize[4]	M1	nc	T9	nc	W9	tdi
C5	vccio(f)	F5	gnd	M2	nc	T10	nc	W10	etxclk
C6	ioctrl(f)	F15	vcc	M3	nc	T11	clk(3)	W11	nc
C7	nc	F16	ioctrl(d)	M4	nc	T12	nc	W12	nc
C8	nc	F17	wrxdat[6]	M5	vcc	T13	nc	W13	nc
C9	vccio(f)	F18	wrxdat[7]	M15	vcc	T14	nc	W14	ioctrl(b)
C10	wrxclk	F19	nc	M16	inref(c)	T15	nc	W15	nc
C11	vccio(e)	G1	waddr[4]	M17	nc	T16	etxdat[4]	W16	etxdat[7]
C12	nc	G2	cellsize[7]	M18	nc	T17	vccpll(2)	W17	etxdat[2]
C13	nc	G3	ioctrl(g)	M19	nc	T18	etxsoc	W18	etxdat[0]
C14	wtxaddr[4]	G4	cellsize[6]	N1	ioctrl(h)	T19	etxclav[0]	W19	pllout(1)
C15	vccio(e)	G5	vcc	N2	nc	U1	erxsoc		
C16	wtxaddr[3]	G15	vcc	N3	nc	U2	erxdat[0]		
C17	wtxaddr[2]	G16	nc	N4	nc	U3	vccpll(3)		
C18	wtxaddr[1]	G17	nc	N5	vcc	U4	erxdat[1]		
C19	wtxaddr[0]	G18	nc	N15	vcc	U5	vccio(a)		

11.0 References

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12.0 Contact

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