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1 OF

12

1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents one product assurance class, class H (high reliability) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN).
 - 1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	<u>Circuit function</u>
01	42106, PA51M/883	High power operational amplifier
02	42106-1, PA51M/883	High power operational amplifier

1.2.2 <u>Case outline(s)</u>. The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	Package style
Χ	See figure 1	8	Flange mount
Υ	See figure 1	8	Flange mount

- 1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.
- 1.3 Absolute maximum ratings.

Supply voltage range Differential input voltage Common mode input	\pm 40 V dc maximum \pm VCC - 3 V \pm VCC
Maximum power dissipation (PD):	
Device type 01	80 W <u>1</u> / 97 W <u>2</u> /
Device type 01 Device type 02 Junction temperature (T _J) Lead temperature (soldering, 10 seconds) Storage temperature range	2.2°C/W 1.8°C/W +200°C +300°C -65°C to +150°C
1.4 Recommended operating conditions.	
Supply voltage (±VCC) Operating temperature range:	±34 V dc
Device type 01 (T _A)	-55°C to +125°C
Device type 02 (T _C)	-55°C to +125°C

^{1/} At ambient temperature of +25°C, derate at 2.2°C/W above ambient temperature of +25°C.

^{2/} At case temperature of +25°C, derate at 1.8°C/W above case temperature of +25°C.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 2

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-973 - Configuration Management.

MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item performance requirements for device class H shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for applicable device class. Therefore, the tests and inspections herein may not be performed for applicable device class (see MIL-PRF-38534). Furthermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. The modification in the QM plan shall not affect the form, fit, or function as described herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and on figure 1.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 2.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 3

- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Marking of device(s)</u>. Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in MIL-HDBK-103 and QML-38534.
- 3.6 <u>Data</u>. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.
- 3.7 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.
- 3.8 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
 - 4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ} C$ minimum for device type 01 and $T_C = +125^{\circ} C$, minimum for device type 02.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 4

	7	FABLE I. Electrical performance of	characteristics.				
Test	Symbol	Conditions $-55^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq +125^{\circ}\text{C}$	Group A subgroups	Device type	Limits		Unit
		$\pm V_{CC} = \pm 34 \text{ V dc}$ unless otherwise specified	Subgroups	туре	Min	Max	
Input offset voltage	V _{IO}	T _A = +25°C	1	01	-5	+5	mV
Input offset voltage drift	DVIO	T _A = -55°C and +125°C	2, 3	01	-40	+40	μV/°C
Input bias current	I _{IB}		1	01	-20	+20	nA
			2, 3		-35	+35	
Input offset current	I _{IO}		1	01	-3	+3	nA
			2, 3		-7	+7	
Power supply rejection ratio	+PSRR	-V _{CC} = -34 V dc,	1	01	-100	+100	μV/V
		+V _{CC} = +10 V to +40 V dc	2, 3		-200	+200	
	-PSRR	+V _{CC} = +34 V dc,	1		-100	+100	
		-V _{CC} = -10 V to -40 V dc	2, 3		-200	+200	
Common mode rejection ratio	CMRR	V _{CM} = ±22 V, f = dc	1	01	80		dB
Tallo			2, 3		76		
Supply current	ICC	V _{CM} = 0 V, no load Condition	1, 2, 3	01	-10	+10	mA
Output voltage peak	VOP	I _O = 10 A peak	4	01		-26	V
		I _O = 10 A peak	4		26		
		R _L = 10 kΩ	5, 6			-30	
		R _L = 10 kΩ	5, 6		30		
Output current peak	IOP	$R_L = 2.6 \Omega$, $T_A = +25^{\circ}C$	4	01	10		А
Voltage gain	Avs	R _L = 10 kΩ	4, 5, 6	01	94		dB
Slew rate	SR	$R_L = 6.5 \Omega, T_A = +25^{\circ}C$	4	01	1.35		V/μs

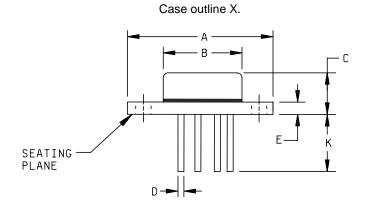
STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 5

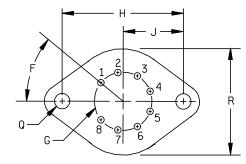
	TA	BLE I. Electrical performa	nce charac	cteristics	<u>s</u> - Con	tinued.			
Test	Symbol	Conditions 1/		Grou		Device	Lir	nits	Unit
		-55°C ≤ T _C ≤ +125 \pm V _{CC} = \pm 34 V do unless otherwise spec	C	subgr	oups	type	Min	Max	
Supply current	IS	V _{IN} = 0 V dc, G = 100,	<u>2</u> /	1,	3	02		10	mA
		$\pm R_{CL} = 0.1 \Omega, V_{CM} = 0.1 \Omega$	√ dc	2)			13	
Input offset voltage	Vos	V _{IN} = 0 V dc, G = 100,	<u>2</u> /	1		02	-16.0	+16.0	mV
		$\pm R_{CL} = 0.1 \Omega$,		2)		-22.5	+22.5	
		±V _{CC} = ±10 V dc		3	3		-21.2	+21.2	
		V _{IN} = 0 V dc, G = 100,	<u>2</u> /	1			-10.0	+10.0	
		$\pm R_{CL} = 0.1 \Omega,$ $\pm V_{CC} = \pm 34 \text{ V dc}$		2	2		-16.5	+16.5	
		± VCC = ±34 V dC		3	3		-15.2	+15.2	
		$V_{IN} = 0 \text{ V dc}, G = 100,$	<u>2</u> /	1			-11.2	+11.2	
		$\pm R_{CL} = 0.1 \Omega,$ $\pm V_{CC} = \pm 40 \text{ V dc}$		2	2		-17.7	+17.7	
		± v C C = ±40 v dc		3	3		-16.7	+16.7	
Input bias current (+IN)	+IS	V _{IN} = 0 V dc,		1		02		40.0	nA
		R _{BIAS} ≤ 100 MΩ		2,	3			80.0	
Input bias current (-IN)	-IS	V _{IN} = 0 V dc,		1		02		40.0	nA
		R _{BIAS} ≤ 100 MΩ		2,	3			80.0	
Input offset current	IOS	$V_{IN} = 0 V dc,$		1		02		10.0	nA
		RBIAS ≤ 100 MΩ		2,	3			30.0	
Output voltage	VO	\pm V _{CC} = ±40 V dc, I _O = 68 mA, R _L = 500 Ω		4, 5	5, 6	02	34		V
		\pm V _{CC} = \pm 34 V dc, I _O = 4 A, R _L = 6 Ω		4, 5	5, 6		24		
		$\pm V_{CC} = \pm 18 \text{ V dc, I}_{O} = 1$ R _L = 1 Ω , T _C = +25°C an		4,	6		10		
		$\pm V_{CC} = \pm 16 \text{ V dc}, I_{O} = 8 \text{ RL} = 1 \Omega, T_{C} = +125^{\circ}\text{C}$	5 A,	5	5		8		
Current limits	ICL	$\pm V_{CC} = \pm 16 \text{ V dc}, \pm R_{CL}$ $R_{L} = 1 \Omega, T_{C} = +25^{\circ}C$		4	ļ.	02	5.0	7.9	A
See footnotes at end of	table.								
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MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000				REVI	SION LEVE B	ĒL	SHEET 6	6	

	TABLE I. <u>Electrical performance characteristics</u> - Continued.						
Test	Symbol	Conditions 1/	Group A	Device	Limits		Unit
		-55° C ≤ T _C ≤ +125°C ±V _{CC} = ±34 V dc unless otherwise specified	subgroups	type	Min	Max	
Current limits	lCL	$\pm V_{CC} = \pm 16 \text{ V dc}, \qquad \underline{2}/$ $\pm R_{CL} = 0.1 \Omega, R_{L} = 1 \Omega,$ $T_{C} = +25^{\circ}C$	4	02	5.0	7.9	A
Stability/noise	E _N	±V _{CC} = ±34 V dc, C _L = 1.5 nF, G = 1	4, 5, 6	02		1.0	mV
Slew rate	SR	\pm V _{CC} = \pm 34 V dc, V _{IN} \geq 4 Vp-p, R _L = 500 Ω	4, 5, 6	02	1.0	10	V/μs
Open loop gain	AOL	\pm V _{CC} = \pm 34 V dc, V _{IN} \geq 4 Vp-p, R _L = 500 Ω , f = 15 Hz	4, 5, 6	02	91		dB
Common mode rejection	CMR	$\pm V_{CC} = \pm 15 \text{ V dc},$ $V_{CM} = \pm 9 \text{ V dc}, +f = dc$	4, 5, 6	02	70		dB

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 7

^{1/2} During all group A testing, terminal connection F. O. (pin 7) is left open. 2/2 A current limiting resistor (R_{CL}) is connected between C_L+ to the output and C_L- to the output during these tests.





BOTTOM VIEW

Symbol	Inches		Millim	neters	
	Min	Max	Min	Max	
Α	1.510	1.550	38.35	39.37	
В	0.745	0.770	18.92	19.56	
С	0.260	0.300	6.60	7.62	
D	0.038	0.042	0.97	1.07	
Е	0.080	0.105	2.03	2.67	
F	40° BSC		40° BSC		
G	0.500	0.500 BSC		12.7 BSC	
Н	1.186 BSC		30.12	BSC	
J	0.593 BSC		15.06	BSC	
K	0.400	0.500	10.16	12.70	
Q	0.151	0.161	3.84	4.09	
R	0.980	1.020	24.89	25.91	

NOTES:

- Leads in true position within 0.010 inch (0.25 mm) R at MMC at seating plane.
 The U. S. preferred system of measurement is the metric SI. This case outline was originally designed using inchpound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound shall take precedence.
- 3. Pin numbers are for reference and may not be marked on package.

FIGURE 1. Case outline(s).

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 8

Case outline Y. SEATING PLANE

Symbol	Inches		Millim	eters
-	Min	Max	Min	Max
А	1.510	1.550	38.35	39.37
В	0.745	0.770	18.92	19.56
С	0.225	0.250	5.71	6.35
D	0.038	0.042	0.97	1.07
Е	0.080	0.105	2.03	2.67
F	40° BSC		40° BSC	
G	0.500 BSC		12.7 BSC	
Н	1.186	1.186 BSC		BSC
J	0.593 BSC		15.06	BSC
K	0.400	0.500	10.16	12.70
Q	0.151	0.161	3.84	4.09
R	0.980	1.020	24.89	25.91

BOTTOM VIEW

NOTES:

- Leads in true position within 0.010 inch (0.25 mm) R at MMC at seating plane.
 The U. S. preferred system of measurement is the metric SI. This case outline was originally designed using inchpound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound shall take precedence.
- 3. Pin numbers are for reference and may not be marked on package.

FIGURE 1. Case outline(s) - Continued.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		B	9

Device type	01and 02
Case outline	X and Y
Terminal number	Terminal symbol
1	Output
2	+Current limit (C _L +)
3	+VCC
4	+IN
5	-IN
6	-Vcc
7	No connection
8	-Current limit (C _L -)

FIGURE 2. <u>Terminal connections.</u>

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		B	10

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1
Final electrical parameters	1*, 2, 3, 4, 5, 6
Group A test requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1

^{*} PDA applies to subgroup 1.

- 4.3 <u>Conformance and periodic inspections</u>. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.
 - 4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 7, 8, 9, 10, and 11 shall be omitted.
 - 4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.
 - 4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - (2) $T_A = +125^{\circ} C$ minimum for device type 01 and $T_C = +125^{\circ} C$, minimum for device type 02.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
 - 4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.
 - 5. PACKAGING
 - 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		B	11

6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.
- 6.6 <u>Sources of supply</u>. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-87620
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL B	SHEET 12

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-01-11

Approved sources of supply for SMD 5962-87620 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38534 during the next revision. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38534.

Standard	Vendor	Vendor
microcircuit drawing	CAGE	similar
PIN <u>1</u> /	number	PIN <u>2</u> /
5962-8762001XA	31757	42106
5962-8762001XC	31757	42106
5962-8762001YA	60024	PA51M/883
5962-8762002XA	31757	42106-1
5962-8762002XC	31757	42106-1
5962-8762002YA	60024	PA51M/883

- 1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number_	Vendor name and address
31757	Micropac Industries, Incorporated 905 E. Walnut Street Garland, TX 75040 Point of contact: 912 E. Walnut Street Garland, TX 75040
60024	Apex Microtechnology Corporation 5980 N. Shannon Road Tucson, AZ 85741

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.