REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Technical changes to table I. Device types 01TX and 02TX not available from an approved source.	1990 SEPT 24	Weckman

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV	A	A																						
SHEET	22	23																						

REV STATUS OF SHEETS																						
REV	A	A	A	A	A		A				A		A									A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Jeffery Sunstrom

CHECKED BY: William K. Heckman

APPROVED BY: William K. Heckman

DRAWING APPROVAL DATE: 1 SEPTEMBER 1988

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL,CMOS, 16-BIT ERROR DETECTION AND CORRECTION UNIT, MONOLITHIC SILICON.

SIZE	CAGE CODE	
A	14933	5962-88613

SHEET 1

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1748

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-88613	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Detect time	Correct time
01	39C60A	16-bit EDCU	24 ns	35 ns
02	39C60	16-bit EDCU	36 ns	73 ns
03	29C60A	16-bit EDCU	24 ns	35 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
T	See figure 1 (48-lead, 1.730" x .410" x .190"), dual-in-line package
U	C-6 (52 terminal, .761" x .761" x .120"), square chip carrier package
X	D-14 (48-lead, 2.435" x .620" x .225"), dual-in-line package
Y	See figure 1 (48-lead, 1.235" x .660" x .060"), flat package
Z	See figure 1 (52 terminal, .761" x .761" x .075"), square chip carrier package

1.3 Absolute maximum ratings.

Voltage on any pin relative to ground	-0.5 V dc to +7.0 V dc
DC output current into outputs	30 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.0 W 1/
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases T, Y, Z	30 °C/W 2/
Cases X and U	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc to 5.5 V dc
Minimum input high voltage (V_{IH})	2.0 V dc
Maximum input low voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2/ When a thermal resistance value is included in MIL-M-38510, appendix C, it shall supersede the value herein.

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Block diagram. The block diagram shall be as specified on figure 3.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/		Group A subgroups	Device types	Limits		Unit
						Min	Max	
Input high voltage	V_{IH}	Guaranteed input logical high voltage for all inputs 2/		1, 2, 3	All	2.0		V
Input low voltage	V_{IL}	Guaranteed input logical low voltage for all inputs 2/		1, 2, 3	All		0.8	V
Input high current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1, 2, 3	All		5.0	µA
Input low current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		1, 2, 3	All		-5.0	µA
Output high voltage	V_{OH}	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300 µA	1, 2, 3	All	V_{CC}-0.2 V		V
			I_{OH} = -6 mA	1, 2, 3	01, 02	2.4		V
			I_{OH} = -12 mA		03			
Output low voltage	V_{OL}	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300 µA	1, 2, 3	All		0.2	V
			I_{OL} = 8 mA	1, 2, 3	All		0.5	V
Off state high impedance output current	I_{OZ}	V_{CC} = 5.5 V	V_O = 0 V	1, 2, 3	All		-10	µA
			V_O = 5.5 V	1, 2, 3	All		10	µA
Output short circuit current 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V		1, 2, 3	01, 02	-20		mA
					03	-30		
Quiescent power supply current (CMOS inputs)	I_{CCQ}	V_{CC} = 5.5 V, $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$, f_{OP} = 0		1, 2, 3	All		5.0	mA
Quiescent input power supply current (per input at TTL high) 4/	I_{CCT}	V_{CC} = 5.5 V, V_{IN} = 3.4 V, f_{OP} = 0		1, 2, 3	All		0.5	mA/ input

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/		Group A subgroups	Device types	Limits Min	Limits Max	Unit
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$, outputs open, $\overline{OE}$ = low		1, 2, 3	All		8.5	mA/ MHz
Total power supply current 5/	I_{CC}	V_{CC} = 5.5 V, f_{OP} = 10 MHz, outputs open, $\overline{OE}$ = low, 50% duty cycle	$V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	1, 2, 3	All		90	mA
			V_{IH} = 3.4 V, V_{IL} = 0.4 V	1, 2, 3	All		100	mA
Input capacitance	C_{IN}	See 4.3.1c		4	All		12	pF
Output capacitance	C_{OUT}						15	pF
I/O capacitance	$C_{I/O}$						15	pF
Functional testing		See 4.3.1d		7, 8	All			
Combinational delay, 1-4 Input: $DATA_{0-15}$ Output:		C_L = 50 pF, see figure 4		9,10,11				
SC_{0-6}	t_{PD1}				01, 03		22	ns
					02		35	ns
$DATA_{0-15}$ 7/	t_{PD2}				01, 03		35	ns
					02		73	ns
$\overline{ERROR}$	t_{PD3}				01, 03		24	ns
					02		36	ns
$\overline{MULT\ ERROR}$	t_{PD4}				01, 03		27	ns
					02		56	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Combinational delay, 5-8 Input: CB_{0-6} (CODE ID 000,011) Output:		C_L = 50 pF, see figure 4	9,10,11				
SC_{0-6} 8/	t_{PD5}			01, 03		17	ns
				02		30	ns
$DATA_{0-15}$	t_{PD6}			01, 03		28	ns
				02		61	ns
$\overline{ERROR}$	t_{PD7}			01, 03		24	ns
				02		31	ns
$\overline{MULT\ ERROR}$	t_{PD8}			01, 03		27	ns
				02		50	ns
Combination delay, 9-12 Input: CB_{0-6} (CODE ID_{2-0} 010,100,101,110,111) Output:		C_L = 50 pF, see figure 4	9,10,11				
SC_{0-6} 8/	t_{PD9}			01, 03		19	ns
				02		30	
$DATA_{0-15}$	t_{PD10}			01, 03		28	ns
				02		50	
$\overline{ERROR}$	t_{PD11}			01, 03		24	ns
				02		31	
$\overline{MULT\ ERROR}$	t_{PD12}			01, 03		27	ns
				02		37	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combination delay, 13-16 Input: GENERATE		C_L = 50 pF, see figure 4	9,10,11				
Output:							
SC_{0-6} 8/	t_{PD13}			01, 03		20	ns
				02		38	
$DATA_{0-15}$ 7/	t_{PD14}			01, 03		28	ns
				02		69	
$\overline{ERROR}$ 8/	t_{PD15}			01		18	ns
				02		41	ns
				03		21	ns
$\overline{MULT\ ERROR}$	t_{PD16}			01		21	ns
				02		62	ns
				03		25	ns
Combinational delay, 17 Input: CORRECT (not internal control mode)		C_L = 50 pF, see figure 4	9,10,11				
Output:							
$DATA_{0-15}$	t_{PD17}			01, 03		25	ns
				02		49	
Combinational delay, 18-21 Input: DIAG MODE (not internal control mode)		C_L = 50 pF, see figure 4	9,10,11				
Output:							
SC_{0-6} 8/	t_{PD18}			01, 03		25	ns
				02		58	
$DATA_{0-15}$ 7/	t_{PD19}			01, 03		28	ns
				02		89	
$\overline{ERROR}$ 8/	t_{PD20}			01, 03		21	ns
				02		65	
$\overline{MULT\ ERROR}$ 8/	t_{PD21}			01, 03		24	ns
				02		90	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combination delay, 22-25 Input: PASSTHRU (not internal control mode)		C_L = 50 pF, see figure 4	9,10,11				
Output:							
SC_{0-6}	t_{PD22}			01, 03		25	ns
				02		39	
$DATA_{0-15}$	t_{PD23}			01, 03		28	ns
				02		51	
$\overline{ERROR}$	t_{PD24}			01, 03		21	ns
				02		34	
$\overline{MULT\ ERROR}$	t_{PD25}			01, 03		24	ns
				02		54	
Combinational delay,26-29 Input: $CODE\ ID_{2-0}$		C_L = 50 pF, see figure 4	9,10,11				
Output:							
SC_{0-6}	t_{PD26}			01, 03		26	ns
				02		69	
$DATA_{0-15}$	t_{PD27}			01, 03		31	ns
				02		100	
$\overline{ERROR}$	t_{PD28}			01, 03		28	ns
				02		68	
$\overline{MULT\ ERROR}$	t_{PD29}			01, 03		31	ns
				02		90	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combinational delay,30-33 Input: LE_{IN} from latched to transparent) Output:		C_L = 50 pF, see figure 4	9,10,11				
SC_{0-6}	t_{PD30}			01, 03		24	ns
				02		44	
$DATA_{0-15}$ 7/	t_{PD31}			01, 03		37	ns
				02		82	
$\overline{ERROR}$ 8/	t_{PD32}			01, 03		26	ns
				02		43	
$\overline{MULT\ ERROR}$	t_{PD33}			01, 03		29	ns
				02		66	
Combinational delay, 34 Input: LE_{OUT} from latched to transparent) Output: $DATA_{0-15}$ 8/	t_{PD34}	C_L = 50 pF, see figure 4	9,10,11	01, 03		16	ns
				02		33	
Combinational delay,35-38 Input: LE_{DIAG} (from latched to transparent; not internal control mode) Output:		C_L = 50 pF, see figure 4	9,10,11				
SC_{0-6} 7/	t_{PD35}			01, 03		24	ns
				02		50	
$DATA_{0-15}$ 7/	t_{PD36}			01, 03		37	ns
				02		88	
$\overline{ERROR}$ 7/	t_{PD37}			01, 03		26	ns
				02		49	
$\overline{MULT\ ERROR}$ 7/	t_{PD38}			01, 03		29	ns
				02		72	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 4.5\ V$ to $5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Combinational delay,39-42 Input: Internal control mode, LE_{DIA} (from latched to transparent)		C_L = 50 pF, see figure 4	9,10,11				
Output:							
SC_{0-6}	t_{PD39}			01, 03		30	ns
				02		75	
$DATA_{0-15}$ 7/	t_{PD40}			01, 03		43	ns
				02		106	
$\overline{ERROR}$ 7/	t_{PD41}			01, 03		32	ns
				02		74	
$\overline{MULT\ ERROR}$ 7/	t_{PD42}			01, 03		35	ns
				02		96	
Combinational delay,43-46 Input: Internal control mode, $DATA_{0-15}$ (via diagnostic latch)		C_L = 50 pF, see figure 4	9,10,11				
Output:							
SC_{0-6}	t_{PD43}			01, 03		30	ns
				02		75	
$DATA_{0-15}$ 7/	t_{PD44}			01, 03		43	ns
				02		106	
$\overline{ERROR}$ 7/	t_{PD45}			01, 03		32	ns
				02		74	
$\overline{MULT\ ERROR}$ 7/	t_{PD46}			01, 03		35	ns
				02		96	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Setup time 1 8/ Hold time 1 Input: $DATA_{0-15}$ To: LE_{IN}	t_{s1}	Setup and hold times relative to latch enables See figure 5	9,10,11	01, 03 02	5.0 7.0		ns
	t_{h1}			01, 03 02	3.0 7.0		ns
Setup time 2 8/ Hold time 2 Input: CB_{0-6} To: LE_{IN}	t_{s2}		9,10,11	All	5.0		ns
	t_{h2}			01, 03 02	3.0 7.0		ns
Setup time 3 8/ Hold time 3 Input: $DATA_{0-15}$ To: LE_{OUT}	t_{s3}		9,10,11	01, 03 02	27 50		ns
	t_{h3}			01, 03 02	2.0 5.0		ns
Setup time 4 8/ Hold time 4 Input: CB_{0-6} (CODE ID 000,011) To: LE_{OUT}	t_{s4}		9,10,11	01, 03 02	24 28		ns
	t_{h4}			All	0		ns
Setup time 5 8/ Hold time 5 Input: CB_{0-6} (CODE ID 010, 100,101,110, 111) To: LE_{OUT}	t_{s5}		9,10,11	01, 03 02	24 30		ns
	t_{h5}			All	0		ns
Setup time 6 7/ 8/ Hold time 6 Input: $\overline{GENERATE}$ To: LE_{OUT}	t_{s6}		9,10,11	01, 03 02	29 46		ns
	t_{h6}			All	0		ns
Setup time 7 8/ Hold time 7 Input: CORRECT To: LE_{OUT}	t_{s7}		9,10,11	01, 03 02	25 28		ns
	t_{h7}			01, 03 02	0 1.0		ns

See footnotes at end of page.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Setup time 8 8/	t_{s8}	Setup and hold times relative to latch enables See figure 5	9,10,11	01, 03	25		ns
Hold time 8				02	84		
Input: DIAG MODE To: LE_{OUT}	t_{h8}			All	0		ns
Setup time 9 8/	t_{s9}		9,10,11	01, 03	25		ns
Hold time 9				02	30		
Input: PASSTHRU To: LE_{OUT}	t_{h9}			All	0		ns
Setup time 10 8/	t_{s10}		9,10,11	01, 03	28		ns
Hold time 10				02	89		
Input: CODE ID_{2-0} To: LE_{OUT}	t_{h10}			All	0		ns
Setup time 11 7/ 8/	t_{s11}		9,10,11	01, 03	30		ns
Hold time 11				02	59		
Input: LE_{IN} To: LE_{OUT}	t_{h11}			01, 03	0		ns
				02	5.0		
Setup time 12 8/	t_{s12}		9,10,11	01, 03	5.0		ns
Hold time 12				02	7.0		
Input: $DATA_{0-15}$ To: LE_{DIAG}	t_{h12}			01, 03	3.0		ns
				02	9.0		
Enable time 1 8/	t_{en1}	C_L = 5.0 pF 4/ See figure 4	9,10,11	01, 03		28	ns
Disable time 1				02		35	
From: $\overline{OE}$ $BYTE_{0-1}$ To: $DATA_{0-15}$	t_{dis1}			01, 03		25	ns
				02		35	
Enable time 2 8/	t_{en2}		9,10,11	01, 03		28	ns
Disable time 2				02		35	
From: $\overline{OESC}$ To: SC_{0-6}	t_{dis2}			01, 03		25	ns
				02		35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 4.5 V to 5.5 V unless otherwise specified 1/	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Minimum pulse widths; LE_{IN}, LE_{OUT}, LE_{DIAG}	t_{pw}		9,10,11	01,03	12		ns
				02	15		ns

1/ $V_{HC} = V_{CC}-0.2$ V and $V_{LC} = 0.2$ V, unless otherwise specified.

2/ These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

3/ Not more than one output should be shorted at a time. Duration of short circuit test should not exceed 1 second.

4/ I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4 V, subtracting out I_{CCQ}, then dividing by the total number of inputs.

5/ Total supply current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the total supply current can be calculated by using the following equation:

$$I_{CC} = I_{CCQ} + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{OP}), \text{ where;}$$

D_H = Data duty cycle TTL high period (V_{IN} = 3.4 V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{OP} = Operating frequency in megahertz.

6/ Output disable tests are performed with C_L = 5.0 pF and are measured to 0.5 V change of output voltage level.

7/ This test is calculated from other measured parameters, not performed in production testing for device type 03.

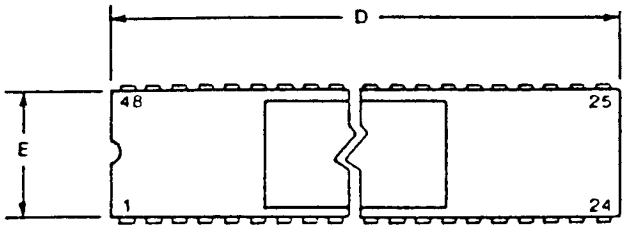
8/ Guaranteed to the limit specified herein by characterization data for device type 03.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

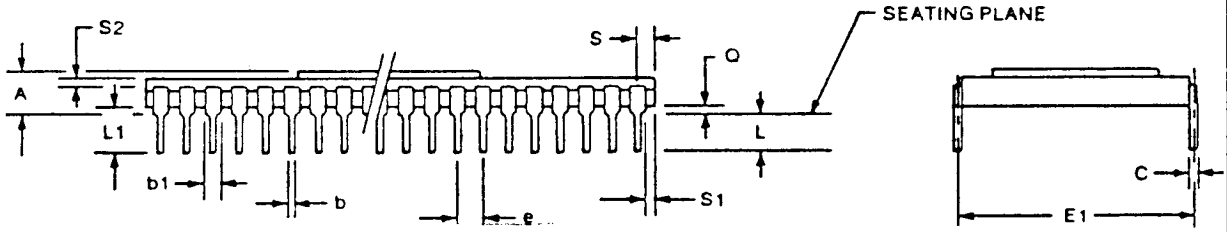
3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.



Case outline T



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.085	.190	2.16	4.83
b	.014	.023	0.36	0.58
b1	.030	.060	0.76	1.52
C	.008	.014	0.20	0.36
D	1.690	1.730	42.93	43.94
E	.380	.410	9.65	10.41
E1	.390	.420	9.91	10.67

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
e	.070 BSC		1.78 BSC	
L	.125	.200	3.18	5.08
L1	.150		3.81	
Q	.020	.070	0.51	1.78
S	.030	.065	0.76	1.65
S1	.005		0.13	
S2	.005		0.13	

NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.

FIGURE 1. Dimensions and configurations.

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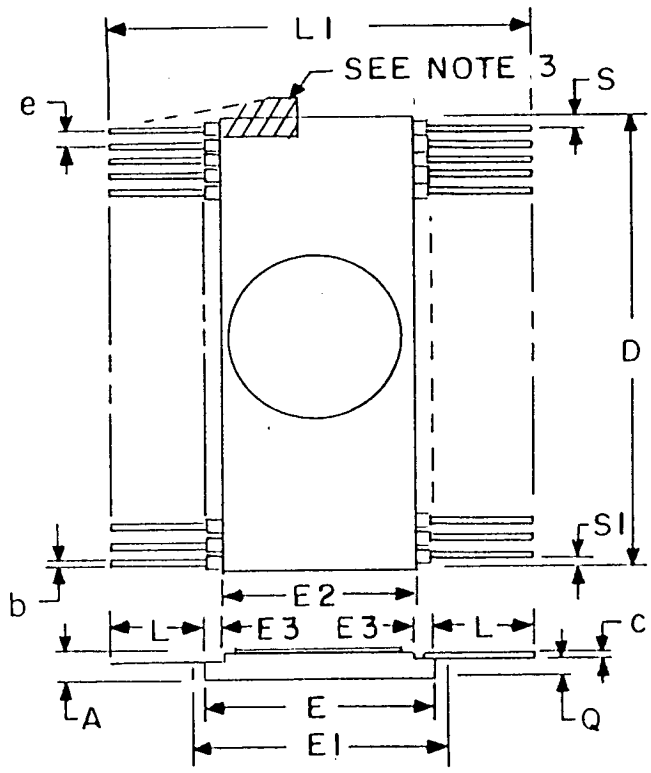
Case outline Y

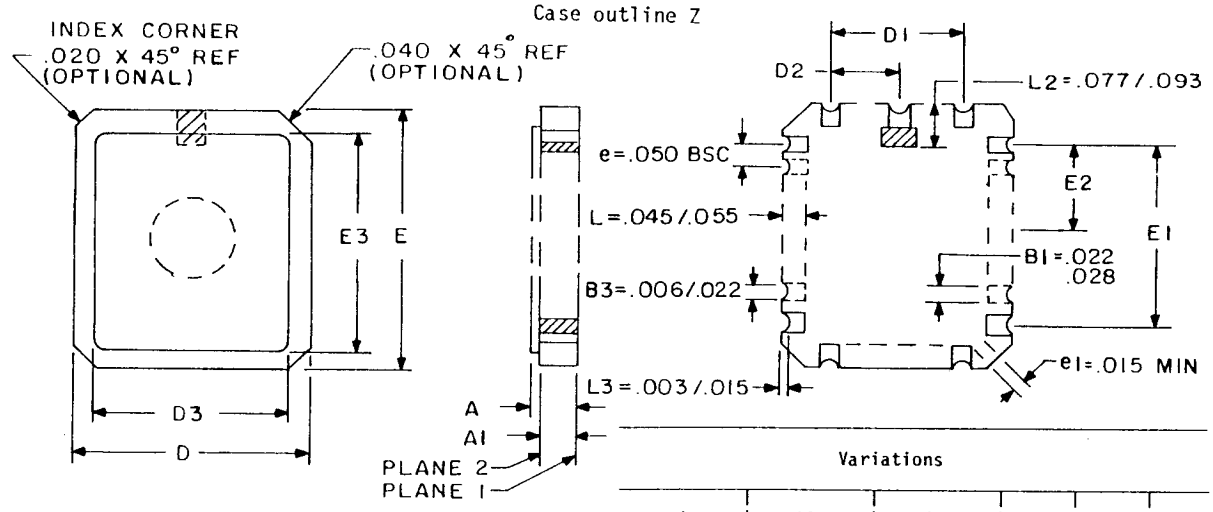
Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	.070	.098	1.78	2.49
b	.017	.023	0.43	0.58
c	.008	.012	0.20	0.30
D	1.185	1.235	30.10	31.37
E	.620	.660	15.75	16.76
E1	---	.720	---	18.29
E2	.520	---	13.21	---
E3	.030	---	0.76	---
e	.045	.055	1.14	1.40
L	.250	.370	6.35	9.40
L1	1.140	1.380	28.96	35.05
Q	.030	.060	0.76	1.52
S	---	.045	---	1.14
S1	.005	---	0.13	---

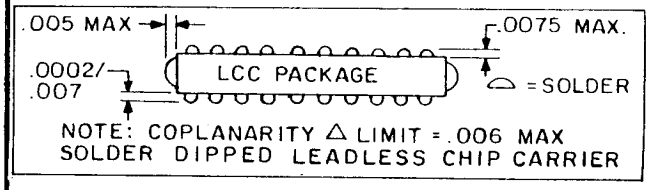


NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for general information only.
3. Index area: A notch, tab, or pin one identification mark shall be located within the shaded area shown.
4. E1 allows for Ag-Cu alloy brazed overrun.
5. Dimensions b and c increase by 3 mils maximum limit if tinplate or solder dip lead finish, or both is applied.

FIGURE 1. Dimensions and configurations - Continued.

Case outline Z





Variations

A		A1		D/E		D1/E1	D3/E3	ND/NE
Min	Max	Min	Max	Min	Max	BSC	Max	
.064	.075	.054	.065	.740	.760	.600	.660	13

NOTES:

1. Dimensions are in inches
2. Metric equivalents are given for general information only.
3. A minimum clearance of .015 inch (0.38 mm) shall be maintained between all metallized features. Corner terminal pads may have A .020 inch (0.51 mm) x 45° maximum chamfer to accomplish e_1 dimension.
4. The lid shall not extend beyond the edges of the body.
5. N is the maximum quantity of terminal positions. ND and NE are the number of terminals along the sides of length D and E, respectively.
6. Electrical connection terminals are required on plane 1 and optional on plane 2. However if plane 2 has such terminals they shall be electrically connected to opposing terminals on plane 1.
7. The index feature for pin 1, identification, optical orientation or handling purposes shall be within the shaded areas shown, and is defined by dimensions B1 and L2.
8. Plane 1 is the heat radiating surface which may optionally be metallized with checker board pattern of thermal conduction pads; the number of pads is determined in accordance with 8 of MIL-M-38510, appendix C for LCC outlines.
9. The chip carrier corner shape (square, notch, radius, etc.) may vary at the manufacturers option from that shown in the detailed drawing.
10. Dimensions B3 and L3 define the castellation width and depth respectively at any point of the surface. Castellations are required on bottom two layers and optional in the top layer. See 50.6 of MIL-M-38510, appendix C for details.
11. Package shall consists of a minimum of two layers.
12. Solderdipped LCC packages shall conform to 40.2.3 of MIL-M-38510, appendix C on coplanarity measurements.

Inches	mm
.0002	0.005
.0075	0.190
.003	0.08
.005	0.13
.006	0.15
.007	0.18
.015	0.38
.020	0.51
.022	0.56
.028	0.71
.040	1.02
.045	1.14
.050	1.27
.054	1.37
.055	1.40
.064	1.63
.065	1.65
.075	1.90
.077	1.96
.093	2.36
.600	15.24
.660	16.76
.740	18.80
.760	19.30

FIGURE 1. Dimensions and configurations - Continued.

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Device type	All		Device type	All	
Package	T, X, and Y	U and Z	Package	T, X, and Y	U and Z
Pin number	Connection	Connection	Pin number	Connection	Connection
1	CORRECT	CORRECT	27	SC_2	SC_6
2	$DATA_{15}$	$DATA_{15}$	28	SC_3	SC_4
3	$DATA_{14}$	$DATA_{14}$	29	SC_5	SC_2
4	$DATA_{13}$	$DATA_{13}$	30	SC_0	SC_3
5	$DATA_{12}$	$DATA_{12}$	31	$\overline{OE}_{SC}$	SC_5
6	LE_{IN}	LE_{IN}	32	$\overline{ERROR}$	SC_0
7	LE_{DIAG}	NC 1/	33	$\overline{MULT\ ERROR}$	NC 1/
8	$\overline{OE}$ $BYTE_1$	LE_{DIAG}	34	CB_1	$\overline{OE}_{SC}$
9	$DATA_{11}$	$\overline{OE}$ $BYTE_1$	35	CB_2	ERROR
10	$DATA_{10}$	$DATA_{11}$	36	V_{CC}	$\overline{MULT\ ERROR}$
11	$DATA_9$	$DATA_{10}$	37	CB_3	CB_1
12	$DATA_8$	$DATA_9$	38	CB_4	CB_2
13	GND	$DATA_8$	39	CB_5	V_{CC}
14	$DATA_7$	GND	40	CB_0	CB_3
15	$DATA_6$	$DATA_7$	41	CB_6	CB_4
16	$DATA_5$	$DATA_6$	42	$\overline{GENERATE}$	CB_5
17	$DATA_4$	$DATA_5$	43	$CODE\ ID_0$	CB_0
18	$\overline{OE}$ $BYTE_0$	$DATA_4$	44	$CODE\ ID_1$	CB_6
19	LE_{OUT}	$\overline{OE}$ $BYTE_0$	45	$CODE\ ID_2$	$\overline{GENERATE}$
20	$DATA_3$	NC	46	$DIAG\ MODE_0$	NC 1/
21	$DATA_2$	LE_{OUT}	47	$DIAG\ MODE_1$	$CODE\ ID_0$
22	$DATA_1$	$DATA_3$	48	PASS THRU	$CODE\ ID_1$
23	$DATA_0$	$DATA_2$	49	---	$CODE\ ID_2$
24	SC_1	$DATA_1$	50	---	$DIAG\ MODE_0$
25	SC_6	$DATA_0$	51	---	$DIAG\ MODE_1$
26	SC_4	SC_1	52	---	PASSTHRU

1/ For device type 03, packages U and Z, pins 7, 20, 33 and 46 are ground.

FIGURE 2. Terminal connections.

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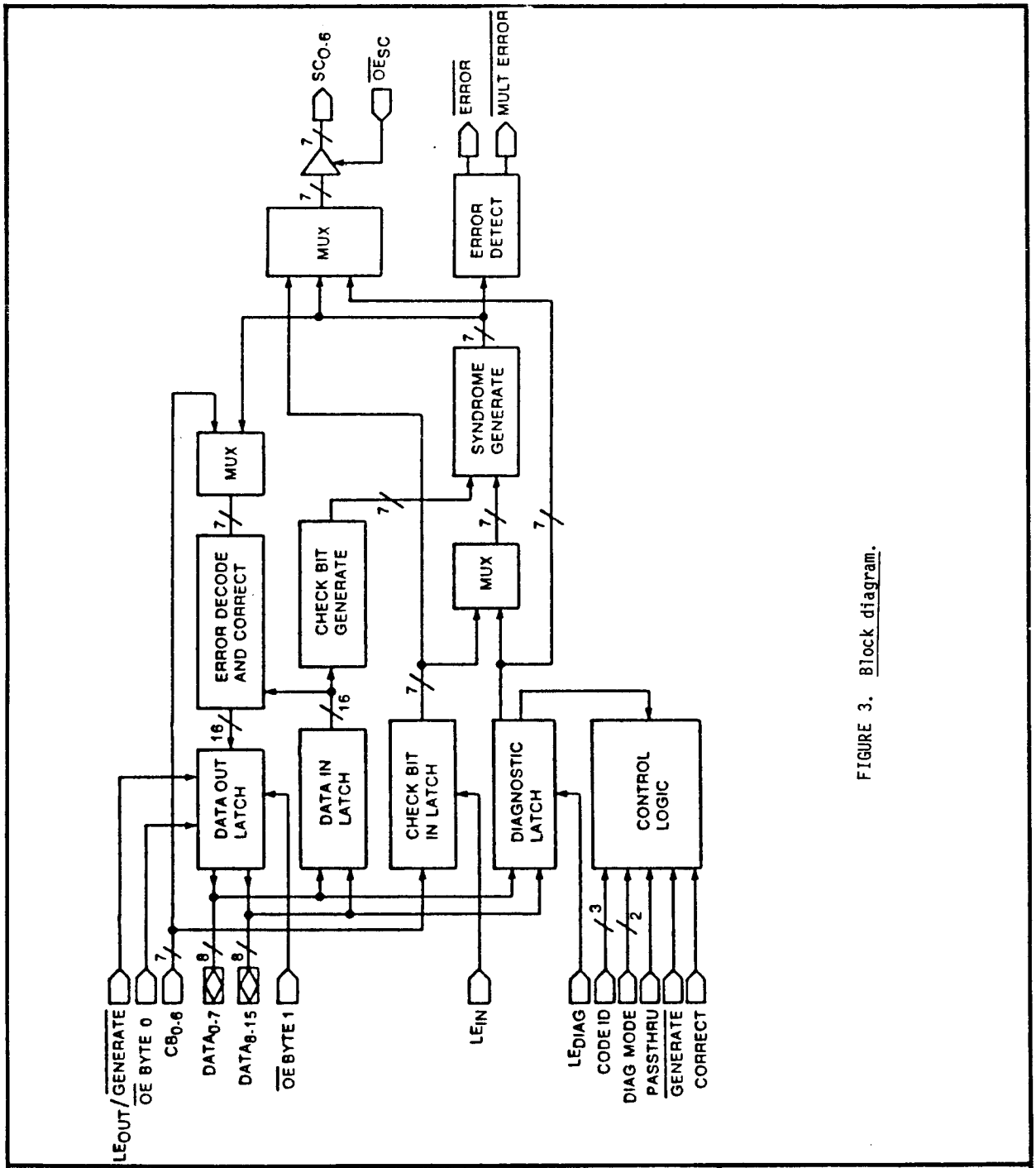

FIGURE 3. Block diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-88613
		REVISION LEVEL	SHEET 18

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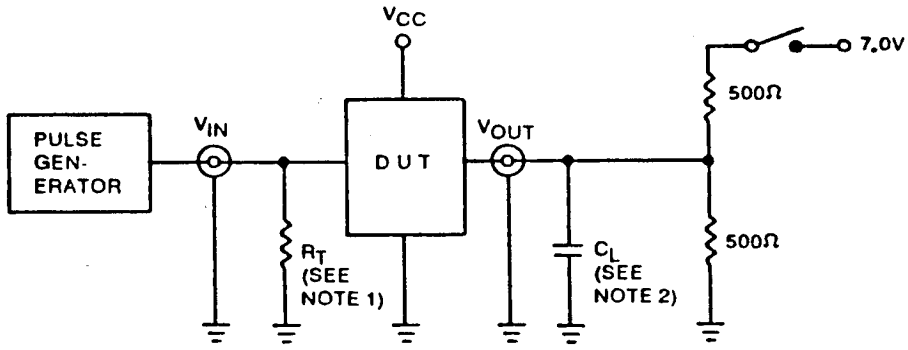

Test	Switch
Open drain Disable low Enable low	Closed
All other inputs	Open

NOTES:
1. R_T = Termination resistor which should be equal to Z_{OUT} of pulse generator.
2. C_L = Load capacitance and incluees jig and probe capacitance.
3. Equivalent loading circuit may be closed.

FIGURE 4. AC testing output load circuit.

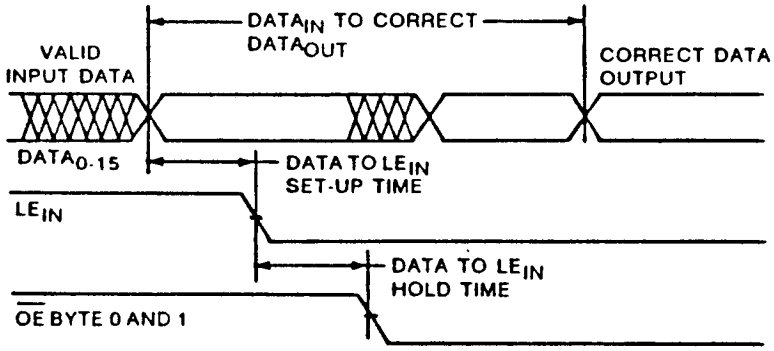

FIGURE 5. Timing diagram (DATA$_{IN}$ or LE$_{IN}$ to correct DATA$_{OUT}$).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{OUT} and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero defects shall be required.

d. Subgroups 7 and 8 testing shall be sufficient to verify functional operation of the device. These tests form a part of the vendors' test tape and shall be maintained and available from the approved sources of supply.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8a, 10

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC. The approved sources listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8861301TX	2/	IDT39C60AXCB	---
5962-8861301XX	61772	IDT39C60ACB	---
5962-8861301UX	61772	IDT39C60ALB	---
5962-8861302XX	61772	IDT39C60CB	---
5962-8861302UX	61772	IDT39C60LB	---
5962-8861302TX	2/	IDT39C60XCB	---
5962-8861303XX	34335	AM29C60A/BXC	---
5962-8861303YX	34335	AM29C60A/BYC	---
5962-8861303ZX	34335	AM29C60A/BZA	---
5962-8861303UX	34335	AM29C60A/BUA	---

1/ Caution. Do not use this number for item acquisition. Items acquired by this number may not satisfy the performance requirements of this drawing.

2/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088
61772	Integrated Device Technology, Incorporated 1566 Moffett Blvd Salinas, CA 93905 Point of contact: 3236 Scott Boulevard Santa Clara, CA 95052