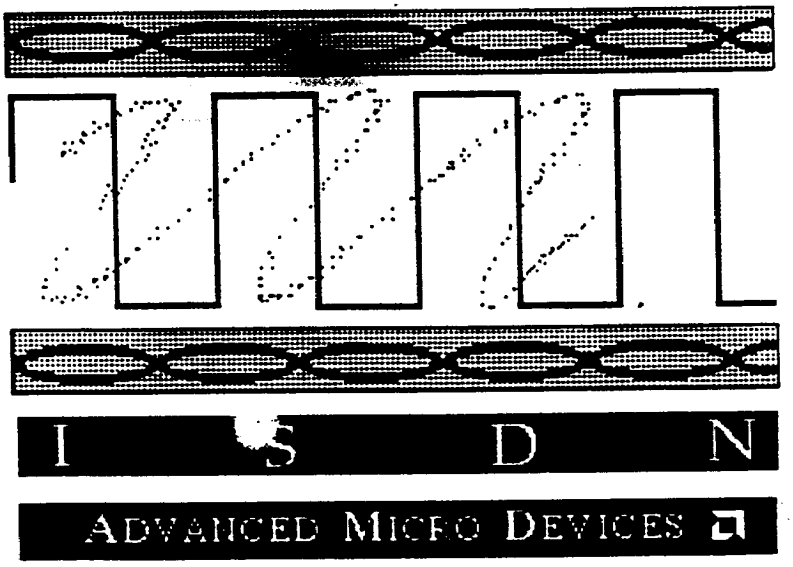
Audio Ringing Codec Filter (ARCOFI™)

Data Sheet
TM 1/90



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1. TABLE OF SYMBOLS

AD	Address bit (CMDR)
A/D	Analog to digital converter
ADI	ARCOFI® digital interface
AFE	Analog front end
ALS	Analog loop back via converter register (CR1)
ALM	Analog loop back via MUX (CR1)
ALZ	Analog loop back via Z side tone stage
AM	Address mode bit (CR2)
ARCOFI®	Audio ringing codec Filter
ASP	ARCOFI® signal processor
A-Law/μ-Law	A-Law/μ-Law bit (CR4)
BM	Beat mode bit (CR4)
BT	Beat tone bit (CR4)
CCITT	Comité Consultatif International Téléphonique et Télégraphique (International Telegraph and Telephone Consultative Committee)
CMDR	Command register
COP	Coefficient operation
CR1-4	Configuration register 1-4
CRAM	Coefficient RAM
D1-D3	Decimation filter 1 to 3
D/A	Digital to Analog Converter
DLM	Digital loop back via analog MUX (CR1)
DLS	Digital loop back via Converter register(CR1)
DLP	Digital loop back via PCM register (CR1)
DRAM	Data RAM
DSP	Digital signal processing
DTMF	Dual tone Multi-Frequency
ELS	Expansion Bit (CR2)
EFC	Enable feature control bit (CR2)
EWDF	Electric wave digital filter
FHM	Handsfree microphone input pin
FR	Frequency correction receive bits (CR1)

FSC	Frame synchronization (8Khz)
FX	Frequency correction transmit bits (CR1)
GNDA	Analog ground (0V)
GNDD	Digital ground (0V)
GR	Receiver gain (CR1)
GX	Transmitter gain (CR1)
GZ	Side tone gain (CR1)
HFS	Hands-Free state (CR3)
HON	Handset earpiece output - pin
HOP	Handset earpiece output + pin
IDR	Initialize Data RAM (CR1)
IOM®2	ISDN oriented modular
ISDN	Integrated service digital network
LSN	Loudspeaker output - pin
LSP	Loudspeaker output + pin
MIN	Handset microphone input - pin
MIP	Handset microphone input + pin
NOP	Normal operation
NOT	No test mode (CR1)
PCI	Peripheral Control Interface
PM	Piezo mode bit (CR4)
POR	Power on reset
PU	Power up bit (CMDR)
RCS	Receive-channel select bit (CMDR)
RDY	Ready state (CR3)
RX	Receive
SA-SD	PCI I/O Pins
CLK/DCLK	System clock pin (512 kHz - SLD; 1.536 MHz - IOM®2)
SIP	Serial interface port pin
SLD	Subscriber line data
SOP	Status operation

SP1-2	Supplementary function pins 1-2
TG	Tone generator (CR4)
TM	Tone mode bits (CR4)
TR	Three party conferencing (CR2)
TX	Transmit
WDF	Wave digital filter

2. INTRODUCTION

The PSB 2160 ARCOFI® provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. The ARCOFI® fulfils all necessary requirements for the completion of a low cost digital telephone. Full featured applications including handsfree telephony are carried out by the addition of a voice switched speakerphone circuit. The ARCOFI® performs all coding, decoding and filtering functions according to CCITT and AT&T norms.

The ARCOFI® integrates a DTMF generator in the transmit direction and a tone generator plus a ringing generator in the receive path. The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on chip as well as a secondary input for a handsfree microphone. The microphone analog gain is user programmable under microprocessor control.

3. GENERAL DESCRIPTION

3.1. DISTINCTIVE FEATURES

* Applications in digital terminal equipment including a voice path
* Low power CMOS technology
* Test and maintenance loopbacks in the analog front end and the digital processor
* SLD or IOM®2 serial interface bus
* Flexible Peripheral Control Interface (PCI).
* CODEC filter
* DTMF, tone and ringing generators
* Separate output for a piezo ringer
* Dual analog inputs for handset and "handsfree" microphones plus an auxiliary differential analog input.
* Two sets of differential outputs for a handset earpiece and a loudspeaker
* Power dissipation: active: 150 mW
standby: 10 mW
* Temperature range: -25 to 70 C (functions guaranteed)
0 to 70 C (specifications guaranteed)
* Package: 24 pin DIL, 28 pin PLCC

3.2. FUNCTIONAL DESCRIPTION

The ARCOFI® bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM CODEC (coder + decoder) with all the necessary transmit and receive filters. A block diagram of the ARCOFI® is shown in FIG 3.1.

The ARCOFI® can be subdivided in three main blocks;

- The ARCOFI® Analog Front End (AFE)
- The ARCOFI® Signal Processor (ASP)
- The ARCOFI® Digital Interface (ADI)

A brief description of each block will provide acquaintance with the ARCOFI®. A detailed description follows in the proceeding chapters.

3.2.1. ANALOG FRONT END (AFE)

The AFE interfaces the analog transducers i.e microphones, earpiece and loudspeaker to the ARCOFI®.

The transmit section of the AFE consists of a high sensitivity differential input for a handset microphone, a differential auxiliary input and a single ended low sensitivity input for a handsfree microphone. Input sources are selectable via the analog I/MUX.

The AFE receive direction features a handset earpiece differential output and a loudspeaker differential output. All outputs are selectable via the analog O/MUX.

High performance A/D and D/A converters provide the necessary interfaces with the ARCOFI® signal processor section.

3.2.2. ARCOFI® BLOCK DIAGRAM

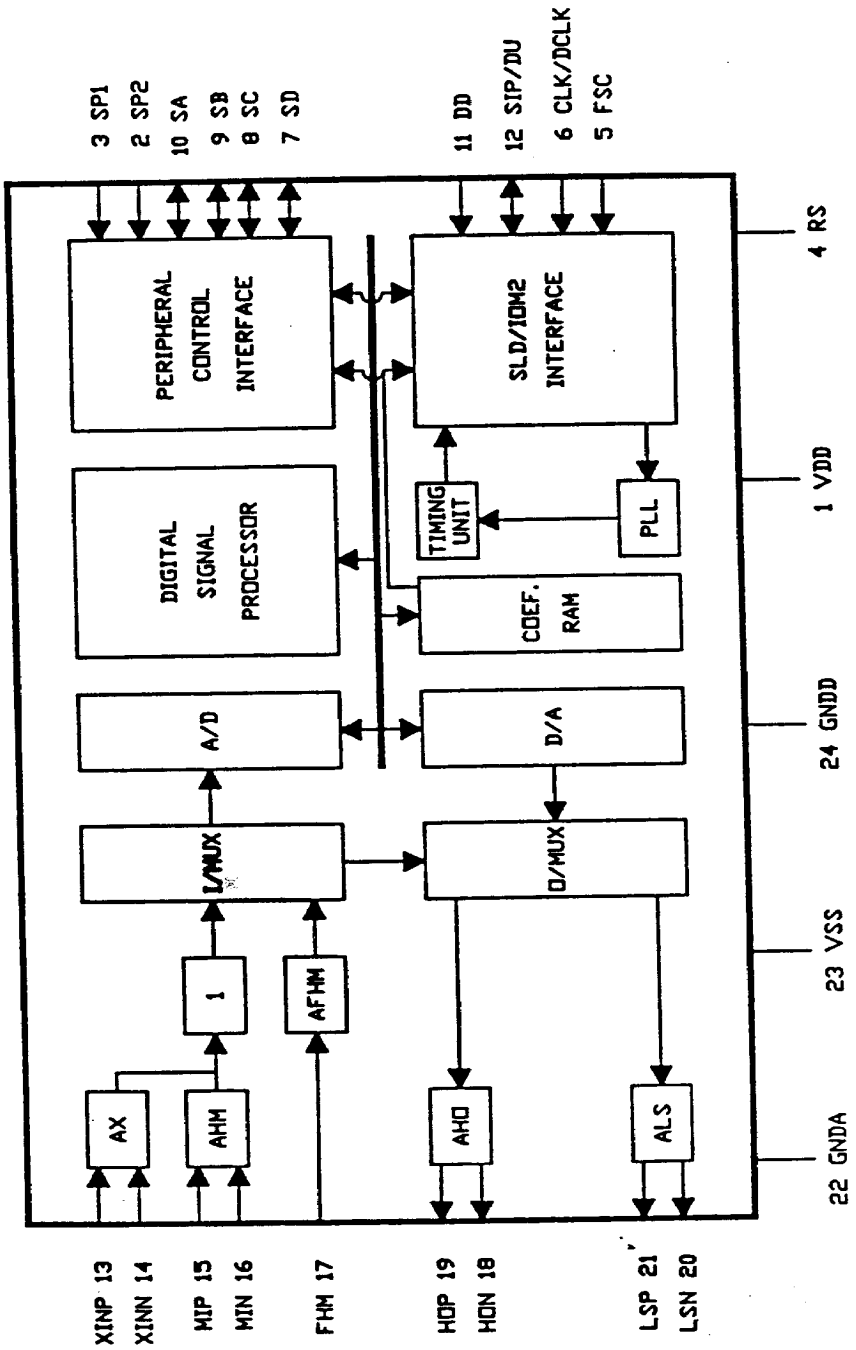


Figure 3.1: ARCOFI® BLOCK DIAGRAM (DIP 24 PINNING)

3.2.3. ARCOFI® SIGNAL FLOW GRAPH

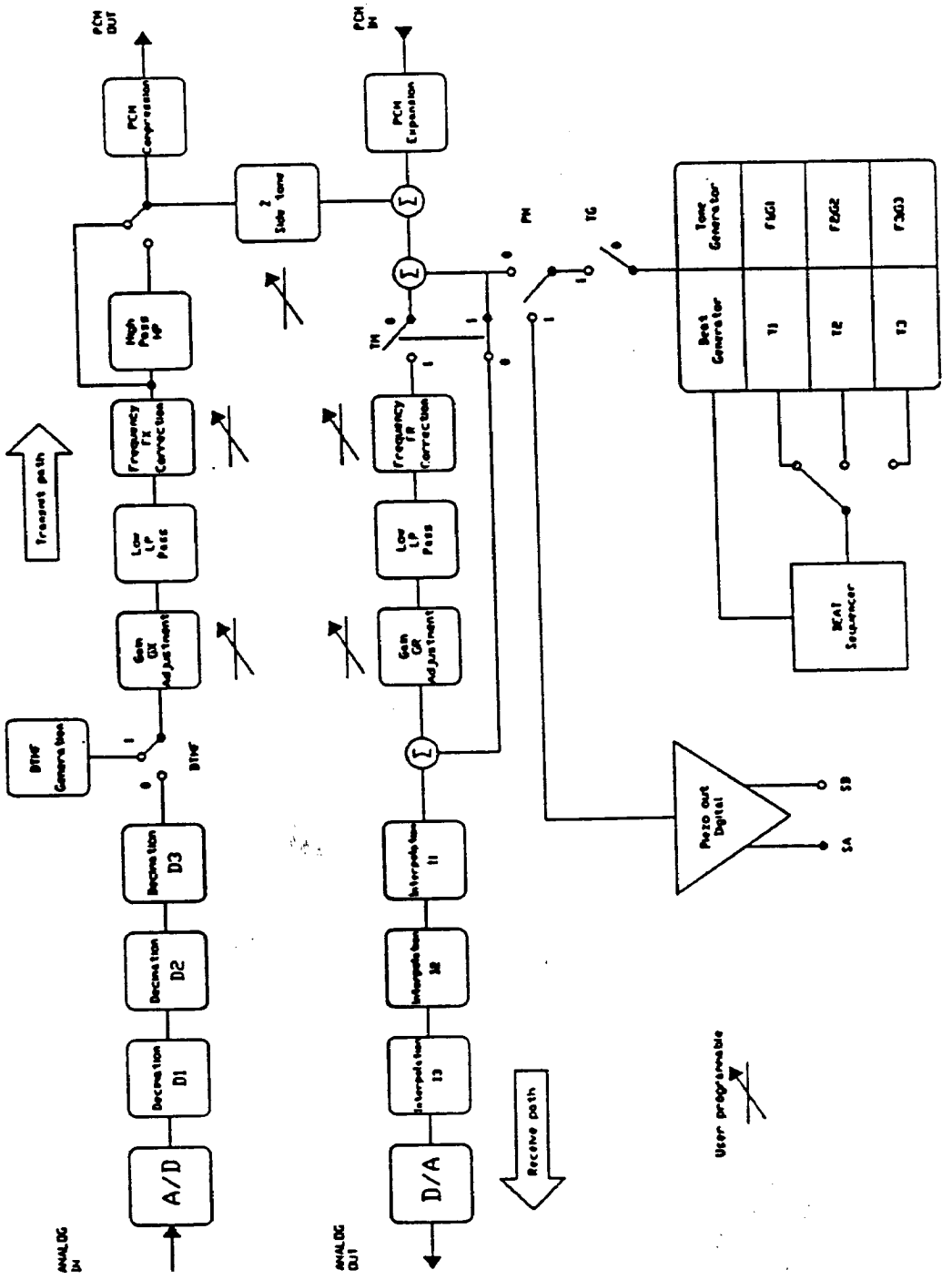


Figure 3.2:

3.2.4. ARCOFI® SIGNAL PROCESSOR (ASP)

The ASP block performs all the CODEC filter functions using digital signal processing techniques. All functions performed by the ASP section can be characterized by their high level of flexibility and programmability.

The ASP main features are:

* two gain adjustment stages

Gain adjustment for both receive and transmit path. A wide control range is programmable directly by the user. Transmit and receive level adaptation is therefore made possible.

* Two transducer correction filters

The FX filter in the transmit direction and the FR filter in the receive direction can be programmed to correct for the analog transducer frequency characteristics.

* Side tone gain adjustment

The side tone level can be adjusted via a programmable Z gain stage.

* DTMF, ringing and tone generation

DTMF signals can be added in the transmit path. In the receive direction a multi-tone ring signal can be generated and output by the loudspeaker or by an independent piezo ringer. Tones can also be superimposed on the incoming PCM signal. All tones are amplitude and frequency programmable (except for piezo ringer).

3.2.5. ARCOFI® DIGITAL INTERFACE (ADI)

The ADI features are:

* a selectable SLD or IOM®2 serial bus interface through which the ARCOFI® transfers the voice channels and communicates with the system microcontroller.
* A programmable multipurpose interface for Peripheral Control use (PCI). The PCI Interface provides 4 programmable I/O pins to control peripheral devices.

3.2.6. TYPICAL APPLICATION

The following diagrams illustrate some of the typical applications possible with the PSB 2160 ARCOFI®.

3.2.7. ISDN IOM®2 ARCHITECTURE

Figure 3.3 shows the ISDN oriented modular (IOM®2) architecture concept. In this context, the ARCOFI® forms, together with the PEB 2070 ICC and a PEB 2080 SBC, or an ISAC-S PEB 2085 a complete digital telephone as specified in the CCITT I-series recommendation at the "S" reference point. The ARCOFI® can also be used with the ISDN echo cancellation circuit PEB 2090 IEC to form a digital telephone at the "U" reference point. Other line transceiver such as the PEB 2095 ISDN Burst transceiver can also be used.

3.2.8. DIGITAL FEATURE PHONE

Figure 3.4 shows a typical digital feature phone application. The SAB 8051 microcontroller handles the key monitoring and display activities as well as some of the communication protocols (LAPD).

3.2.9. FEATURE PHONE WITH SPEAKERPHONE

A digital feature phone using the ARCOFI® can easily be expanded for handsfree applications by the addition of a voice switched speakerphone circuit (see Figure 3.5).

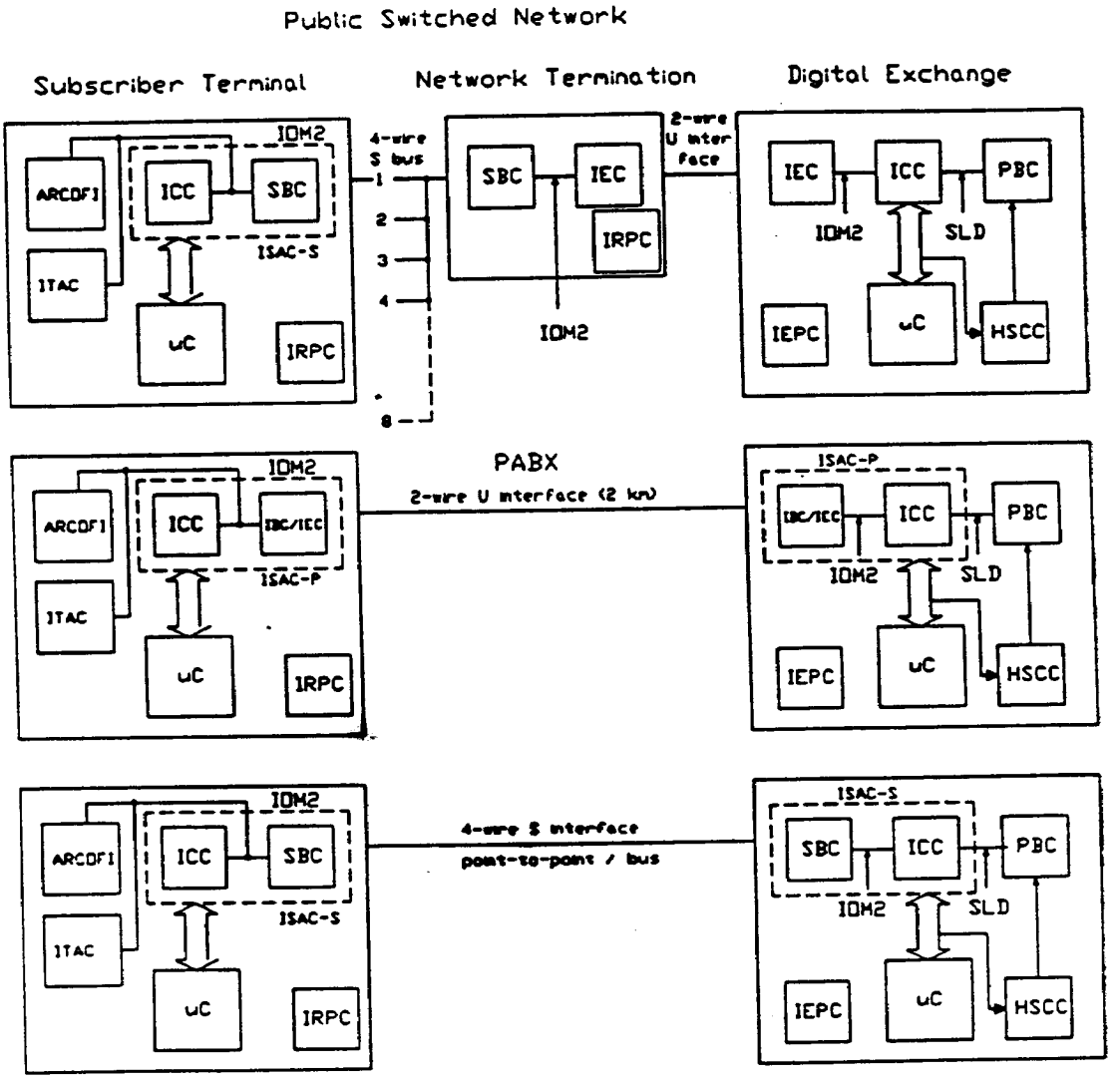


Figure 3.3:

3.2.11. DIGITAL FEATURE PHONE

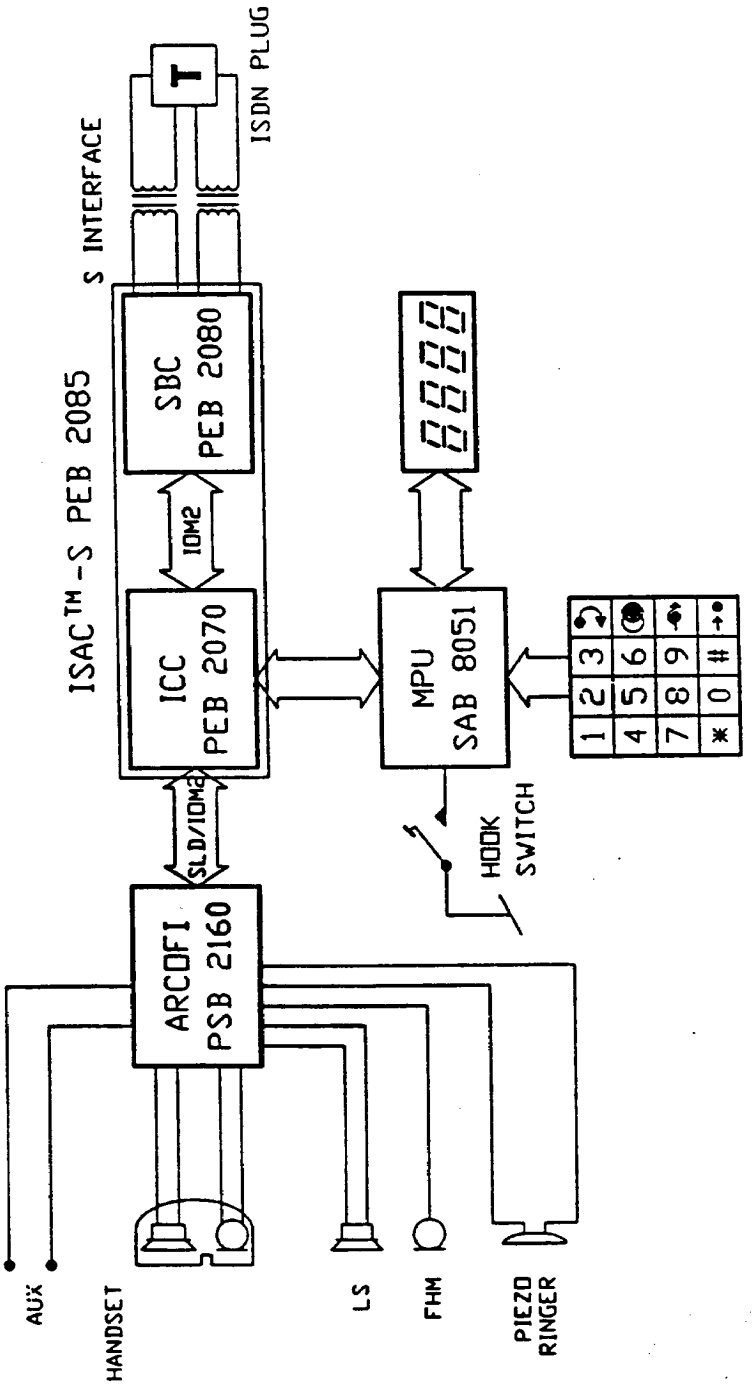


Figure 3.4:

3.2.1:. FEATURE PHONE WITH SPEAKERPHONE (FIG 3.5)

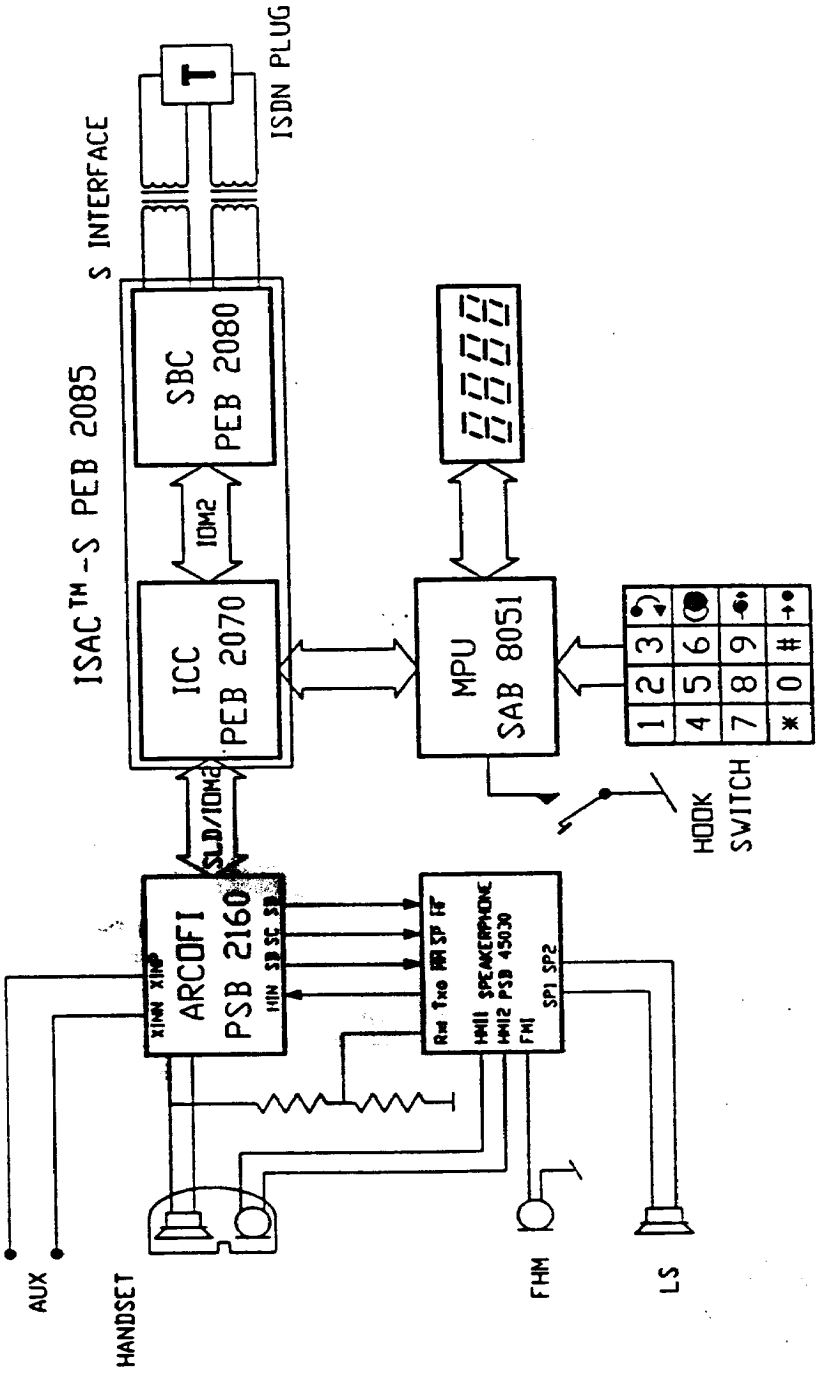


Figure 3.5:

3.3. PIN DEFINITION & FUNCTIONS

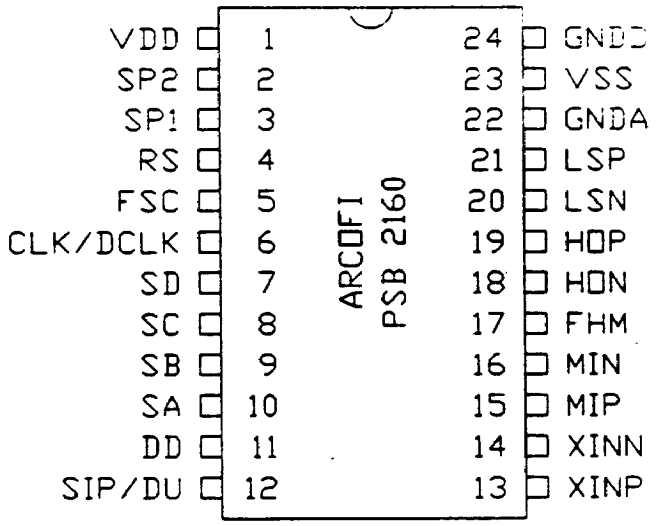
PIN PLCC28	PIN DIL24	SYMBOL	FUNCTION
8,17,19, 23	1	VDD	+5V Positive power supply
24 25	2 3	SP2 SP1	Supplementary function: Appropriate pin strapping access supplementary functions including test modes as describe in section 6. ADI.
26	4	RS	Reset input: When pin RESET is forced high the ARCOFI® is placed in a power down mode. All configration registers are reset to default values. The I/O pins SA-SD and SIP/DU are defaulted to inputs until the ARCOFI® is reconfigured
28	5	FSC	Frame sync.: 8 kHz signal, phase locked to CLK. When high, SIP behaves as an input and the ARCOFI® can receive data through pin SIP. When low, SIP behaves as an output and data can be transferred from the ARCOFI® to the system via pin SIP. When in IOM®2 mode FSC supplies to the ARCOFI® a synchronization signal according to the IOM®2 specification.
1	6	CLK/DCLK	CLK System clock: 512 kHz supplied by the application system clock when SLD mode is selected. DCLK system clock: 1.536 MHz supplied by the application system clock when IOM®2 mode is selected.
2 3 4 5	7 8 9 10	SD SC SB SA	Programmable I/O PCI pins: With the appropriate bit setting in configuration register CR2, each SA-SD pin can be declared independently as input or as output. Data received from or forwarded to the PCI pins are allocated to the signalling channel. When selected, the tone generator signals can be directed to pins SA & SB. (SA & SB then in opposite phase).
6	11	DD	DD; Data Downstream: Receive data from a layer 1 IOM®2 controlling device.
7	12	SIP/DU	SIP; Serial Interface Port: This serial bidirectional port is clocked by CLK when SLD mode is selected. DU; data upstream: Transmit data to the layer 1 IOM®2 controlling device.
9 10	13 14	XINP XINN	X input: These auxiliary inputs provide a normalized differential audio input for an additional analog device.

PIN PLCC28	PIN DIL24	SYMBOL	FUNCTION
11 12	15 16	MIP MIN	Handset microphone inputs: MIP & MIN provide highly symmetrical differential inputs for commonly used telephone microphones.
13	17	FHM	Handsfree microphone: This single ended input can be used to interface an electret microphone for speakerphone applications.
14 15	18 19	HON HOP	Handset earpiece outputs: HOP & HON are differential output pins which can drive handset earpiece transducers directly.
16 18	20 21	LSN LSP	Loudspeaker outputs: LSN and LSP are differential outputs pins which can drive a 50 Ohms loudspeaker directly. A piezo transducer connected via SA and SB can also be used for ringing signals instead of a loudspeaker
20	22	GNDA	Analog ground: not internally connected to GNDD. All analog signals are referred to this pin
21	23	VSS	-5V Negative power supply
22	24	GNDD	Digital ground: (0V) not internally connected to GNDA. All digital signals are referred to this pin

Table 3.1:

3.3.1. ARCOFI® PINOUT

DIP :



PLCC :

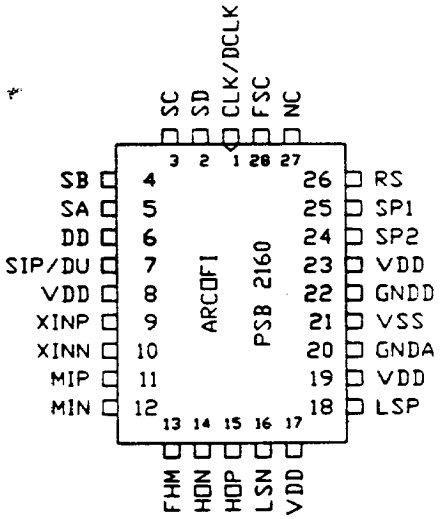


Figure 3.6:

3.4. PROGRAMMABLE REGISTERS

The SLD or the IOM®2 bus mode is used to control and program the operations performed by the ARCOFI®. The following lists the ARCOFI® internal registers as they appear in each section.

ARCOFI® DIGITAL INTERFACE (ADI)

* CMDR: 8 bit command register
* CR1-4: four 8 bit configuration registers

ARCOFI® SIGNAL PROCESSOR (ASP)

* Transmit gain register GX (2 bytes)
* Receive gain register GR (2bytes)
* Transmit filter coefficient register FX (10 bytes)
* Receive filter coefficient register FR (10 bytes)
* Sidetone gain register Z (1 byte)
* DTMF frequency tone register (2 bytes)
* Tone Ring/Tone Generator frequency register (6 bytes)
* Tone Ring/Tone Generator amplitude register (3 bytes)
* Beat tone Generator timing register (6 bytes)

3.5. OPERATING MODES

Some of the possible ARCOFI® operating modes are documented in the following paragraph. The four ARCOFI® configuration registers have enough built in flexibility to accommodate an extensive set of user calling procedures. In conjunction with the system µP, the PEB 2070 ICC ISDN communication controller and the PEB 2080 SBC S-Bus Controller, the system designer can implement an extensive set of terminal attributes.

The following operating mode description table on the next page is not exhaustive but should be used as an example of possible functions performed by the ARCOFI®.

STATE	DESCRIPTION
POR	Power on reset: When power is supplied to the ARCOFI® a hardware reset via an RC network connected to input pin RESET will force all ARCOFI® internal registers to default values. The ARCOFI® registers reset state is described in section 4.0 (ADI)
STAND BY	The system microprocessor can initialize the ARCOFI via the SLD or the IOM®2 bus to a different set of filter and configuration values. Whilst remaining in power down (PU=0, CMDR) a new set of filter coefficient and configuration bits can be loaded in the ARCOFI®.
READY	The system MPU detects activity from the hookswitch or from the keyboard. The ARCOFI® can be placed in READY state where all handset I/O are enabled (MIP, MIN & HOP, HON activated).
RINGING	The system MPU detects an incoming call, the ARCOFI® can be placed in a RINGING state by activating the tone ringer via CR4 and configuring the ARCOFI® such that either the loudspeaker outputs LSN & LSP or the piezo ringer outputs pin SA & SB are enabled.
DTMF	All audio inputs can be disabled by forcing a MUTE code in CR3. DTMF tones are generated in the ASP transmit path.
PULSE DIAL	Handset audio path can be enabled by forcing a READY code in CR3. A single tone can be superimposed into the audio receive path so as to provide audible feedback when dialling.
LOUD HEARING	The handset microphone inputs MIP & MIN and the loudspeaker outputs LSN & LSP can be activated by configuring CR3.
HANDS FREE	The handset audio I/O's are disabled. The handsfree microphone input and loudspeaker outputs LSN & LSP are activated by configuring CR3.
MUTE	The ARCOFI® can be placed in a mute state by enabling the handset outputs HOP & HON. All other analog I/O's being disabled. (MUTE code in CR3).
FEATURE TONE	A single tone can be superimposed to the incoming PCM voice signal. Application requiring system function audible feedback are therefore made possible.

Table 3.2:

4. ANALOG FRONT END DESCRIPTION

The analog front end section of the ARCOFI® interfaces the analog transducers with the subsequent signal processor. In the transmit direction the AFE function is to amplify the transducer input signals (microphones) and convert them into digital signals. In the AFE receive section , the incoming digital signals are converted to analog signals output to an earpiece and a loudspeaker. The attenuation plan and electrical characteristics of the AFE are adapted to meet commonly used voice transducers.

4.1. ANALOG INPUTS

A high sensitive differential input MIP and MIN connects a handset microphone to a gain programmable amplifier AHM. When selected the differential X inputs (amplification stage AX) can be activated while deselecting the MIP/MIN inputs. Coming from AHM or AX the signal is forwarded to the input of the analog multiplexer driving the oversampling A/D converter. A third analog input source is provided through pin FHM. This "handsfree" microphone input connects the multiplexer via amplifier AFHM. The programmable amplifier AHM provides a coarse gain adjustment range. Fine gain adjustment is performed in the digital domain via the programmable gain adjustment filter GX (see ARCOFI® signal processing section). This allows a perfect level adaptation to various types of microphone transducers without loosing on the signal to noise performance. The main electrical characteristics of the analog inputs are summarized in table 4.2

4.2. ANALOG OUTPUTS:

Fully differential outputs HOP and HON connect the amplifier AHO to the handset earpiece. Differential outputs LSN & LSP are provided for use with a 50 ohm loudspeaker. Up to 100 mW of power can be delivered to the loudspeaker via amplifier ALS. The power amplifier ALS is short-circuit protected. All outputs are sourced by a digital to analog converter via an output analog multiplexer. The selection of the output source is performed through the configuration register CR3 via the SLD int[redacted]. The main electrical characteristics of the analog outputs are summarized in table 4.3

4.2.1. AUXILIARY OUTPUT

A separate auxiliary X output can be provided in conjunction with the earpiece output. The discrete circuit diagram shown in FIG 4.1 is suggested when an auxiliary headset output is required. Table 4.1 indicates the resulting output levels at points 1..1' and 2..2' for different load impedances.

Output load	Min	Typ	0 dBmO	Max	Peak	Unit	Ref
HOP/HON output level	-24.13	-9.13	4.17	5.87	7.31	dBm	0.775V
X output (2..2')	6.70E-02	3.77E-01	1.77E00	2.12E00	2.50E00	Vpk	V
	4.73E-02	2.66E-02	1.23E00	1.50E00	1.77E00	Vrms	V
Rl = 10 kohms	-30.447	-15.477	-2.147	-0.447	0.933	dBmO	1.576V
Rh = 10 kohms	-24.277	-9.277	4.023	5.723	7.163	dBm	0.775V
R-network attenuation	0.147	0.147	0.147	0.147	0.147	dB	gain
X output (2..2')	6.33E-02	3.56E-01	1.65E00	2.00E00	2.36E00	Vpk	V
	4.47E-02	2.52E-01	1.16E00	1.41E00	1.67E00	Vrms	V
Rl = 10 kohms	-30.939	-15.939	-2.639	-0.939	0.501	dBmO	1.576V
Rh = 200 ohms	-24.769	-9.769	3.531	5.231	6.671	dBm	0.775V
R-network attenuation	0.639	0.639	0.639	0.639	0.639	dB	gain
Earpiece output (1..1')	3.88E-02	2.18E-01	1.01E00	1.23E00	1.45E00	Vpk	V
	2.75E-02	1.54E-01	7.14E-01	8.69E-01	1.03E00	Vrms	V
Rl = 10 kohms	-35.176	-20.176	-6.876	-5.176	-3.736	dBmO	1.576V
Rh = 200 ohms	-29.006	-14.0006	-0.706	0.994	2.434	dBm	0.775V
R-network attenuation	4.876	4.876	4.876	4.876	4.876	dB	gain

Table 4.1:

4.2.2. AUXILIARY OUTPUT DIAGRAM (FIG 4.1)

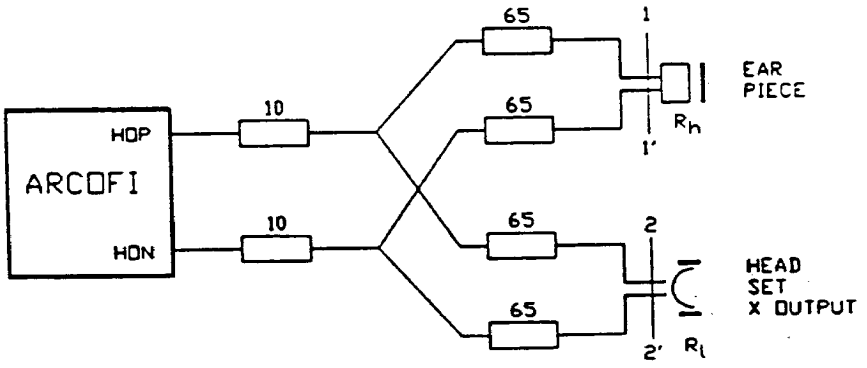


Figure 4.1:

4.2.3. ANALOG FRONT END ELECTRICAL INTERFACE INPUTS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST COND
ZHM	Handset microphone input impedance	150		Kohm	300-3400 Hz
VHM	Handset microphone max input voltage swing *)		8.04**)	mVp	
AHM	Handset microphone amplifier gain AHM	16	52.0**)	dB	Pin MIP,MIN 3.86 mV at 1Khz
ZFHM	Handsfree microphone input impedance	150		Kohm	300-3400Hz
VFHM	Handsfree mircophone max input voltage swing *)		127	mVp	
AFHM	Handsfree microphone amplifier gain		28.0	dB	Pin FHM 19.5 mV at 1kHz
ZXIN	Auxiliary pin input impedance	150		Kohm	300-3400 Hz
VXIN	Auxiliary Xin max input voltage swing *)		563	mVp	
AXIN	Auxiliary Xin amplifier gain AX		15.1	dB	Pin XINN & XINP 270 mV at 1 Khz

Table 4.2:

*) A maximum swing signal corresponds to a 3.14 dBm0 signal at the A/D converter. This corresponds also to a PCM code overload +/-127.(3.14 dBm0 = 2.26 Vrms = 3.2 Vp= 6.4 Vpp)

**) See description of CR3

4.2.4. ANALOG FRONT END ELECTRICAL INTERFACE OUTPUTS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST COND
ZHO	Handset earpiece output impedance		2	Ohms	300-3400Hz
VHO	Handset earpiece max output voltage swing *)		2.542	Vp	Load measured from HOP to HON
VHOH	Handset earpiece output high voltage *)		2.54	Vp	input load -1mA @ HOP/HON
VHOL	Handset earpiece output low voltage *)		2.54	Vp	input load +1mA @ HOP/HON
ZLS	Loudspeaker output impedance		2	Ohms	300-3400 Hz
VLS	Loudspeaker max output voltage swing *)		3.2	Vp	Load measured from LSN to LSP
VLSOH	Loudspeaker output high voltage *)		3.0	Vp	input load -100mA @ LSN/LSP
VLSOL	Loudspeaker output low voltage *)		3.0	Vp	input load +100mA @ LSN/LSP

*) The maximum output voltage swing corresponds to a maximum incoming PCM code (+/-127).

Table 4.3:

4.2.5. ARCOFI® AFE ATTENUATION PLAN

Transmit direction

Transmit	Min	Typ	0 dBMO	Max	Peak	Unit	Ref
MIP/MIN	2.15E-04	1.21E-03	5.60E-03	6.81E-03	8.04E-03	Vpk	V
Microphone	1.52E-04	8.56E-04	3.96E-03	4.82E-03	5.68E-03	Vrms	V
input level at	-80.3	-65.3	-52	-50.3	-48.86	dBmO	1.576V
max gain	-74.13	-59.13	-45.83	-44.13	-42.69	dBm	0.775V
AHM = 52 dB	52	52	52	52	52	dB	gain
Xin	1.51E-02	8.48E-02	3.92E-01	4.77E-01	5.63E-01	Vpk	V
Input level	1.07E-02	5.99E-02	2.77E-01	3.37E-01	3.98E-01	Vrms	V
	-43.4	-28.4	-15.1	-13.4	-11.96	dBmO	1.576V
	-37.23	-22.23	-8.93	-7.23	-5.79	dBm	0.775V
AX gain	15.1	15.1	15.1	15.1	15.1	dB	gain
FHM	3.41E-03	1.92E-02	8.87E-02	1.08E-01	1.27E-01	Vpk	V
Input level	2.41E-03	1.36E-02	6.28E-02	7.63E-02	9.01E-02	Vrms	V
	-56.3	-41.3	-28	-26.3	-24.86	dBmO	1.576V
	-50.13	-35.13	-21.83	-20.13	-18.69	dBm	0.775V
AFHM gain	28	28	28	28	28	dB	gain
A/D	8.57E-02	4.82E-01	2.23E00	2.71E00	3.20E00	Vpk	V
Input level	6.06E-02	3.41E-01	1.58E00	1.92E00	2.26E00	Vrms	V
ARCOFI	-28.3	-13.3	0	1.7	3.14	dBmO	1.576V
(Bypass mode)	-22.13	-7.13	6.17	7.87	9.31	dBm	0.775V
PCM value	+/-43	+/-83	+/-118	+/-123	+/-127	PCM word	

Table 4.4:

Receive	Min	Typ	0 dBmO	Max	Peak	Unit	Ref
LSN/LSP	8.57E-02	4.82E-01	2.23E00	2.71E00	3.20E00	Vpk	V
Output level	6.06E-02	3.41E-01	1.58E00	1.92E00	2.26E00	Vrms	V
symmetrical in	-28.3	-13.3	0	1.7	3.14	dBmO	1.576V
a 50 ohms load	-22.13	-7.13	6.17	7.87	9.31	dBm	0.775V
ALS gain	0	0	0	0	0	dB	gain
HOP/HON	6.81E-02	3.83E-01	1.77E00	2.15E00	2.54E00	Vpk	V
Output level	4.82E-02	2.71E-01	1.25E00	1.52E00	1.80E00	Vrms	V
symmetrical in	-30.3	-15.3	-2	-0.3	1.14	dBmO	1.576V
a 200 ohms load	-24.13	-9.13	4.17	5.87	7.31	dBm	0.775V
AHO gain	-2	-2	-2	-2	-2	dB	gain
D/A	8.57E-02	4.82E-01	2.23E00	2.71E00	3.20E00	Vpk	V
Output level	6.06E-02	3.41E-01	1.58E00	1.92E00	2.26E00	Vrms	V
ARCOFI®	-28.3	-13.3	0	1.7	3.14	dBmO	1.576V
(Bypass mode)	-22.13	-7.13	6.17	7.87	9.31	dBm	0.775V
PCM value	+/-43	+/-83	+/-118	+/-123	+/-127	PCM word	

Table 4.5:

4.2.6. AFE BLOCK DIAGRAM (FIG 4.2)

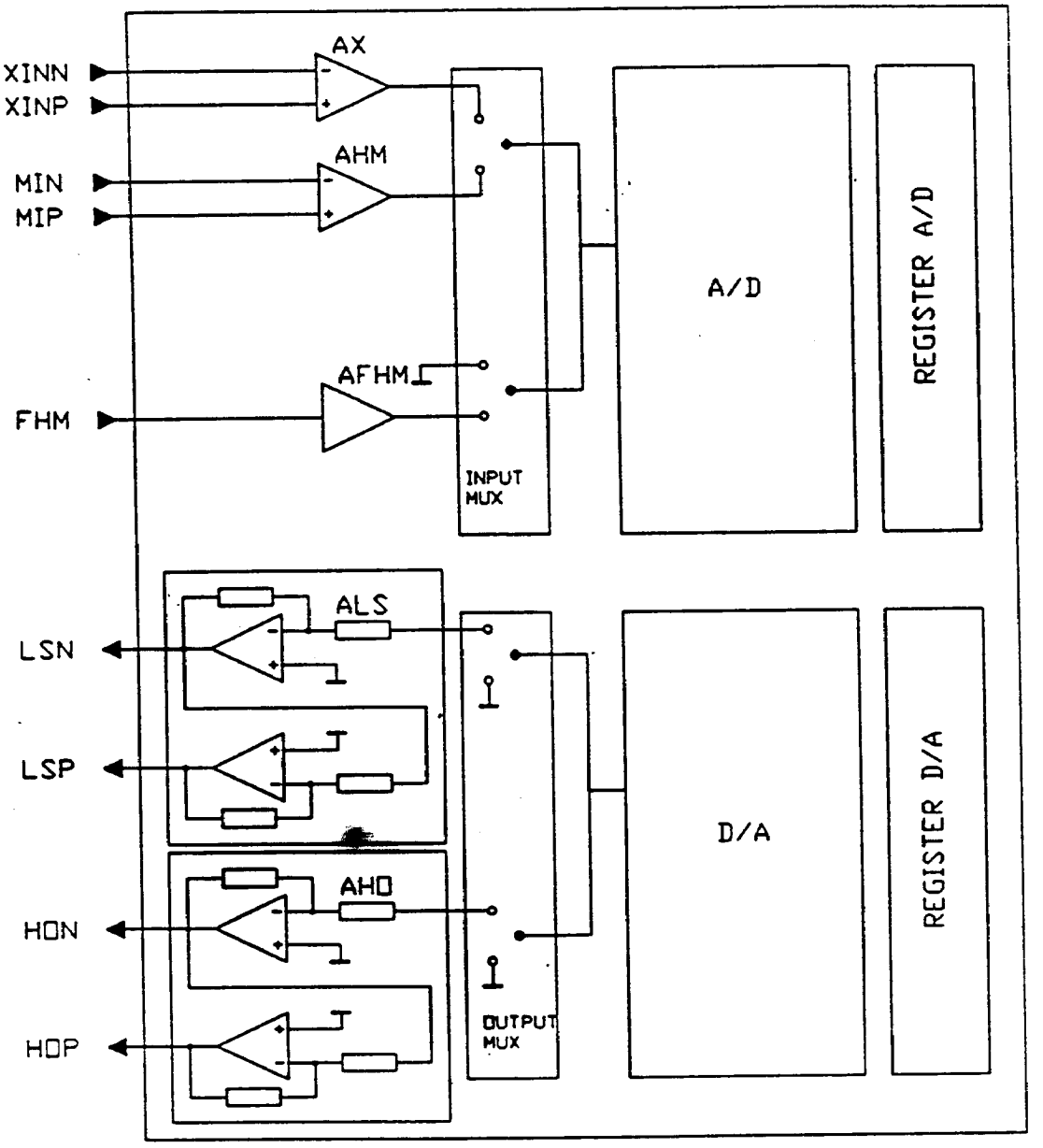


Figure 4.2:

4.2.7. USING THE ARCOFI® WITH A SPEAKERPHONE CIRCUIT

When using the ARCOFI® with a speakerphone circuit PSB 45030 the ready mode RDY in configuration register 3 can be selected. In this particular mode, the MIP/MIN input and the HOP/HON output are activated. The HOP/HON level should be attenuated to match the maximum PSB45030 RXI pin input level. A maximum of 50 mW can be delivered at the PSB 45030 SP1 and SP2 pins in a 50 ohms loudspeaker without using additional discrete circuitry. A block diagram of the combined PSB2160 ARCOFI® and the PSB45030 SPEAKERPHONE is shown in figure 4.3 using the RDY mode.

Alternative application diagram combining the ARCOFI® and the PSB45030 are also possible. A more detailed description of these types of application will be summarized in a separate application note.

4.2.8. ARCOFI® PLUS SPEAKERPHONE (FIG 4.3)

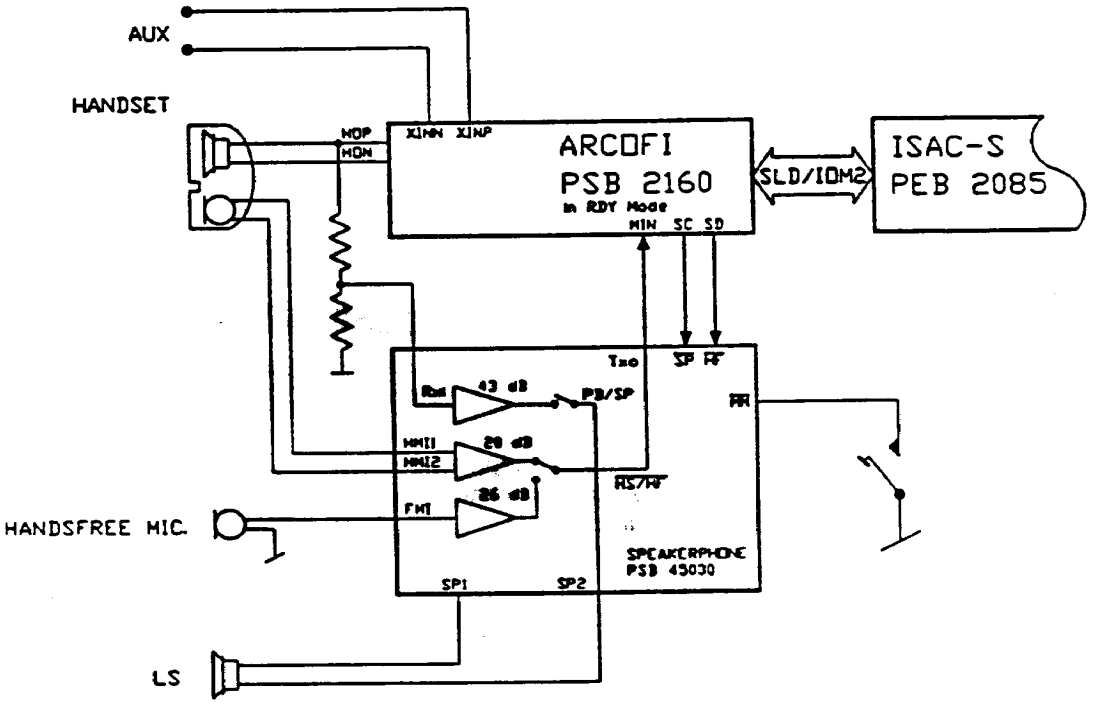


Figure 4.3:

5. ARCOFI® SIGNAL PROCESSOR DESCRIPTION

5.1. THE ARCOFI® SIGNAL PROCESSOR (ASP)

The ARCOFI® signal processor (ASP) has been conceived to perform all CCITT recommended filtering in both transmit and receive paths and is therefore fully compatible to the G.714 CCITT specification. The code processed by the ASP is provided in the transmit direction by an oversampling A/D converter situated in the analog front end (AFE). Once processed the speech signal is converted into an 8 bit A-law or μ-law PCM format or remains a 16 bit linear word according to the bit setting in the configuration register 3 (see CR3 in section 6., ADI).

In the receive direction the incoming PCM stream is expanded in a linear format and subsequently processed until passed to the D/A converter.

The entire ARCOFI® signal flow plan is shown in FIG 5.1

5.2. TRANSMIT PATH SIGNAL PROCESSING

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8 kHz PCM rate. These filters attenuate out-of-band noise by limiting the received signal to the voiceband.

The decimation stages end with a low pass filter which band limits the voice signal according to the CCITT recommendation G.714. A high pass filter is also provided to remove power line frequencies. The ARCOFI® meets or exceeds all CCITT and north-American recommendation on attenuation distortion and group delay distortion (See Fig 5.2 and 5.3)

The GX gain adjustment stage is digitally programmable allowing the gain to be programmed from -45 to +12 dB within a +/-0.25 dB tolerance range.The CCITT templates are guaranteed in the area 0dB to +6dB when using either FHM or AUX or MIC programmed with either 16dB or 22dB or 28dB. Two bytes are necessary to set GX to the desired value.

The voice signal after being linearly processed can be output as an 8 bit PCM word according to the CCITT G711 A-Law or the north American μ-Law format. If desired the compression stage can be by-passed, a 16 bit linear word is then output to the ARCOFI® digital interface.

The transmit path contains a frequency correction filter FX allowing an optimum adaptation to different types of microphone (dynamic, piezoelectric or electret).

Table 5.1 specifies the parameters for the transmit path. The measurements are made with GX and FX disabled and are applicable for both A-Law or μ-Law.

5.2.1. ARCOFI® SIGNAL FLOW GRAPH (FIG 5.1)

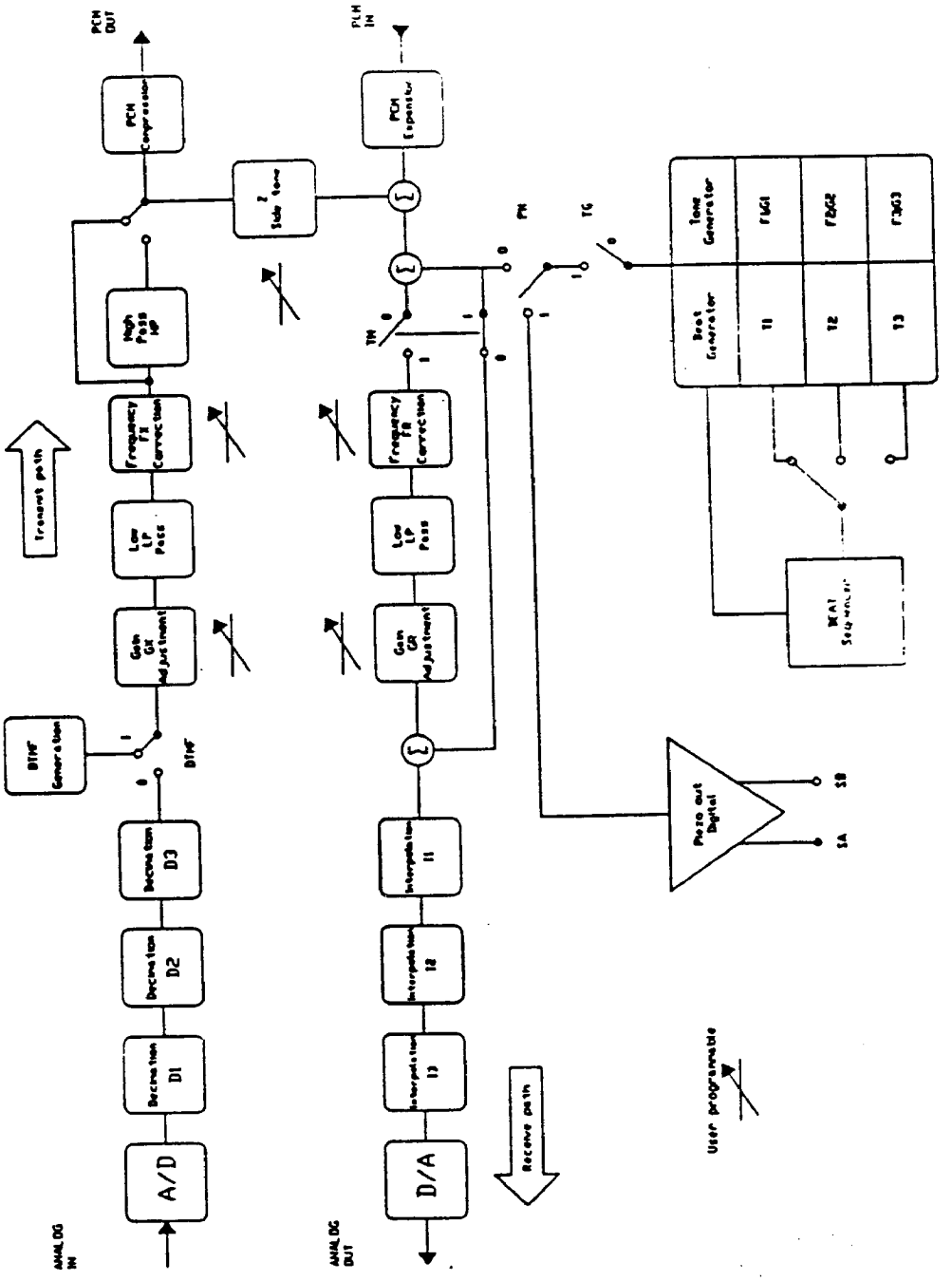


Figure 5.1:

5.2.2. ATTENUATION DISTORTION IN TRANSMIT DIRECTION

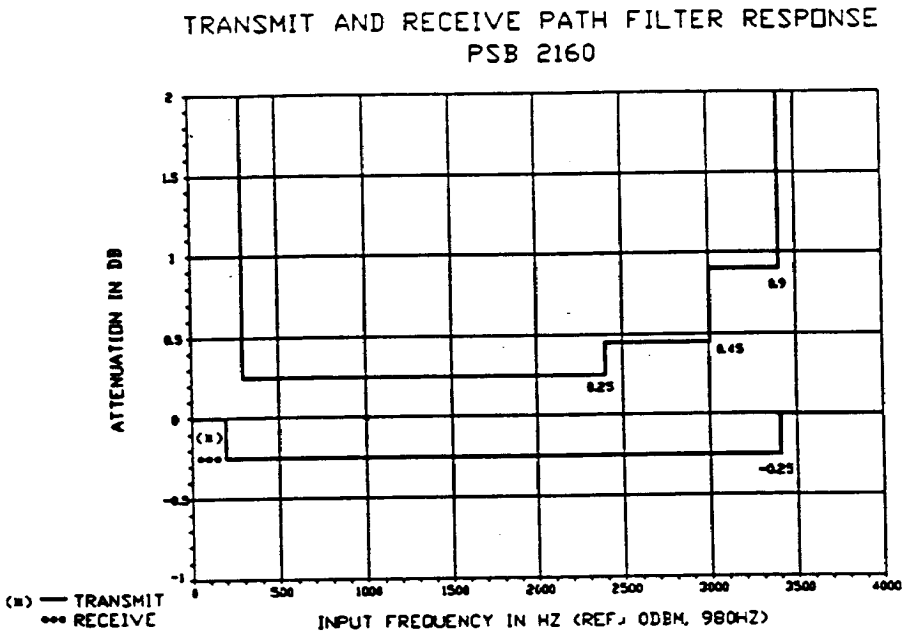


Figure 5.2:

5.2.3. GROUP DELAY DISTORTION IN TRANSMIT DIRECTION

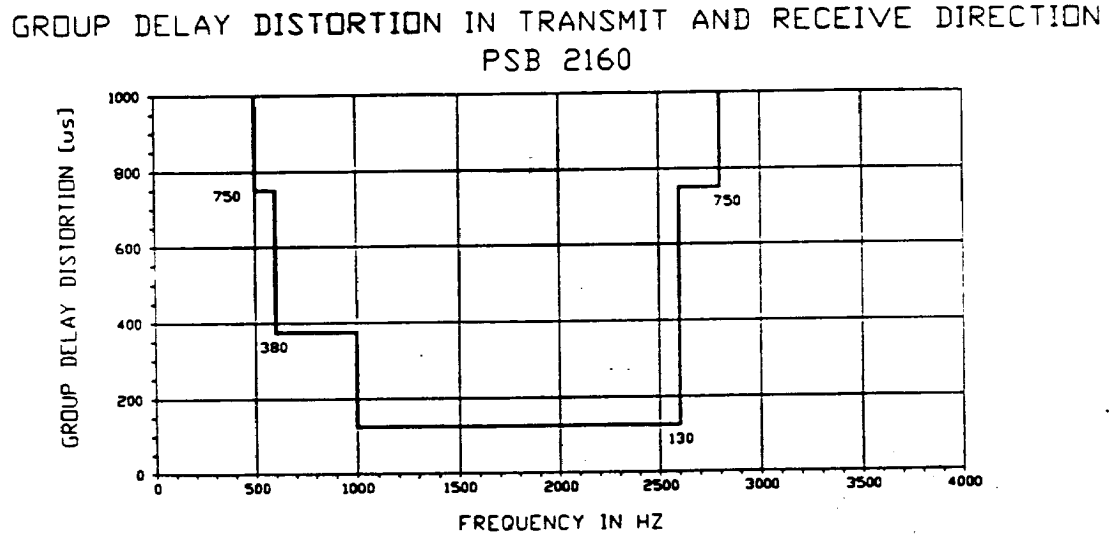


Figure 5.3:

5.2.4. TRANSMISSION CHARACTERISTICS (TABLE 5.1)

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNITS
Attenuation relative to a -10dBmO 1020Hz signal	<200Hz 200-300Hz 300-2400Hz 2400-3000Hz 3000-3400Hz >3400Hz	0 -0.25 -0.25 -0.25 -0.25 0		 0.25 0.45 0.9 	dB dB dB dB dB dB
Envelope 1) delay distortion @ 0dBmO	500-600Hz 600-1000Hz 1000-2600Hz 2600-2800Hz			750 380 130 750	µs µs µs µs
Gain tracking method 2	+3 to -40 dBmO -40 to -50 dBmO -50 to -55 dBmO	-0.3 -0.6 -1.6		0.3 0.6 1.6	dB dB dB
Quantization distortion method 2	0 to -30 dBmO -40 dBmO -45 dBmO	35 29 24			dB dB dB
Idle channel noise	Receiver Transmitter			-75 -66	dBmO dBmO
Crosstalk between Transmitter & Receiver	Reference level = 0dBmO (300-3400 Hz)	-66			dB
Absolute gain	Relative to dBmO in BYP-mode AFE-mode transmit 2) AFE-mode receive 2)	-0.4 -1 -1.5	0 -0.3 -0.6	+0.4 +1 +1.5	dB dB dB

1) Delay measurements include delays through the A/D with all features filters FX,GX disabled.

2) Only for specified gain levels. Indeed 50 Ω loudspeakers can provocate violation of this specified absolute gain.

Table 5.1:

5.2.5. OUT-OF-BAND SIGNALS AT ANALOG INPUTS

When applying an out-of-band sine wave signal with frequency F and level A to the analog inputs the level of any frequency component below 4kHz at the digital output is attenuated according to the following table. The reference level used for this measurement is a 800Hz, 0dBmO signal applied to the FHM analog input in BY-PASS mode. The digital gain GX in configuration register CR1 is set to a flat 0dB.

out-of-band input frequency F	out-of-band input level A	attenuation at digital output
0 Hz ≤ F ≤ 60 Hz	-45 dBmO ≤ A ≤ 0 dBmO	25 dB
60 Hz ≤ F ≤ 100 Hz	-45 dBmO ≤ A ≤ 0 dBmO	10 dB
3400 Hz ≤ F ≤ 4000 Hz	-45 dBmO ≤ A ≤ 0 dBmO	0 dB
4000 Hz ≤ F ≤ 4600 Hz	-45 dBmO ≤ A ≤ 0 dBmO	14 dB
4600 Hz ≤ F ≤ 12 kHz	-45 dBmO ≤ A ≤ -15.8 dBmO	35 dB
12 kHz ≤ F ≤ 20 kHz	-45 dBmO ≤ A ≤ -23.2 dBmO	35 dB
20 kHz ≤ F	-45 dBmO ≤ A ≤ -25 dBmO	35 dB

Table 5.2:

5.2.6. DTMF GENERATOR

A DTMF generator is also built into the ARCOFI® transmit path. The DTMF generator is programmed by a COP command (see section 6. ADI). Two frequency values for the dual tones must be written into the coefficient RAM (COP_8 + 2 bytes) before activating the DTMF generator through a SOP_7 command (CR4, bit 6). The signal amplitude is programmed via the GX gain coefficient (COP_2 + 2 bytes)

A pre-emphasis of 2 dB is guaranteed between the high and the low DTMF frequency groups. The total power level of all unwanted frequency components is at least 20 dB below the level of the low frequency group component of the signal.

The level of any unwanted frequency component does not exceed the following limits:

In the frequency band 0-300 Hz: > -33 dB

In the frequency band 300-3400 Hz : > -20 dB

In the frequency band 3400-4000 Hz : > -33 dB

All generated DTMF frequencies are guaranteed within a +/- 1% deviation. A typical DTMF programming sequence is highlighted in Fig 5.4.

DTMF FREQUENCY PROGRAMMING

CCITT Q.23	ARCOFI® NOMINAL	RELATIVE DEVIATION FROM CCITT *	HEX COEFFICIENT H nibble/L nibble
Low Group			
697	697.754	+ 1 081 ppm	F8
770	773.438	+ 4 464 ppm	A8
852	852.783	- 513 ppm	F9
941	939.453	- 1 646 ppm	BA
High group			
1 209	1 203.125	- 4 883 ppm	21
1 336	1 339.844	+ 2 877 ppm	40
1 477	1 476.563	- 295 ppm	10
1 633	1 632.813	- 114 ppm	00

*) The deviations due to the inaccuracy of the incoming clock CLK, when added to the nominal deviations tabulated above give the total absolute deviation from the CCITT recommended frequencies.

Table 5.3:

ex: To send the DTMF pair 770Hz + 1477Hz, the following COP sequence has to be generated by the μP

COP_8 + C1 + C2

h08 h10 hA8

The DTMF signals of the high frequency group are programmed by default to generate a - 2.2 dBmO PCM level for a 0 dB GX gain setting.

5.2.7. DTMF PROGRAMMING SEQUENCE (FIG 5.4)

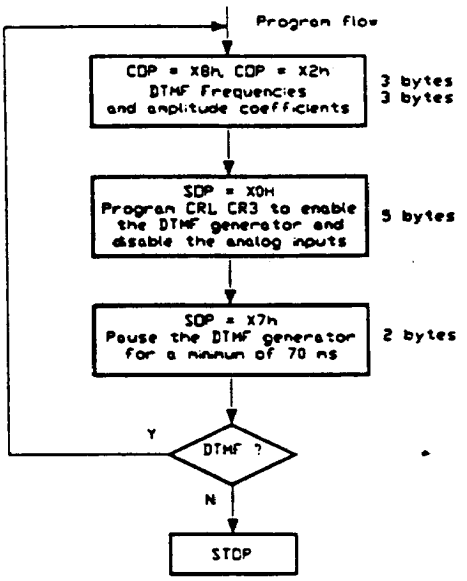


Figure 5.4:

5.3. RECEIVE PATH SIGNAL PROCESSING

In the receive path the incoming PCM signal is expanded into a linear code according to the selected A-Law or μ-Law. If the linear mode is chosen, the PCM expander circuit is by-passed and a 16 bit linear word has to be provided to the processor.

A programmable sidetone gain stage Z adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from -50 to -2.5 dB within a +/- 1dB tolerance range (0dB is also possible). On reset the Z gain default value is -18dB.

The FR frequency correction filter is similar to the FX filter allowing an optimum adaptation to different type of loudspeakers and earpieces.

A low pass EWDF filter limits the signal bandwidth in the receive direction according to CCITT recommendations (see Fig. 5.2 and 5.3). The GR gain adjustment stage is digitally programmable from -45dB to +12dB within a 0.25dB tolerance range. The CCITT templates

are guaranteed in the area -8dB to 0d3. Two bytes are coded in the CRAM to set GR to the desired value. On reset the initial GR setting is 0dB. A series of low pass interpolation filters increases the sampling frequency up to 128kHz. The last interpolator feeds the D/A converter.

5.3.1. TONE RING AND TONE GENERATOR

The ASP receive path contains two signal generators; a tone ring and a beat tone generator (TG & BT). Those generators can be used for tone alerting, call progress tones or other audible feedback tones. All generated tones can be provided at either the handset earpiece, the loudspeaker output or the piezo ringer output (SA & SB).

Distinctive alerting signals, allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjunction with the tone ringer. In the case of a two or three tone ringing signal, the tone ring generator controls the output frequency pitch whilst the beat tone generator controls the repetition rate.

Examples of the complex pattern involving the repetition of multifrequency signals with different duty cycles are shown in table 5.4 Tones can be superimposed on the incoming voice signal or can be output separately to the piezo ringer output. The tones can also be low passed or directly applied as a square wave to the D/A output. The tone generators can be programmed to specify frequencies, amplitudes and repetition rates through a COP command. Two bytes in the CRAM are necessary to set the frequency. An additional byte is necessary to set the amplitude and two bytes are required for the timing rate.

Five distinctive bits in configuration register 4 (CR4) control the ARCOFI® tone generator. The tone generator TG and beat tone BT bits enable or disable the generators. Tone mode bit TM selects or deselects the mixing of voice and tones. Piezo mode bit PM selects to which output the tone will go: piezo output (pins SA & SB) or D/A. The piezo outputs amplitude is not variable. Fixed digital level signals are generated at the SA & SB pins. Beat mode bit BM selects a two or a three tone ring signal pattern.

Either a square wave or trapezoidal shaped tones can be generated depending on the TM bit setting (TM = 0; square, TM = 1; trapeze). Tones superimposed on voice are generated as trapezoidal waves, all other tones are generated as square wave. Different coefficients are required to produce the same frequency signal in a square or trapezoidal form.

5.3.2. TONE PATTERN EXAMPLES (TABLE 5.2)

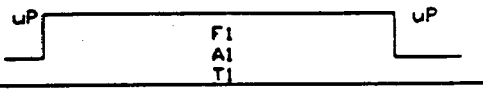
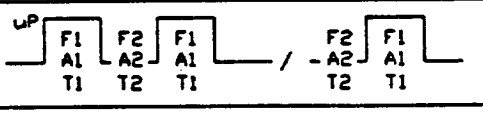
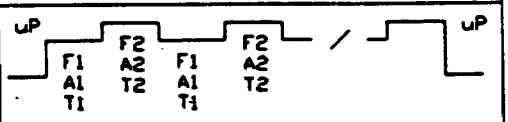
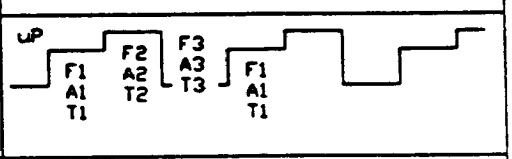
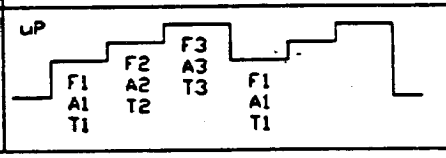
Name	CR1,CR2	Coefficient range	Pattern
Constant single Tone	TG = 1 BT = 0 BM = 0	F1: 0 to 4000 Hz A1: - ∞ to 0 dB T1: 5ms to 16 s	
Cycled single tone	TG = 1 BT = 1 BM = 0	F1;F2; 0 to 4000 Hz A1;A2; - ∞ to 0 dB T1;T2; 1ms to 16.4 s F2:0 A2:x	
Cycled two tones without pauses	TG = 1 BT = 1 BM = 0	F1;F2; 6.5 to 3600 Hz A1;A2; - 50 to 0 dB T1;T2; 1ms to 16.4 s	
Cycled two tones with pauses	TG = 1 BT = 1 BM = 1	F1;F2; 0 to 4000 Hz A1;A2; - ∞ to 0 dB T1;T2;T3; 1 ms to 16.4 s F3: 0 Hz A3: x	
Cycled three tones without pauses	TG = 1 BT = 1 BM = 1	F1;F2;F3; 6.5 to 3600 Hz A1;A2;A3; - 50 to 0 dB T1;T2;T3; 5 ms to 16 s	

Table 5.4:

F1 : first frequency coefficient
A1 : first amplitude coefficient
T1 : first Beat generator timing coefficient
x : don't care
µP : microprocessor intervention through COP & SOP commands

TONE BIT PROGRAMMING

TG	TM	PM	Speech path	Tone generator	Analog out	piezo out
0	0	0	no	no	DC 0V	PCI
0	0	1	no	no	DC 0V	const
0	1	0	yes	no	Speech	PCI
0	1	1	yes	no	Speech	const
1	0	0	no	square	square	PCI
1	0	1	no	square	DC 0V	square
1	1	0	yes	trapeze	+ Speech	PCI
1	1	1	yes	square	Speech	square

Table 5.5:

BEAT GENERATOR PROGRAMMING (TG = 1)

BT	BM	Tone signal
0	0	Continuous signal F1;G1
0	1	Continuous signal F2;G2
1	0	Alternating signal F1;G1,T1 F2;G2,T2
1	1	Alternating signal F1;G1,T1 F2;G2,T2 F3;G3,T3

Table 5.6:

5.3.3. GAIN TRACKING IN TRANSMIT DIRECTION METHOD 2; SINUS (FIG 5.9)

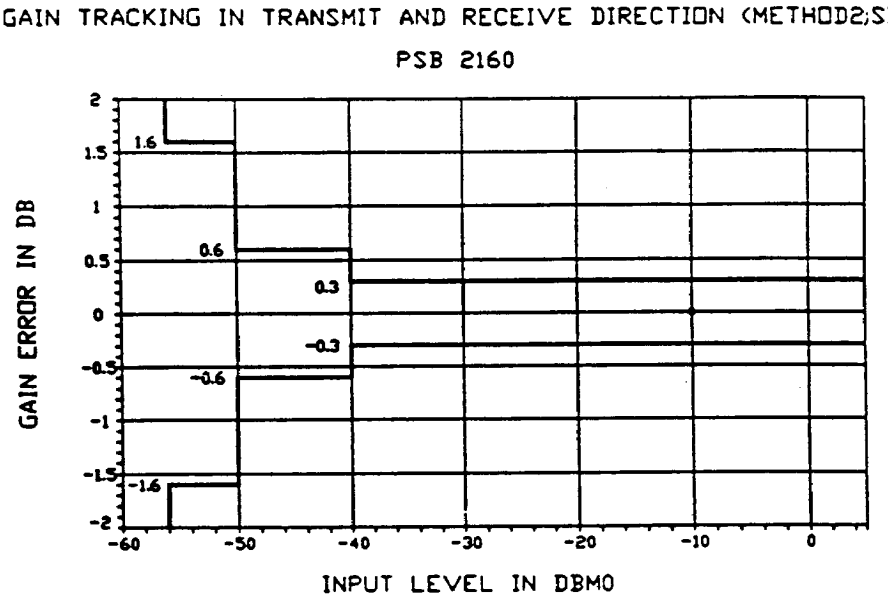


Figure 5.5:

5.3.4. TOTAL DISTORTION METHOD 2; SINUS

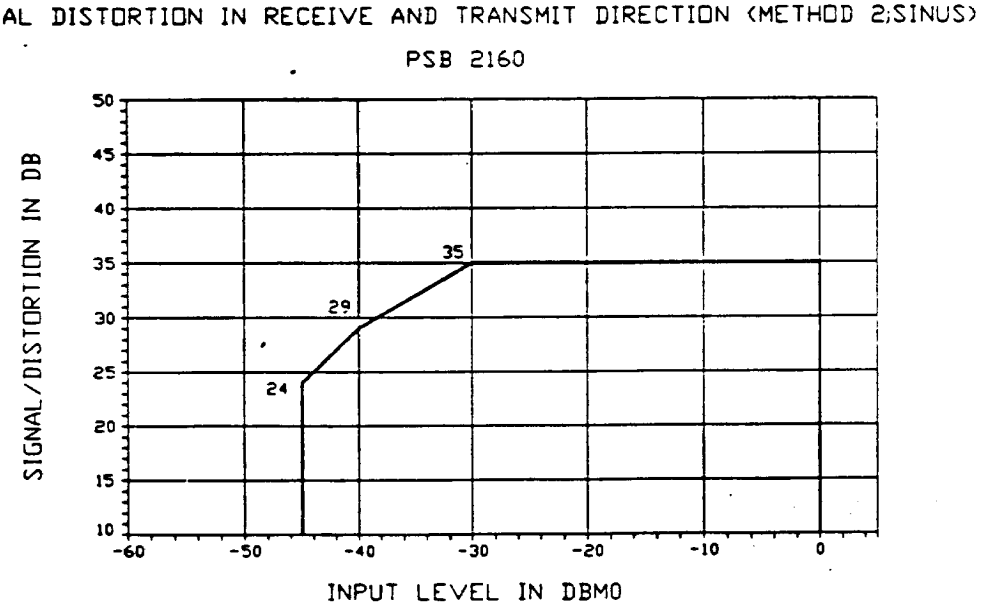


Figure 5.6:

6. ARCOFI® DIGITAL INTERFACES (ADI)

The Arcofi Digital Interface section consists of a serial interface bus which can be configured to be compatible to the SLD or the IOM®2 standard, and a set of four programmable I/O pins grouped as a Peripheral Control Interface (PCI).

6.1. IOM®2 INTERFACE

The IOM®2 interface consists of two data lines and two clock lines. DU: Data Upstream carries data from the ARCOFI® to the layer 1 device and DD: Data Down stream carries data from the layer 1 device to the ARCOFI®. A FSC frame synchronization clock is supplied to the ARCOFI® as well as a DCLK 1.536 MHz data clock for bit clocking.

Selecting between the IOM®2 and the SLD interfacing mode is performed by strapping pins SP1 & SP2 according to the pin strapping function table 6.1 (paragraph 6.3.2).

The ARCOFI® implements all IOM®2 terminal functions spelled out in the IOM®2 interface specification.

In terminal mode the IOM®2 frame consists of three IOM®2 channels numbered respectively 0,1 and 2. The ARCOFI® can receive and transmit voice data in the IOM®2 B1 & B2 channels as well as in the IC1 and IC2 intercommunication channels located in IOM®2 channels 0 and 1 respectively. The voice/data channel allocation is programmable via the ARCOFI® IOM®2 channel select bit SEL in CR2. B1 or B2 resp. IC1 or IC2 can be programmed by use of the RCS bit in the CMDR register.

The IC1 and IC2 intercommunication channels can be used in the terminal for local data communication. This makes post-processing of voice/data information possible (see figure 6.1).

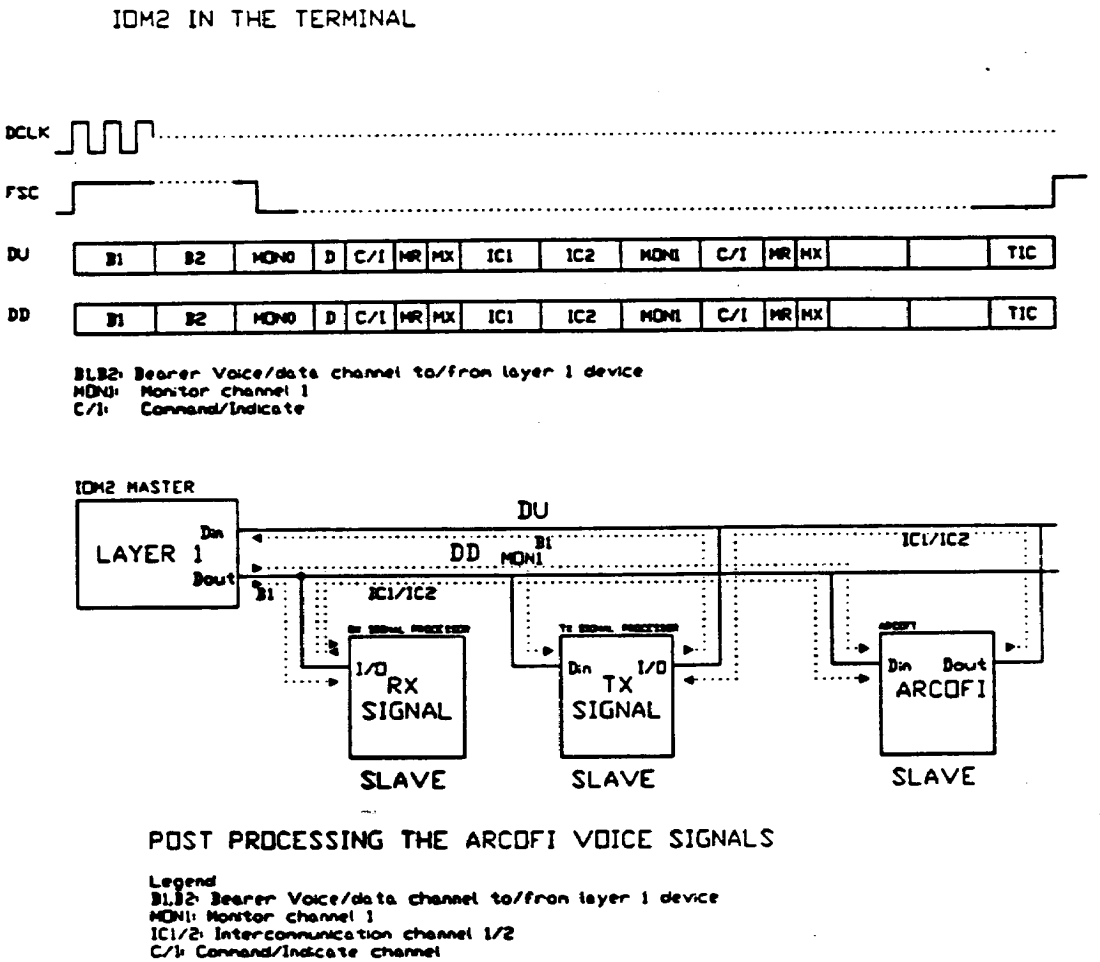


Figure 6.1:

6.1.2. THE IOM®2 MONITOR CHANNEL

All programming data required by the ARCOFI® including coefficients are transmitted exclusively in the monitor 1 time slot in the IOM®2 channel 1. The MON1 monitor channel allows a point to multi-point access where the layer 1 component acts as the master to programmable devices like the ARCOFI®. Each programmable device is accessed by sending a specific address byte at the start of each SOP or COP command stream. The programmable device compares the received address byte with its own SP1 wire strapped IOM®2 address before executing a command. Bit AD in the CMDR must be consistent with the SP1 pin hardware strap.

6.1.3. IOM®2 IDENTIFICATION

The ARCOFI® responds to the following DD identification sequence by sending a DU identification sequence:

DD 1st value	101X	0000
DD 2nd value	0000	0000

DU 1st value	101X	0000
DU 2nd value	10	DESIGN

X: **logical 0** (active low): SP1 = 0; AD = 0
Logical 1 (passive high): SP1 = 1; AD = 1

DESIGN: between 00h and 0Fh; indicates software compatibility between ARCOFI® versions

6.1.4. IOM®2 FEATURE COMMAND SEQUENCE

An ARCOFI® **programming sequence** is characterized by a 1 being sent in the LSB nibble of the first incoming **identification code.**

All programmed **coefficients can be read back** when issuing an appropriate CMDR read (CMDR; R/W = 1). **The** ARCOFI® **responds by** sending an IOM®2 specific address byte identifying the chip **followed by the requested data.**

	Write sequence
DD 1st value	101X 0001
DD 2nd value	COP , SOP_X
DD 3rd value	DATA byte_1
DD nth value	DATA byte_n

	Read
DU 1st value	101X 0001
DU 2nd value	DATA byte_1
DU nth value	DATA byte_n

(*) Remark : Only after the addressing code (101X 0001) it is possible to change the AD and RCS bits in the CMDR register (COP, SOP).

6.1.5. MONITOR TRANSFER PROTOCOL

The transfer of a stream of commands in the MON1 channel is regulated by a handshake protocol mechanism implemented by two bits MX and MR in the fourth slot of the IOM®2 channel 1.

The maximum effective transfer rate in the MON1 channel is 32 kb/s. Thanks to the implemented handshake mechanism a command sequence can be delayed at the convenience of the transmitting IOM®2 bus master device and resumed subsequently.

An abort mechanism allows the interruption of a command sequence. In that case the command may be partially executed by the ARCOFI® (i.e coefficients partially modified in the ARCOFI® CRAM). If use of the abort mechanism is made, a new command has to be issued to program the ARCOFI®. The handshake mechanism is explained below.

Handshake by maximum speed.

IOM® frame	1 DD_CH1:	MX = 0 ; DU_CH1: MR = 1 ;1st MON1 byte
" "	2 DD_CH1:	MX = 0 ; DU_CH1: MR = 0 ;byte acknowledge
" "	3 DD_CH1:	MX = 1 ; DU_CH1: MR = 0 ;2nd MON1 byte
" "	4 DD_CH1:	MX = 0 ; DU_CH1: MR = 1 ;
.....		
" "	n DD_CH1:	MX = 1 ; DU_CH1: MR = 0 ;nth MON1 byte + ACK
" "	n+1 DU_CH1:	MX = 0 ; DU_CH1: MR = 1 ;nth byte ACK
" "	n+2 DD_CH1:	MX = 1 ; DU_CH1: MR = 0 ;
" "	n+3 DU_CH1:	MX = 1 ; DU_CH1: MR = 1 ;EOM

1st & 2nd MON1 bytes received contain the ARCOFI® specific IOM®2 address.

EOM: End Of Transmission

MX,MR active low = 0

MX,MR passive high = 1

6.1.6. MONITOR TRANSFER PROTOCOL RULES:

MX and MR inactive (MX,MR = Z) for two or more consecutive frames indicates an idle state or an end of transmission (EOM).

A command stream initiated by a transmitter in the monitor MON1 slot is accompanied by an activated downstream MX bit (DD_MX = 0).

The receiver acknowledges a received byte by toggling the upstream MR bit (DU_MR = 0) from inactive to active in the subsequent IOM®2 frame for at least one frame.

The transmitter indicates a new byte in the monitor channel by the transition of the DD_MX bit from the active to the inactive state. The DD_MX bit returns to the active state after one frame. Two frames with the DD_MX bit in the inactive state indicate the end of transmission. The receiver acknowledges each new byte by a similar one frame transition of the DU_MR bit to the inactive state. Two frames with the DU_MR bit set to inactive indicate a receiver request for abort.

The transmitter can delay a transmission sequence by sending the same byte continuously. In that case the MX bit remains active in the IOM®2 frame following the first byte occurrence.

Delaying a transmission sequence is only possible while the receiver MR bit and the transmitter MX bit are active.

6.1.7. THE C/I CHANNEL

The C/I channel bits are represented so that the first bit transmitted/received appears on the left. The data presented to the four peripheral control interface (PCI) pins SA to SD are transparently routed to the C/I IOM®2 channel 1. Pins SA-SD can be configured individually as input or output and will appear respectively in the DD or DU CH1-C/I channel.

The mapping of the peripheral control interface (PCI) pins SA,SB,SC,SD into the six C/I channel bits depends on the hardwired SP1 address as follows:

SP1 = 1

DD and DU	–	–	SB	SA	SD	SC	–	–

SP1 = 0 (AM = 0; two chip mode)

DD and DU	SD	SC	–	–	–	–	–	–

The ARCOFI® with the address pin SP1 strapped to 0 transmits/receives the SD and SC values on DU/DD

SP1 = 0 (AM = 1; one chip mode)

DD and DU	SD	SC	SB	SA	-	-	-	-

In case a reset has been asserted, the SA to SD pins are programmed as input, however the SA to SD values are not switched to the C/I channel unless a CR1 to CR4 SOP_0 write command is issued.

6.2. SLD INTERFACE

The SLD Serial interface consists of a bidirectional data line SIP, a synchronization clock input CLK and a data direction input FSC. Data bits are loaded or read out of the serial interface pin SIP under control of a direction signal FSC. Bits are clocked in on the falling edge and clocked out on the rising edge of the slave clock pin CLK (512kHz). FSC and CLK inputs must be phase locked.

A SLD frame lasts 125 µs and consists of 32 bits transferred to the ARCOFI® (FSC high) followed by 32 bits transferred from the ARCOFI® to the SLD bus (FSC low).

The SLD interface thus provides a full duplex 256kb/s communication capacity. This capacity is subdivided in two 64kb/s voice/data channels reserved for the ISDN B1 and B2 channels. The remaining bandwidth is used by a feature control channel (64kb/s) and a signalling channel (64kb/s). Bytes in all channels are serialized MSB first.

A command received over the SLD bus can cause a response over the SLD bus within the same frame. This leaves the ARCOFI® 31.25 µs to interpret the command and generate the appropriate answer in the following half-frame TX command channel.

All ARCOFI® internal registers are accessible via the SLD bus in the time slot allocated to the feature control channel. The first byte transferred in the feature control channel specifies the type of operation and the number of bytes allocated to the transfer set-up according to the coding table described in the section "Command Register". In a multiple byte transfer the ARCOFI® address register points to the first location implied in the command register bit field CB0-CB3. Following bytes transfer in successively higher order locations.

When in power down (PU = 0 ;CMDR), the command channel remains active in both transmit and receive direction providing that the address bit (AD ;CMDR) matches the address strapped on SP1,SP2(see supplementary functions). In power down however both data channels are disabled; SIP being tristated during data channel transmit time slots.

If the linear mode is selected (LIO 2 = 1,0 ;CR3) a full linear 16 bits word is transmitted or received in the data channels B1 & B2.

If mixed mode is selected (LIO 1 = 0,1 ;CR3) a full linear 16 bits word is transmitted in the TX-FC & TX-SIG channels. This option is available only if ELS = 0 in CR2.

6.2.1. SLD Bus (FIG 6.2)

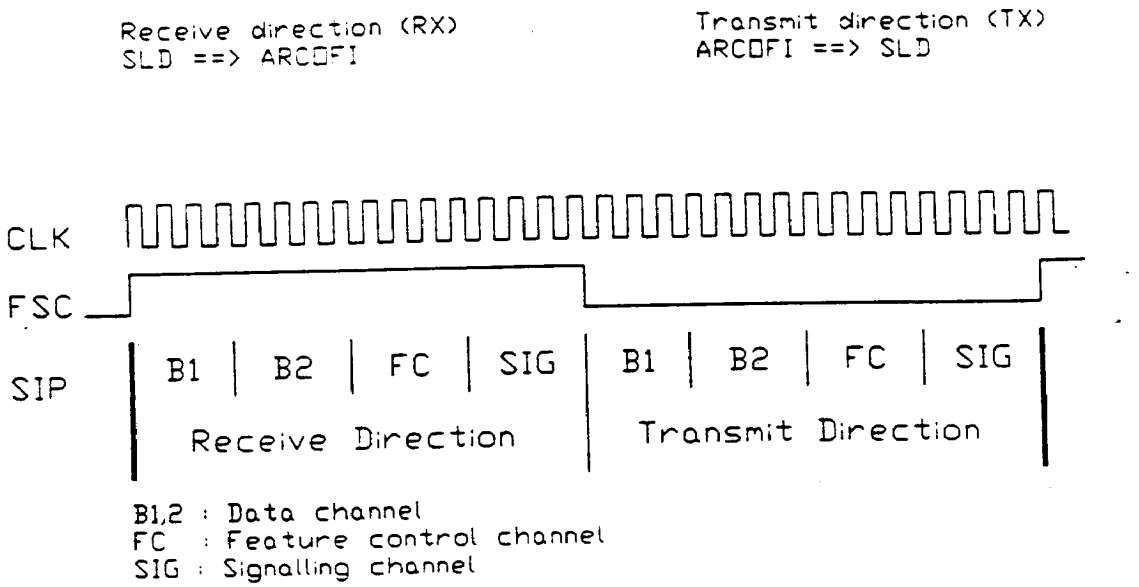


Figure 6.2:

6.2.2. SLD BUS CONTENTION RESOLUTION

When connecting more than one device to the SLD bus, the access to the Transmit Bearer, Feature Control and Signalling channels has to be managed so as to avoid contention on the SIP line. Each individual channel will be considered separately and the proper configuration bit set-up when accessing a particular channel will be described.

6.2.3. BEARER/DATA CHANNEL CONTENTION RESOLUTION

Contention may arise in the Bearer channels TX-B1 and TX-B2 if two devices connected to the SIP line try to access these channels simultaneously.

When powered down (PU = 0 ; CMDR) both data channels are ignored (TX-B1 & TX-B2 tristated). When activated (PU = 1 in CMDR) only one channel is active according to the bit setting in the CMDR (RCS = 1; RX & TX-B2 active. RCS = 0; RX & TX-B1 active), the other Bearer/Data channel is tristated if CR2 bit AM = 0, otherwise NOP's are transmitted in the non-selected channel.

If mixed mode is selected (LIO = 0,1 in CR3) both channels are activated, thus no access is allowed from an other SLD connected device. It is up to the user, after a power on reset to properly select the use of the bearer/data channels so as to avoid contention.

When two ARCOFI®'s are connected to the SLD bus, each using a different bearer channel, it is possible to swap channels using the following procedure:

1) command ARCOFI®#1 to power down and SWAP bearer channels

2) command ARCOFI®#2 to SWAP bearer channels

3) command ARCOFI®#1 to power up

The ARCOFI®#1 loses two receive/transmit words when following this procedure.

6.2.4. FEATURE CONTROL CHANNEL CONTENTION RESOLUTION

Contention in the Feature Control (FC) channel when issuing a SOP or COP read command:

If the received SOP or COP command bit AD matches the strapped address on Pin SP1 and SP2, the SIP buffer is activated during the following TX-FX time slots until the entire read sequence has been executed, the SIP buffer returns to tristate thereafter if AM = 0, otherwise NOP's are transmitted.

6.2.5. SIGNALLING CHANNEL CONTENTION RESOLUTION

When two or more devices share the TX-SIG channel, care must be taken to avoid collision. When the ELS & AM bits are set to one in CR2, the SA - SD pins which are not programmed as TX-SIG inputs are tristated. Depending on the programming of AM & ELS, the TX-SIG bits which are not defined as inputs are transmitted as 0 or are tristated (see 6.3.6 signalling channel bit allocation table).

6.3. ARCOFI® PERIPHERAL CONTROL INTERFACE (PCI)

The ARCOFI® Peripheral Control Interface (PCI) consists of 6 pins; 4 pins SA to SD are used as a peripheral control port and can be programmed individually as inputs or outputs.

The remaining two pins SP1 and SP2 are used to address the device and to implement supplementary functions.

6.3.1. PCI PINOUT DESCRIPTION

The ARCOFI® communicates with the terminal equipment microcontroller through either the SLD or the IOM®2 bus.

In the SLD interfacing mode all internal registers including the coefficient RAM are solely accessible using the command register as an address pointer. The signalling channel is transparent to the ARCOFI® and is routed to the four SA-SD pins.This allows SA-SD to be used as peripheral control interface lines.

Pins SA-SD can be configured individually as inputs or outputs. A quarter of the total available

signalling channel bandwidth is routed this way to the PCI port, the remaining signalling channel capacity can be made available through the use of an expansion option.

6.3.2. SUPPLEMENTARY FUNCTION TABLE

Supplementary functions are accessed by strapping pins SP1 and SP2 according to the following table:

Pin SP1	Pin SP2	Chip Address	PLL/ EXT	Mode sel SLD/IOM	Description
-1	0	x			
-1	-1	x	EXT	SLD fast	TEST mode 1
-1	1	x	PLL	SLD fast	TEST mode 2
0	1	AD = 0	PLL	SLD slow	PLL circ. enabled the SLD transfer
1	1	AD = 1	PLL	SLD slow	rate is CLK 1)
0	0	AD = 0	PLL	IOM2	PLL circuit is enabled, the IOM rate
1	0	AD = 1	PLL	IOM2	is 1.536 MHz 2)
0	-1	AD = 0	EXT	SLD fast	PLL circuit is bypassed, SLD rate is
1	-1	AD = 1	EXT	SLD fast	the internal master clock CLK

-1 = -5 Volts (VSS) ; 1 = 5 Volts (VDD) ; 0 = 0 Volt(GNDD)

1) When powered down (PU = 0 in CMDR) both data channels are also ignored (TX-B1 & B2 high-Z). Thus the SLD-bus is free for external device access.

2) Release A1&A2 of the ARCOFI® does not implement the IOM®2 mode but instead the PLL circuit is by-passed with an SLD transfer rate of CLK/8.

Table 6.1:

6.3.3. SLD TRANSFER RATE MODE

The ARCOFI® operates either from an on chip generated 4.096MHz master clock derived by an internal PLL circuit supplied from the 512 kHz slave clock CLK (PLL on), or the PLL circuit is by-passed and the internal master clock rate equals the externally supplied clock on pin CLK (EXT).

Two data transfer modes are possible on the SLD-Bus: a "slow mode" (512 kHz slave clock or frequency of the external CLK when the PLL is on) and a "fast mode" (internal master clock rate or CLK when the PLL is by-passed).

The selection of the supplied clock and the SLD clock rate is made via Pins SP1, SP2 as listed in the preceding supplementary function table.

In "fast mode" 8 or 16 bits are transferred depending on the programmed I/O mode (CR3: Bits LIO).

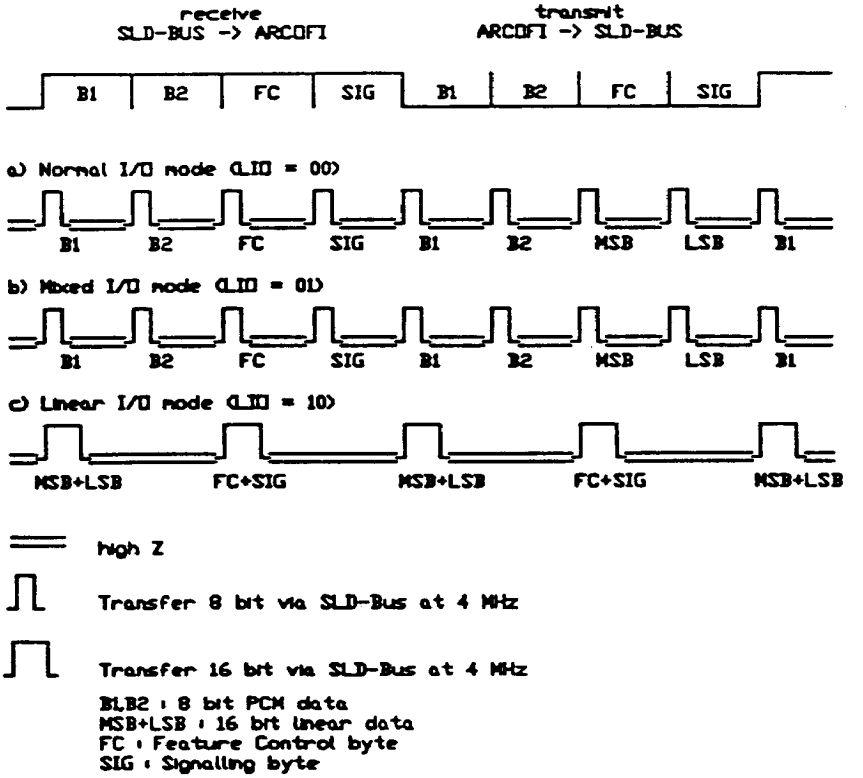


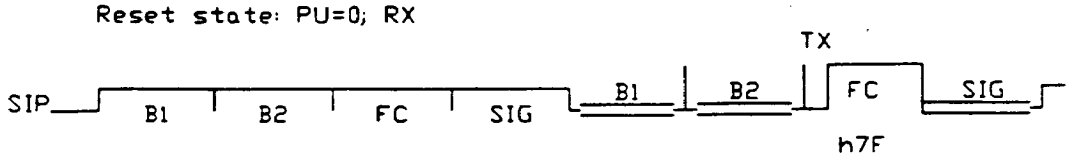
Figure 6.3:

During the processing of a COP or SOP read instruction the ARCOFI® sends Feature Control and signalling Bytes. During COP or SOP write,NOP's are sent back.

6.3.4. ARCOFI® RESET FLAG

A reset flag "R" monitors the reset pin of the ARCOFI®. When a reset is asserted the R flag is cleared. This is indicated by bit 7 being set to 0 during TX-FX NOP time slots (7F hex is transmitted instead of the normal NOP's FF hex). Flag R can be set to one by performing a CR4 to CR1 SOP_0 write operation. All configuration registers are cleared after a reset has been asserted and need to be reconfigured anyway.

So as to read out the status of the R flag the TX-FX channel has to be activated as described in section 6.2.4, Feature Control channel contention resolution.



6.3.5. EXPANSION OPTION

To fully use the signalling channel bandwidth capacity an expansion option has been devised. If the ELS bit in the configuration register CR2 has been set to 1 the expansion option is considered to be connected. In the receive direction, the PCI pins SA-SD which have been programmed as outputs receive data from the corresponding bits in the RX-SIG channel. Remaining bits can thus be allocated to a second device connected to the SLD bus. In the transmit direction, the PCI pins which have been connected as inputs transfer data in the corresponding bits of the TX-SIG channel. During the remaining bits transfer SIP is tristated allowing a second device on the SLD bus to transfer PCI data. The ELS option is independent from the address bit setting (AD,bit 7) in CMDR. The user must consequently program the PCI pins to avoid contention on the SLD bus.

6.3.6. SIGNALLING CHANNEL BIT ALLOCATION TABLE

RECEIVE-SIG	TRANSMIT-SIG	CONFIGURATION		
76543210	76543210	AM	ELS	CASE
XXXXXXXX	SSSS DCBA0000	1	0	one chip
XXXXXXXX	SSSS DCBAZZZZ	1	1	PCI pins as INPUTS
SSSS DCBAXXXX	00000000	1	0	one chip
SSSS DCBAXXXX	ZZZZZZZZ	1	1	PCI pins as OUTPUTS
1# XXXXXXXX	SSSS DCBAZZZZ	0	1	two chips
2# XXXXXXXX	SSSS ZZZZDCBA	0	1	PCI pins as INPUTS
SSSS 1# DCBAXXXX	0000ZZZZ	0	0	two chips
SSSS 2# XXXXDCBA	ZZZZ0000	0	0	PCI pins as OUTPUTS
SS 1# XXBAXXXX	SS DC00ZZZZ	0	0	two chips
SS 2# XXXXDCXX	SS ZZZZ00BA	0	0	PCI pins IN & OUT

X: don't care
Z: tri-state

ARCOFI® EXPANSION OPTION USE EXAMPLE

ARCOFI® #1 PCI pins SA & SB are configured as outputs, the remaining pins as inputs.

ARCOFI® #2 PCI pins SC & SD are configured as outputs, the remaining pins as inputs.

According to this selection a quarter of the PCI channel capacity is directed to ARCOFI® #1, an other quarter is directed to ARCOFI® #2. The following timing diagram indicates where the allocated bits are transferred.

The following bits are defined in the CMDR and CR registers.

ARCOFI® #1 : AD = 0; AM = 0; RCS = 1; ELS = 0; TR = 0; (EFC = 1)

ARCOFI® #2 : AD = 1; AM = 0; RCS = 1; ELS = 0; TR = 0; (EFC = 0)

Time slot	t0			
Transfer direction	RX ARCOFI®#1	RX ARCOFI®#2	TX ARCOFI®#1	TX ARCOFI®#2
CH - B1	X	B1/7-B1/0	SIP high Z	B1/7-B1/0
CH - B2	B2/7-B2/0	X	B2/7-B2/0	SIP high Z
FC - CH	AD = 0 CMD 7-0	X	AD = 0 CMDR 7-0	SIP high Z
SIG - CH	rest is X	rest is X	rest SIP high Z	rest SIP high Z

X: don't care

6.3.7. SLD EXPANSION OPTION (FIG 6.3)

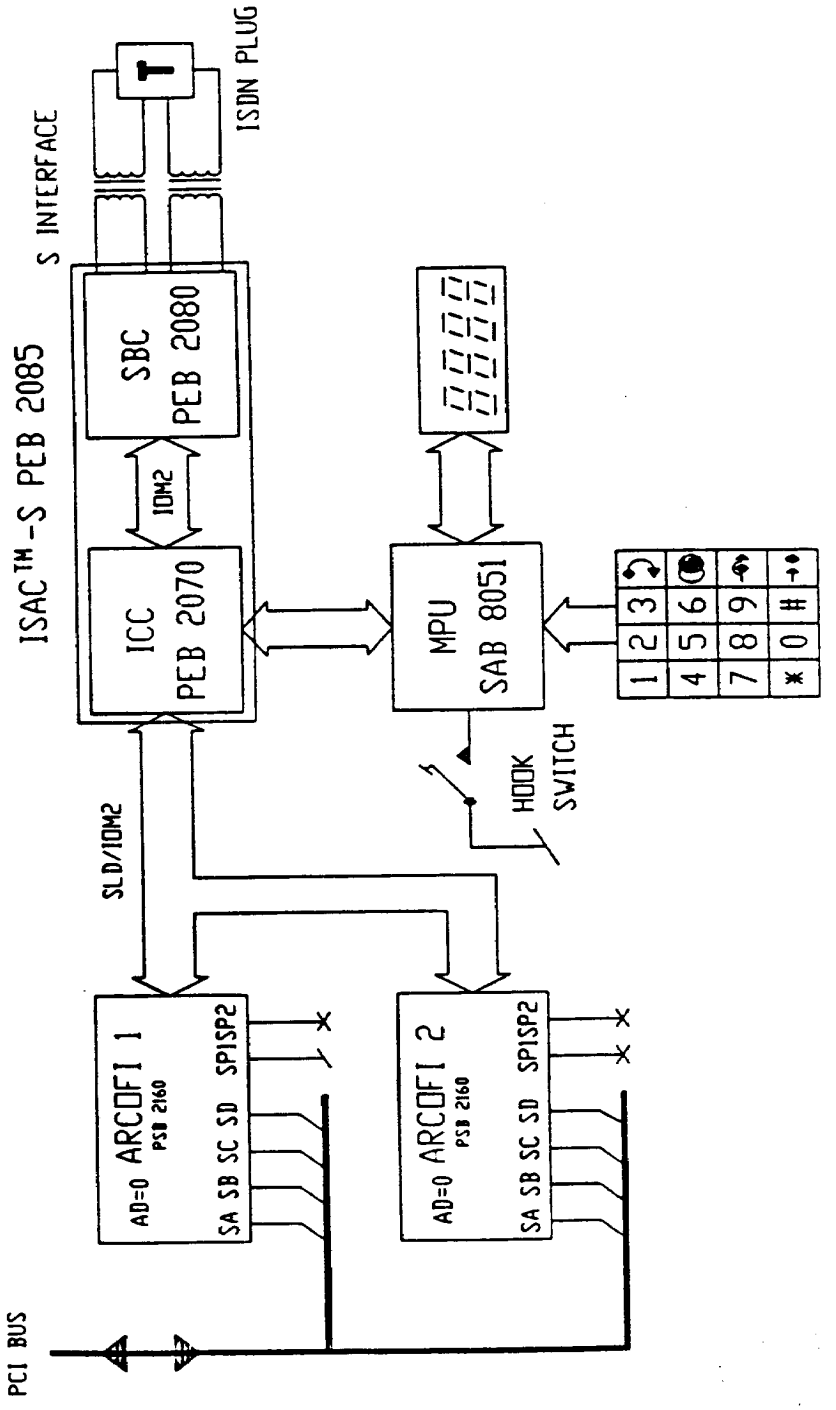


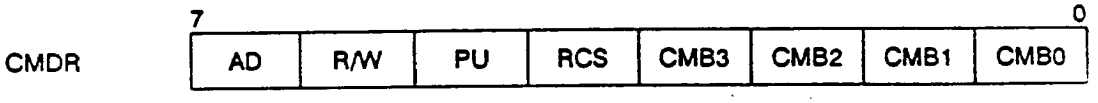
Figure 6.4:

6.4. ARCOFI® INTERNAL REGISTER DESCRIPTION

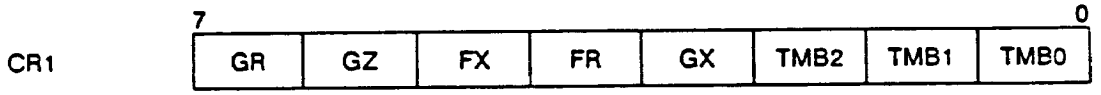
The following describes the various ARCOFI® registers and coefficient RAM locations accessible from the terminal equipment microcontroller via the SLD bus.

A summary of the 5 registers located in the ADI block is presented below followed by a detailed description of the register content.

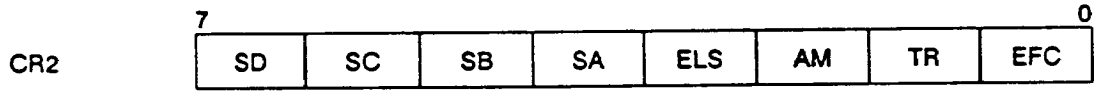
Command register (CMDR)



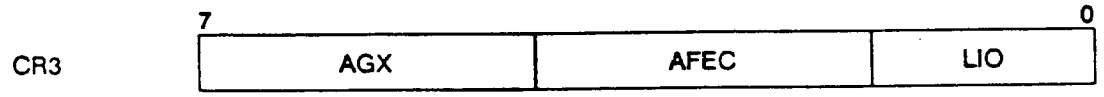
Configuration register 1 (CR1)



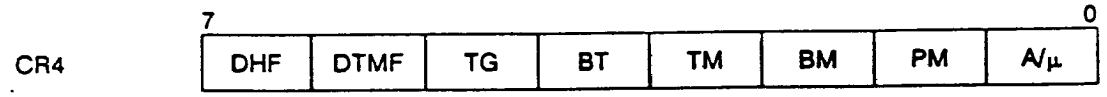
Configuration register 2 (CR2)



Configuration register 3 (CR3)



Configuration register 4 (CR4)



6.4.1. COMMAND REGISTER (CMDR)

	Logical 1	Logical 0
BIT 7	AD = 1; if bit AD matches the address convention . strapped on SP1; pin SIP is active as output during SLD-TX slots	AD = 0; if address bit is not consistent with the logical level strapped on SP1; SIP is tristated during SLD transmit time slots
BIT 6	R/W = 1; reading from CR1, CR2, CR3, CR4 or CRAM	R/W = 0; writing to CR1, CR2, CR3, CR4 or CRAM
BIT 5	PU = 1; The ARCOFI is in a normal operating mode (powered up)	PU = 0; The ARCOFI is placed in stand by (powered down). All register contents are saved
BIT 4	RCS = 1; receive and transmit in CH-B2 (see SLD bus description).	RCS = 0; receive and transmit in CH-B1.

Note: RCS versus AM bit

In case of one chip mode (AM = 1) RSC operates as described above.

In case of two chip mode (AM = 0), if pin SP1 is strapped to 0 same as above. If SP1 is strapped to 1, RCS operates in reverse order:

RCS = 1 RX and TX in channel B1

RCS = 0 RX and TX in channel B2

A full sequence consists of a command byte followed by ..n byte coefficients.

BIT 3 2 1 0	CMD NAME	STATUS MODE	CMD SEQ. LEN.	CMD SEQUENCE DESCRIPTION	;COMMENTS
0 0 0 0	SOP_0	R/W	5	<CR4> <CR3> <CR2> <CR1>	;Reset F flag
0 0 0 1	COP_1	R/W	5	<t1> <t1> <f1> <f1>	;Beat tone time span T1 & ;tone generation frequency F1
0 0 1 0	COP_2	R/W	3	<gx1> <gx2>	;GX gain
0 0 1 1	COP_3	R/W	5	<t2> <t2> <f2> <f2>	;Beat tone time span T2 & ;tone generation frequency F2
0 1 0 0	SOP_4	R/W	2	<CR1>	;Configuration register 1
0 1 0 1	SOP_5	R/W	2	<CR2>	;Configuration register 2
0 1 1 0	SOP_6	R/W	2	<CR3>	;Configuration register 3
0 1 1 1	SOP_7	R/W	2	<CR4>	;Configuration register 4
1 0 0 0	COP_8	R/W	3	<dtmf_high> <dtmf_low>	;DTMF frequencies
1 0 0 1	COP_9	R/W	5	<gz> <a3> <a2> <a1>	;GZ gain & tone generator ;amplitudes A1,A2,A3
1 0 1 0	COP_A	R/W	9	<fx1> <fx2> <fx3> <fx4> <fx5> <fx6> <fx7> <fx8>	;FX frequency correction ;coefficient set 1
1 0 1 1	COP_B	R/W	3	<gr1> <gr2>	;GR gain
1 1 0 0	COP_C	R/W	9	<fr1> <fr2> <fr3> <fr4> <fr5> <fr6> <fr7> <fr8>	;FR frequency correction ;coefficient set 1
1 1 0 1	COP_D	R/W	5	<fr9> <fr10> <fx9> <fx10>	;FX & FR coefficient set 2
1 1 1 0	COP_E	R/W	5	<t3> <t3> <f3> <f3>	;Beat tone time span T3 & ;tone generation frequency F3
1 1 1 1	NOP	R		<hff>	;No operation, CMDR ;bits 7,6,5,4 are masked
		W			;No operation, CMDR ;bits 7,6,5,4 can be written

W: ;write
R: ;read
<..> ;mandatory byte coefficient sequence

BITS 7 0

AD	R/W	PU	RCS	CMB3	CMB2	CMB1	CMB0

Initial value on RESET : 0Fh (NOP)

6.4.2. CONFIGURATION REGISTER 1 (CR1)

	Logical 1	Logical 0
BIT 7	GR = 1; GR gain loaded from CRAM	GR = 0; GR gain set to 0dB
BIT 6	GZ = 1; Z gain loaded from CRAM	GZ = 0; Z gain set to -18 dB
BIT 5	FX = 1; X filter loaded from CRAM	FX = 0; X filter set to 0dB flat
BIT 4	FR = 1; R filter loaded from CRAM	FR = 0; R filter set to 0dB flat
BIT 3	GX = 1; GX gain loaded from CRAM	GX = 0; GX gain set to 0dB

BIT 2 1 0	TEST MODE	CONFIGURATION DESCRIPTION
0 0 0	NOT	No test mode
0 0 1	ALS	Analog loop back via converter registers
0 1 0	ALM	The MIC/Xin input loops back to HON & HOP (AHO amplifier). The FHM input loops back to analog MUX. FHM input loops back to LSN & LSP (ALS amplifier).
0 1 1	BYP	By-pass: The analog front end is by-passed. FHM serves as a direct single ended input to the A/D converter while HOP outputs the single ended signal generated by the D/A converter
1 0 0	IDR	Data RAM initialisation, reset all data RAM locations to hex C0
1 0 1	DLS	Digital loop back via converter registers
1 1 0	DLM	The D/A output is looped back to the A/D input via the analog I/O mux
1 1 1	DLP	Digital loop back via PCM registers

BITS 7 0

GR	GZ	FX	FR	GX	TMB2	TMB1	TMB0

Initial value on RESET : 00h

6.4.3. CONFIGURATION REGISTER 2 (CR2)

	Logical 1	Logical 0
BIT 7	SD = 1 ;SD pin programmed as input	SD = 0 ;SD pin programmed as output
BIT 6	SC = 1 ;SC pin programmed as input	SC = 0 ;SC pin programmed as output
BIT 5	SB = 1 ;SB pin programmed as input	SB = 0 ;SB pin programmed as output
BIT 4	SA = 1 ;SA pin programmed as input	SA = 0 ;SA pin programmed as output
BIT 3	ELS = 1 ;PCI pins SA-SD, which are not programmed as TX-SIG transmit inputs, tristate SIP in TX direction	ELS = 0 ;pins SA-SD which are not TX-SIG inputs, are sending zeros
BIT 2	AM = 1 ;only one device is connected to the SLD bus, send NOP's during TX-FC	AM = 0 ;two devices are connected to the SLD-bus, tristate SIP during TX-FC
BIT 1	TR = 1 ;Three party conferencing enabled CH-B1 is added to CH-B2 in the RX direction	TR = 0 ;Three party conferencing disabled
BIT 0	SLD MODE EFC = 1 ;Enable feature control. TX-FC channel is enabled IOM2 MODE SEL = 1 ;Bearer channels transmit & receive in IOM channel 0	EFC = 0 ;TX-FC channel is disabled (high Z) SEL = 0 ;B channels transmit & receive in IOM channel 1

BITS 7 ... 0

SD	SC	SB	SA	ELS	AM	TR	EFC/ SEL

Initial value on RESET: F9h

6.4.4. CONFIGURATION REGISTER 3 (CR3)

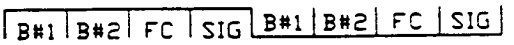
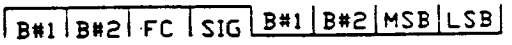
BIT 7 6 5			
0 0 0	52.0 dB default on RESET (*)	0 1 1	34.0 dB (*)
0 0 1	46.0 dB (*)	1 0 0	28.0 dB
0 1 0	40.0 dB (*)	1 0 1	22.0 dB
1 1 1	X input enabled with a 15.1 dB amplification factor. MIC input disabled	1 1 0	16.0 dB

(*) When using one of these values the specifications of the transmission characteristics and of the gain error are not guaranteed anymore.

BIT 4 3 2 Operating mode Configuration description
Analog Front End Control (AFEC)

Code	State	MIC/Xin	FHM	Hout	LSout	Comments
0 0 0	POR	off	off	off	off	power on reset
0 0 1	RDY	on	off	on	off	ready
0 1 0	LH1	off	off	off	on	loud hearing 1
0 1 1	LH2	on	off	off	on	loud hearing 2
1 0 0	LH3	on	off	on	on	loud hearing 3
1 0 1	HFS	off	on	off	on	handsfree
1 1 0	MUT	off	off	on	off	mute
1 1 1	RES	X	X	X	X	reserved

X: not defined

BIT 1	0	Operating mode	Linear Input/Output (LIO)
0	0	LIO 0 Normal I/O mode	
0	1	LIO 1; ELS = 0 Mixed I/O mode not available in IOM2 mode	
1	0	LIO 2 Linear I/O mode	
1	1	LIO 3 reserved	

BITS	7		0
	AGX	AFEC	LIO

Initial value on Reset : 00h

6.4.5. CONFIGURATION REGISTER 4 (CR4)

	Logical 1	Logical 0
BIT 7	DHF = 1 ;digital high-pass in TX direction enabled	DHF = 0 ;digital high-pass in TX disabled
BIT 6	DTMF = 1 ;DTMF generator enabled	DTMF = 0 ;DTMF generator disabled
BIT 5	TG = 1 ;tone ring enabled	TG = 0 ;tone ring disabled
BIT 4	BT = 1 ;Beat tone generator enabled	BT = 0 ;Beat tone generator disabled
BIT 3	TM = 1 ;Tone mode bit set, incoming voice is activated	TM = 0 ;incoming voice is blocked
BIT 2	BM = 1 ;Beat mode. 3 tone ring activated when BT generator enabled	BM = 0 ;2 tone ring activated when BT generator enabled
BIT 1	PM = 1 ;Piezo mode bit set, tone generator is output to the piezo ring pins SA & SB	PM = 0 ;The tone generator is directed to the loudspeaker (D/A out)
BIT 0	A/μ = 1; μ-law enabled	A/μ = 0; A-law enabled

BITS

7							0
DHF	DTMF	TG	BT	TM	BM	PM	A/μ

X: don't care

Initial value on RESET: 00h

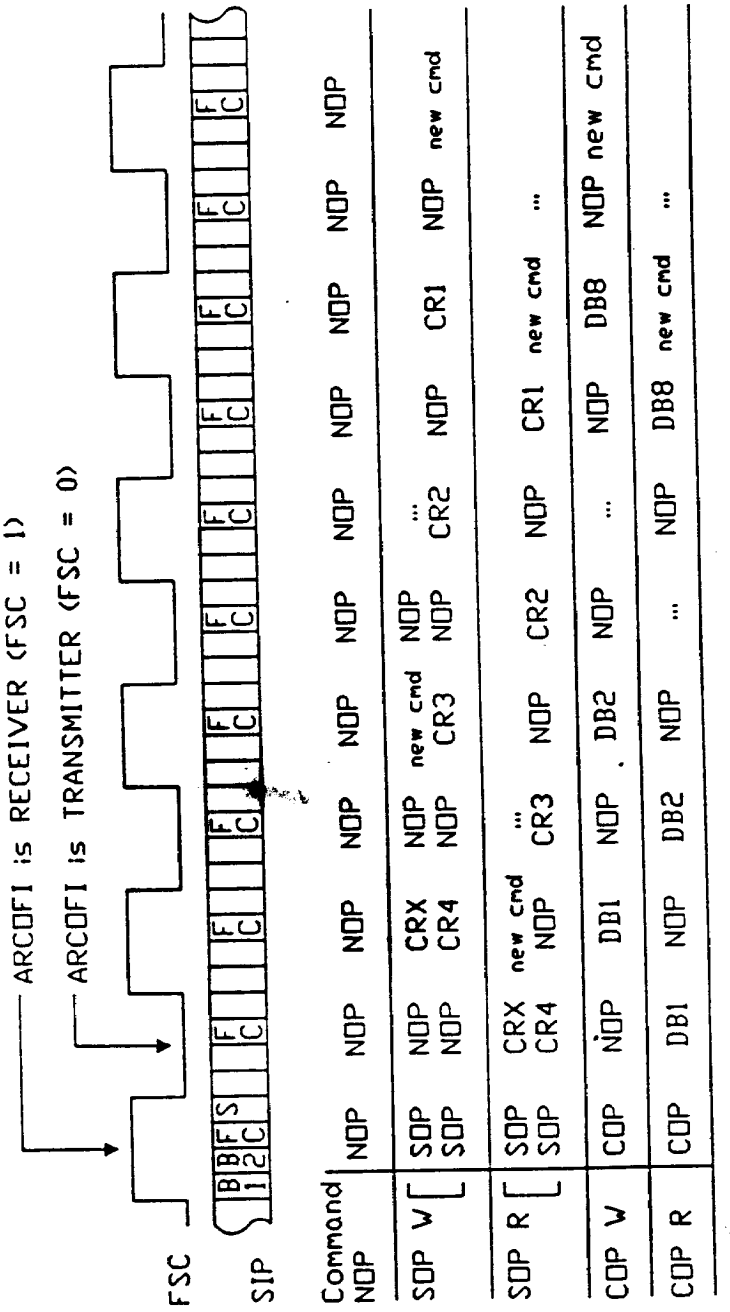
6.4.6. ARCOFI® PROGRAMMING VIA THE SLD BUS

Time slot	t0	t1	t2	t3	t4	t5
Transfer direction	RX TX	RX TX	RX TX	RX TX	RX TX	RX TX
CH - B1	B1 B1	B1 B1	B1 B1	B1 B1	B1 B1	B1 B1
CH -B2	X Z	X Z	X Z	X Z	X Z	X Z
FC - CH	SOP NOP	CR4 NOP	CR3 NOP	CR2 NOP	CR1 NOP	NOP SOP COP
SIG - CH	SIG SIG	SIG SIG	SIG SIG	SIG SIG	SIG SIG	SIG SIG

X: don't care

Z: high impedance

6.4.7. ARCOFI® CONTROL BYTE SEQUENCES IN THE FC TIME SLOT



Command												
NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP
SOP W X	SOP	NOP	CRX	NOP	new cmd	NOP	...					
	SOP	NOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	NOP	new cmd	
SOP R X	SOP	CRX	new cmd	...								
	SOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	new cmd	...		
COP W	COP	NOP	DB1	NOP	DB2	NOP	...	NOP	DB8	NOP	new cmd	
COP R	COP	DB1	NOP	DB2	NOP	...	NOP	DB8	new cmd	...		

X = 1,2,3 or 4
new cmd = NOP- or COP- or SOP- Command bytes in transmit direction
DB1 = 1st Data Bit
W = Write
R = Read

7. ARCOFI ELECTRICAL CHARACTERISTICS

The following section defines the electrical characteristics of the ARCOFI under normal operating conditions unless otherwise specified.

Vdd = 5V +/- 5%, DGND = OV

Vss = -5V +/- 5%

TEMP = -25 to 70 C (functions guaranteed)
0 to 70 C (Specifications guaranteed)

7.1. ABSOLUTE MAXIMUM RATING

	SYMBOL	MIN	MAX	UNIT
Storage temperature	Tstg	-60	125	C
Ambient temperature under bias	Ta	-10	80	C
Vdd referred to GNDD		-0.3	5.5	V
Vss referred to GNDA		-5.5	0.3	V
GNDA to GNDD		-0.3	0.3	V
Analog input and output voltages referred to Vdd referred to Vss	V	 -10.3 -0.3	 0.3 10.3	 V V
All digital input and output voltages referred to GNDD referred to Vdd	V	 -0.3 -5.3	 5.3 0.3	 V V
Power dissipation	Pd		1	W

7.2. ARCOF DC CHARACTERISTICS

DESCRIPTION	PARA-METER	CONDITION	MIN	TYP	MAX	UNIT
DIGITAL						
Input leakage current	I_{IL}	$-0.3 \le V_{IN} \le V_{DD}$			±1	µA
H-input level	V_{IH}		2.0		V_{DD} +0.3	V
L-input level	V_{IL}		-0.3		0.8	V
H-output level	V_{OH}	I_O = 400µA	2.0			V
L-output level (except DU-Pin)	V_{OL1}	I_O = -2mA			0.45	V
L-output level DU-Pin	V_{OL2}	I_O = -7mA			0.45	V
V_{DD} Supply current standby	I_{DD}	V_{SS} = 0V V_{DD} = 5.25V CLK = 512kHz		1.6	2	mA
		No clock		0.7	1	mA
standby		+/- 5% supply		3.4	4.5	mA
operating *)		+/- 5% supply		11	15	mA
V_{SS} Supply current Standby	I_{SS}	+/- 5% supply		-2.4	-3.5	mA
operating *)		+/- 5% supply		-8	-13	mA
Standby power dissipation	P_D	+/- 5% supply		30	42	mW
Operating power dissipation	P_{d1}	+/- 5% supply LH3 **)		100	150	mW
Input capacitance	C_I				10	pF
Output capacitance	C_O				15	pF

*) Operating power dissipation is measured with all analog outputs open.
**) RDY needs less than LH3

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7.3. SLD BUS SWITCHING CHARACTERISTICS

DESCRIPTION	Parameter	MIN	TYP	MAX	UNIT
CLK period	t_{CLK}	1.76	1.953	2.15	µs
CLK duty cycle		30	50	70	%
FSC period	t_{FSC}		125		µs
FSC delay time	td_{FSC}	-20		100	ns
FSC high time	th_{FSC}	t_{CLK}	62.5		µs
SIP data in setup time	td_{IN_S}	50			ns
SIP data in hold time	td_{IN_H}	80			ns
SIP data out delay	td_{OUT}			250	ns

Note: SIP is an I/O pin; SIP IN denotes timings for incoming data and SIP OUT denotes timings relation with outgoing data.

7.3.1. SLD BUS TIMING DIAGRAM (FIG 7.1)

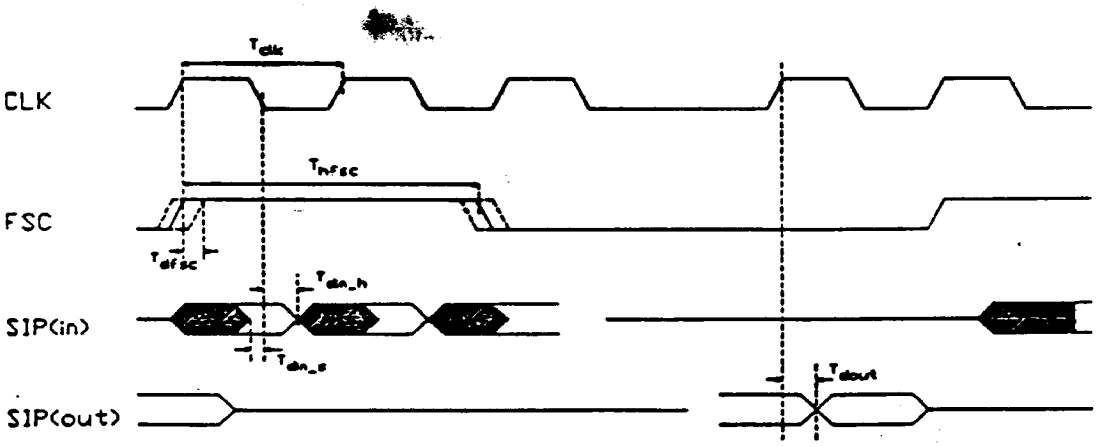

Figure 7.1:

7.4. IOM®2 BUS SWITCHING CHARACTERISTICS

DESCRIPTION	Parameter	MIN	TYP	MAX	UNIT
DCLK period	T_{DCLK}	487	651	815	ns
DCLK duty cycle		20	50	80	%
FSC period	T_{FSC}		125		µs
FSC delay time	T_{dFSC}	-20		100	ns
FSC high time	T_{hFSC}	T_{DCLK}	41.67		µs
Input data setup time	Tids	50			ns
Input data hold time	Tidh	50			ns
Output data delay	Todd			200	ns

7.4.1. IOM®2 BUS TIMING DIAGRAM (FIG 7.2)

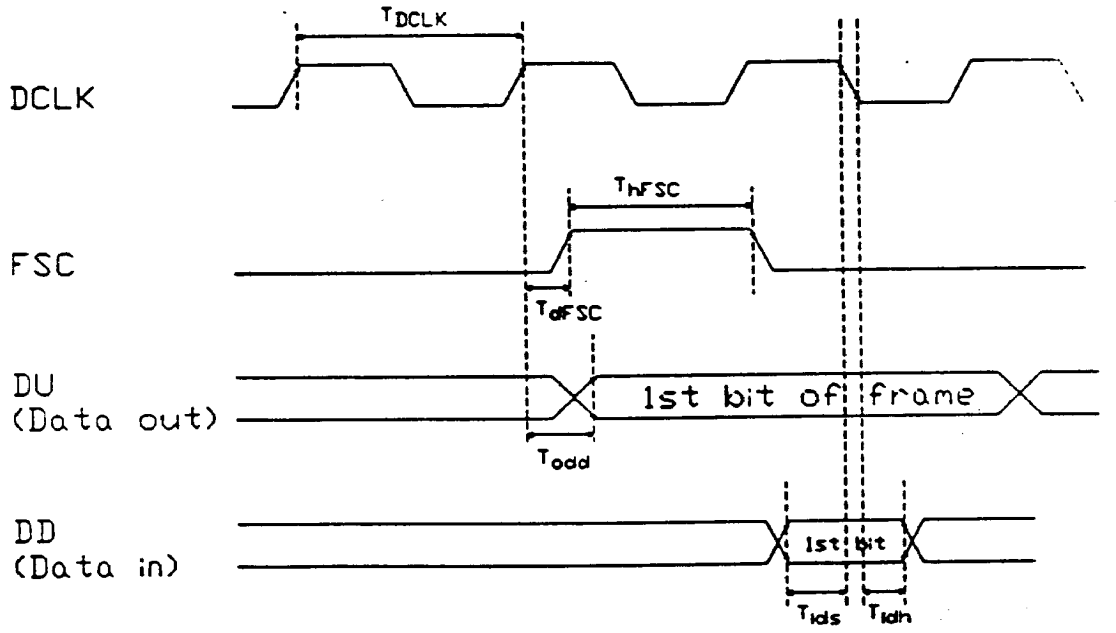

Figure 7.2:

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7.5. PCI SWITCHING CHARACTERISTICS

DESCRIPTION	Parameter	MIN	MAX	UNIT
SIP in to PCI out	td_{PCIo}		350	ns
PCI in setup time	t_{PCIins}	50		ns
PCI in hold time	t_{PCIinh}	100		ns

7.5.1. PCI TIMING DIAGRAM (FIG 7.3)

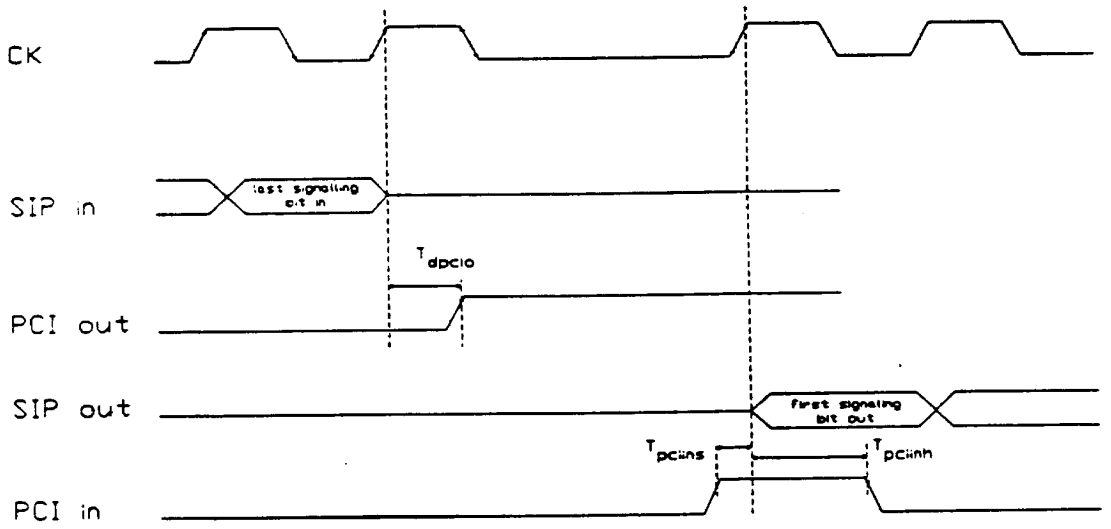

Figure 7.3:

7.6. RESET TIMING

DESCRIPTION	Parameter	MIN	MAX	UNIT
V_{DD} rise time	t_{RVdd}	0	20	ms
Reset pulse width	t_{RS}	2		µs
Power Stable to reset low	t_{SRS}	1		µs
Reset transition time	t_{tr}		1	ms

7.6.1. RESET TIMING DIAGRAM (FIG 7.4)

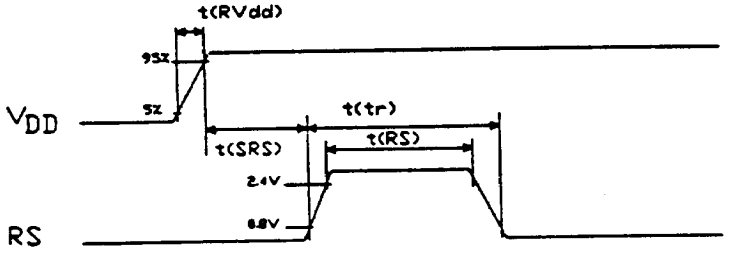

Figure 7.4:

7.7. TEST CONDITIONS

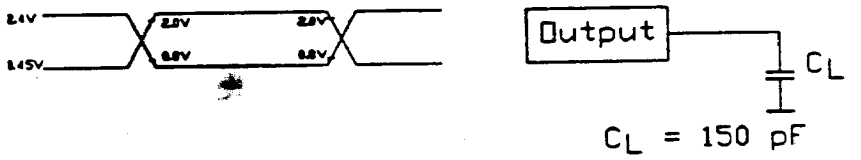

Figure 7.5:

AC testing inputs are driven at 2.4V for a logical one and 0.45V for a logical zero. Timing measurements are made at 2.0V and 0.8V for a logical one and a logical zero respectively.

7.8. PACKAGE OUTLINES