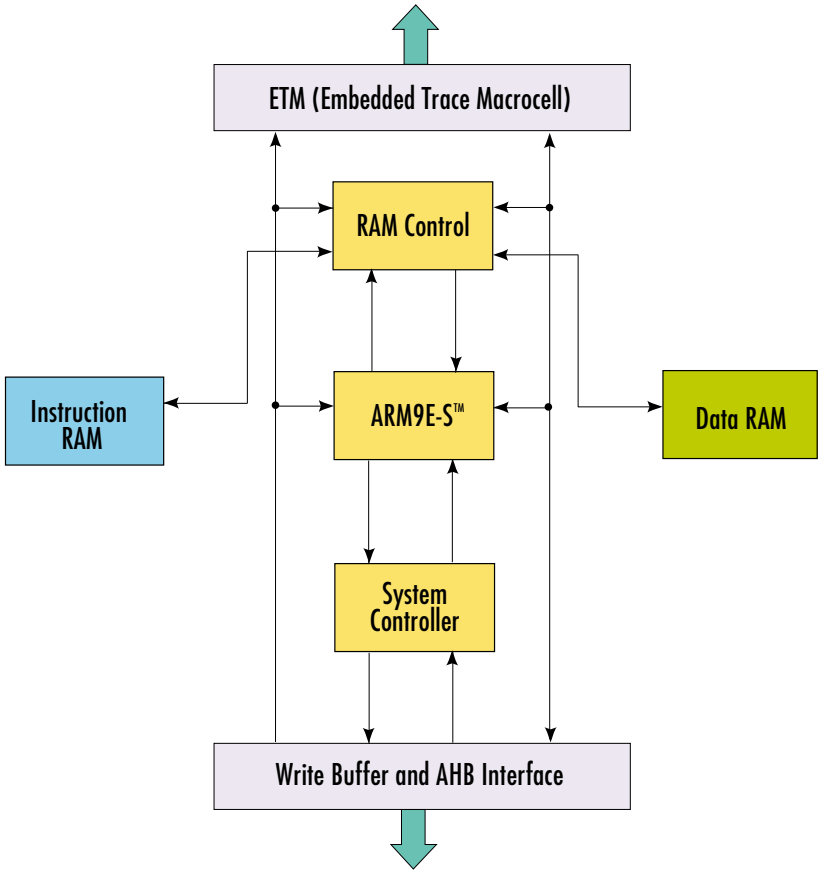
CW001102 - 120 MHz Low Power Synthesized ARM966E-S™ Core

OVERVIEW

The CW001102 processor core is a low power implementation of the popular ARM966E-S™, synthesized onto LSI Logic's G12L 0.18 micron low leakage process technology.

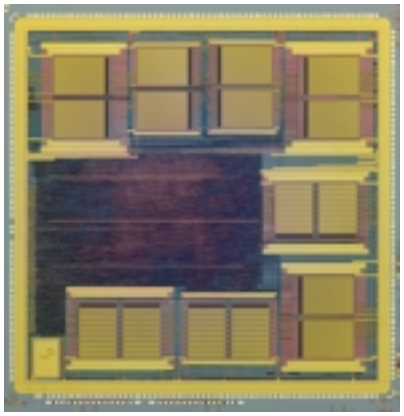
The ARM966E-S, which is based on the five stage pipeline ARM9E-S™ Harvard architecture processor, also contains a complete memory subsystem of tightly coupled instruction and data RAMs, an Embedded Trace Macrocell (ETM) interface, and an AMBA™ (Advanced Microprocessor Bus Architecture) AHB (Advanced High performance Bus) interface unit. This high level of integration helps ease the task of integrating the core into your System on Chip (SoC) design. Tight coupling of the RAM allows for high speed operation and predictable memory timing. This makes the core an ideal choice for real time systems needing timing critical execution. The instruction and data RAM sizes are user configurable up to 512 K bytes. The AHB interface includes a write buffer capable of burst transfers and split transactions. The ETM interface, when used with the optional ETM core, provides extensive real-time trace capabilities.



ARM966E-S™ Block Diagram

FEATURES AND BENEFITS

- 0.7 mW/MHz power dissipation T_j =115 °C, V_{dd} =1.8 V, slow process
- G12L 0.18 micron, 1.8 V low leakage process
- 120 MHz Operating frequency
- ARM966E-S Industry Standard Architecture
- Configurable memory subsystem for maximum flexibility
- Synthesized core for optimal timing accuracy and ASIC compatible design flow
- Complete AMBA subsystem reference design available
- Extensive portfolio of AMBA peripherals
- Regional ARM CoreWare design support



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The ARM966E-S supports the ARMv5TE instruction set including all of the ARM9E family DSP instruction extensions. The core supports for both the ARM® 32-bit and Thumb® 16-bit instruction sets, making it upwardly code-compatible with both the ARM7TDMI™ and ARM9TDMI™ families. The ability to switch on the fly between ARM and Thumb instruction sets allows the user to trade between high performance and code density.

The built in AMBA bus interface of the ARM966E-S core is an ideal standard bus for building a complete CPU subsystem design. LSI Logic offers both an AMBA subsystem reference design, and a library of popular AMBA CPU peripherals for use by customers on SoC designs. Customers can also incorporate their own AMBA based blocks onto this widely used industry standard bus.

The ARM966E-S is supported by a wide array of software development tools available from ARM Limited as well as third party vendors.

The core is implemented in LSI Logic's G12L low leakage 0.18 micron (drawn) process, giving a maximum speed of 120 MHz (worst case commercial). Power consumption for the core is just 0.7 mW/MHz, making this core ideal for a variety of portable applications.

The CW001102 core is synthesized onto the G12L SoC cell library and is provided complete with highly accurate timing models that fully support Static Timing Analysis (STA) through the core. This can be a significant benefit for achieving timing closure on high performance designs. The core is fully compatible with LSI Logic's entire FlexStream® SoC ASIC design flow making it straightforward to integrate into complex customer designs. The CW001102 comes complete with built in full scan chains for good testability, and is provided with a comprehensive set of deliverables including design files, STA and ATPG scripts, and detailed integration guidelines. To further assist customers with their designs, LSI Logic provides specialized ARM CoreWare® integration support through our team of regionally based Field CoreWare Engineers.

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