

**128M x 72 2-Bank Registered SDRAM Module****Features**

- 168-Pin Registered 8-Byte Dual In-Line Memory Module
- 128Mx72 Synchronous DRAM DIMM

|                                      |                   | -75A<br>Reg. |      | Units |
|--------------------------------------|-------------------|--------------|------|-------|
| DIMM $\overline{\text{CAS}}$ Latency |                   | 4            |      |       |
| $f_{\text{CK}}$                      | Clock Frequency   | 133          | 100  | MHz   |
| $t_{\text{CK}}$                      | Clock Cycle       | 7.5          | 10.0 | ns    |
| $t_{\text{AC}}$                      | Clock Access Time | 5.65         | 5.65 | ns    |

- Intended for 100MHz and 133MHz applications
- Inputs and outputs are LVTTTL (3.3V) compatible
- Single  $3.3\text{V} \pm 0.3\text{V}$  power supply
- Single Pulsed  $\overline{\text{RAS}}$  interface
- SDRAMs have four internal banks
- Module has two physical banks
- Fully synchronous to positive clock edge

- Programmable operation:
  - DIMM  $\overline{\text{CAS}}$  Latency: 4 (Registered mode);
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, and 8
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge commands
- Suspend mode and Power Down mode
- 13/11/2 Addressing (Row/Column/Bank)
- 8192 refresh cycles distributed across 64ms
- Card size: 5.25" x 1.70" x 0.320"
- Gold contacts
- DRAMs in TSOJ - 2 High Package
- Serial Presence Detect with Write protect feature

**Description**

IBM13M13734BCA is a registered 168-Pin Synchronous DRAM Dual In-Line Memory Module (DIMM) organized as a 128Mx72 high-speed memory array. The DIMM uses 18 128Mx4 SDRAMs in 400 mil TSOJ stacked packages. The DIMM achieves high-speed data-transfer rates of 100MHz and 133MHz by employing a prefetch/pipeline hybrid architecture that synchronizes the output data to a system clock.

The DIMM is intended for use in applications operating at 100MHz and 133MHz memory bus speeds. All control and address signals are re-driven through registers/buffers to the SDRAM devices. Operating in registered mode (REGE pin tied high), the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

A phase-lock loop (PLL) on the DIMM is used to re-drive the clock signals to both the SDRAM devices and the registers to minimize system clock loading. (CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated on the DIMM). A single clock

enable (CKE0) controls all devices on the DIMM, enabling the use of SDRAM Power Down modes.

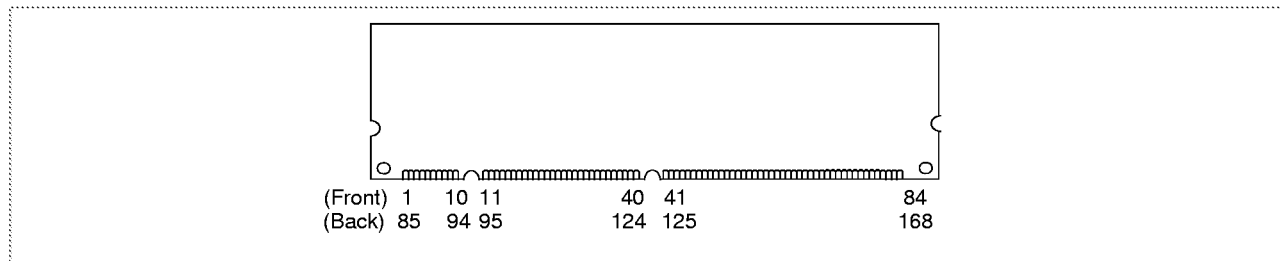
Prior to any access operation, the device  $\overline{\text{CAS}}$  latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A9 using the mode register set cycle. The DIMM  $\overline{\text{CAS}}$  latency when operated in Registered mode is one clock later than the device  $\overline{\text{CAS}}$  latency due to the address and control signals being clocked to the SDRAM devices.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked by the DIMM manufacturer. The last 128 bytes are available to the customer and may be write protected by providing a high level to pin 81 on the DIMM. An on-board pull-down resistor keeps this in the Write Enable mode.

All IBM 168-pin DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

IBM13M13734BCA  
128M x 72 2-Bank Registered SDRAM Module

## Card Outline



## Ordering Information

| Part Number         | Organization | Clock Cycle<br>(CL, $t_{RCD}$ , $t_{RP}$ ) | Access Time | Leads | Dimension              | Power |
|---------------------|--------------|--------------------------------------------|-------------|-------|------------------------|-------|
| IBM13M13734BCA-75AY | 128Mx72      | 7.5ns (333)                                | 5.4ns       | Gold  | 5.25" x 1.70" x 0.320" | 3.3V  |



## Pin Description

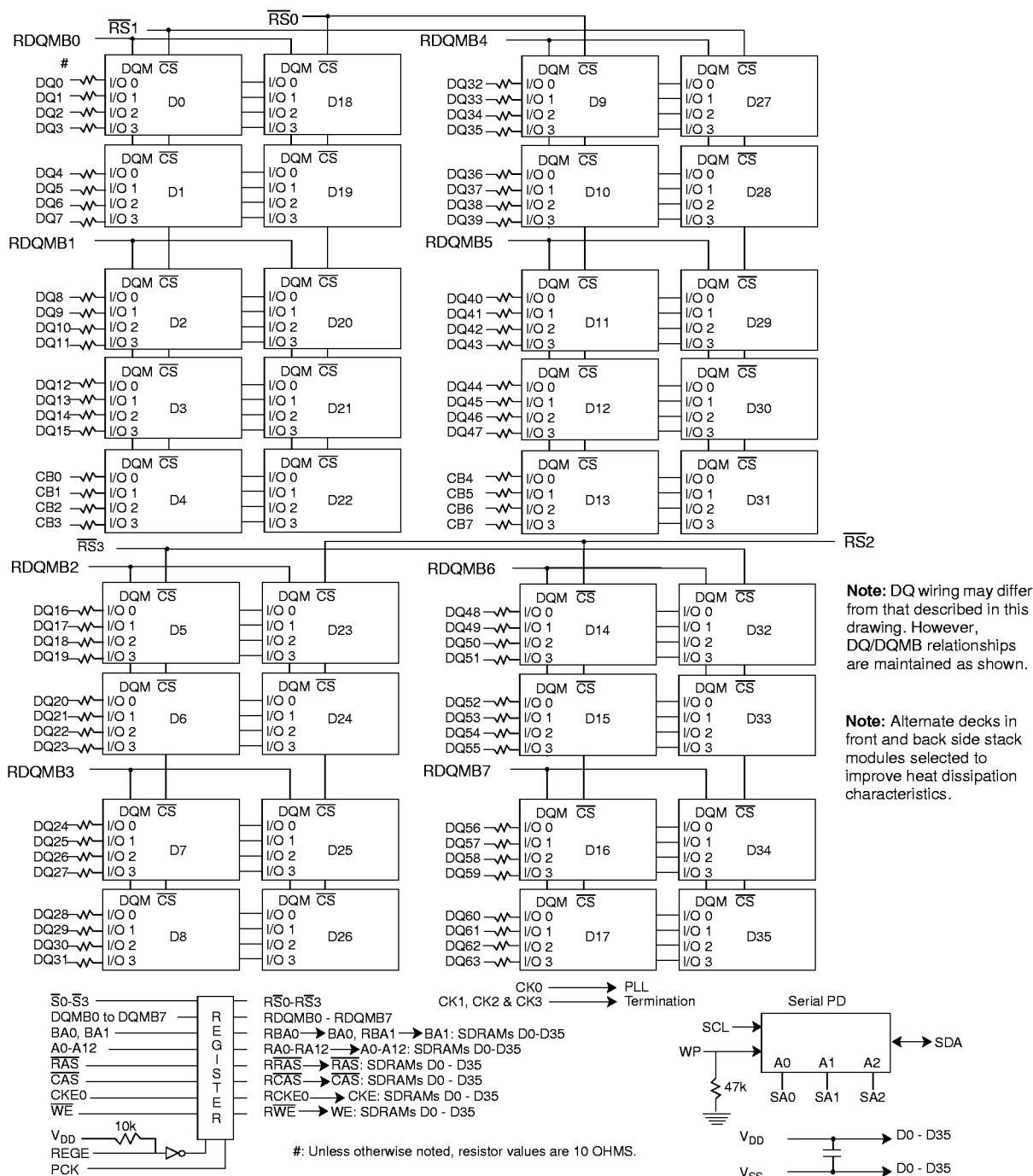
|                                               |                             |                 |                                          |
|-----------------------------------------------|-----------------------------|-----------------|------------------------------------------|
| CK0 - CK3                                     | Clock Inputs                | DQ0 - DQ63      | Data Input/Output                        |
| CKE0                                          | Clock Enable                | CB0 - CB7       | Check Bit Data Input/Output              |
| $\overline{\text{RAS}}$                       | Row Address Strobe          | DQMB0 - DQMB7   | Data Mask                                |
| $\overline{\text{CAS}}$                       | Column Address Strobe       | $V_{\text{DD}}$ | Power (3.3V)                             |
| $\overline{\text{WE}}$                        | Write Enable                | $V_{\text{SS}}$ | Ground                                   |
| $\overline{\text{S}}0 - \overline{\text{S}}3$ | Chip Selects                | NC              | No Connect                               |
| A0 - A9, A11, A12                             | Address Inputs              | SCL             | Serial Presence Detect Clock Input       |
| A10/AP                                        | Address Input/Autoprecharge | SDA             | Serial Presence Detect Data Input/Output |
| BA0, BA1                                      | SDRAM Bank Address Inputs   | SA0-2           | Serial Presence Detect Address Inputs    |
| WP                                            | SPD Write Protect           | REGE            | Register Enable                          |

## Pinout

| Pin# | Front Side      | Pin# | Back Side       | Pin# | Front Side             | Pin# | Back Side               | Pin# | Front Side             | Pin# | Back Side              | Pin# | Front Side      | Pin# | Back Side       |
|------|-----------------|------|-----------------|------|------------------------|------|-------------------------|------|------------------------|------|------------------------|------|-----------------|------|-----------------|
| 1    | $V_{\text{SS}}$ | 85   | $V_{\text{SS}}$ | 22   | CB1                    | 106  | CB5                     | 43   | $V_{\text{SS}}$        | 127  | $V_{\text{SS}}$        | 64   | $V_{\text{SS}}$ | 148  | $V_{\text{SS}}$ |
| 2    | DQ0             | 86   | DQ32            | 23   | $V_{\text{SS}}$        | 107  | $V_{\text{SS}}$         | 44   | NC                     | 128  | CKE0                   | 65   | DQ21            | 149  | DQ53            |
| 3    | DQ1             | 87   | DQ33            | 24   | NC                     | 108  | NC                      | 45   | $\overline{\text{S}}2$ | 129  | $\overline{\text{S}}3$ | 66   | DQ22            | 150  | DQ54            |
| 4    | DQ2             | 88   | DQ34            | 25   | NC                     | 109  | NC                      | 46   | DQMB2                  | 130  | DQMB6                  | 67   | DQ23            | 151  | DQ55            |
| 5    | DQ3             | 89   | DQ35            | 26   | $V_{\text{DD}}$        | 110  | $V_{\text{DD}}$         | 47   | DQMB3                  | 131  | DQMB7                  | 68   | $V_{\text{SS}}$ | 152  | $V_{\text{SS}}$ |
| 6    | $V_{\text{DD}}$ | 90   | $V_{\text{DD}}$ | 27   | $\overline{\text{WE}}$ | 111  | $\overline{\text{CAS}}$ | 48   | NC                     | 132  | NC                     | 69   | DQ24            | 153  | DQ56            |
| 7    | DQ4             | 91   | DQ36            | 28   | DQMB0                  | 112  | DQMB4                   | 49   | $V_{\text{DD}}$        | 133  | $V_{\text{DD}}$        | 70   | DQ25            | 154  | DQ57            |
| 8    | DQ5             | 92   | DQ37            | 29   | DQMB1                  | 113  | DQMB5                   | 50   | NC                     | 134  | NC                     | 71   | DQ26            | 155  | DQ58            |
| 9    | DQ6             | 93   | DQ38            | 30   | $\overline{\text{S}}0$ | 114  | $\overline{\text{S}}1$  | 51   | NC                     | 135  | NC                     | 72   | DQ27            | 156  | DQ59            |
| 10   | DQ7             | 94   | DQ39            | 31   | NC                     | 115  | $\overline{\text{RAS}}$ | 52   | CB2                    | 136  | CB6                    | 73   | $V_{\text{DD}}$ | 157  | $V_{\text{DD}}$ |
| 11   | DQ8             | 95   | DQ40            | 32   | $V_{\text{SS}}$        | 116  | $V_{\text{SS}}$         | 53   | CB3                    | 137  | CB7                    | 74   | DQ28            | 158  | DQ60            |
| 12   | $V_{\text{SS}}$ | 96   | $V_{\text{SS}}$ | 33   | A0                     | 117  | A1                      | 54   | $V_{\text{SS}}$        | 138  | $V_{\text{SS}}$        | 75   | DQ29            | 159  | DQ61            |
| 13   | DQ9             | 97   | DQ41            | 34   | A2                     | 118  | A3                      | 55   | DQ16                   | 139  | DQ48                   | 76   | DQ30            | 160  | DQ62            |
| 14   | DQ10            | 98   | DQ42            | 35   | A4                     | 119  | A5                      | 56   | DQ17                   | 140  | DQ49                   | 77   | DQ31            | 161  | DQ63            |
| 15   | DQ11            | 99   | DQ43            | 36   | A6                     | 120  | A7                      | 57   | DQ18                   | 141  | DQ50                   | 78   | $V_{\text{SS}}$ | 162  | $V_{\text{SS}}$ |
| 16   | DQ12            | 100  | DQ44            | 37   | A8                     | 121  | A9                      | 58   | DQ19                   | 142  | DQ51                   | 79   | CK2             | 163  | CK3             |
| 17   | DQ13            | 101  | DQ45            | 38   | A10/AP                 | 122  | BA0                     | 59   | $V_{\text{DD}}$        | 143  | $V_{\text{DD}}$        | 80   | NC              | 164  | NC              |
| 18   | $V_{\text{DD}}$ | 102  | $V_{\text{DD}}$ | 39   | BA1                    | 123  | A11                     | 60   | DQ20                   | 144  | DQ52                   | 81   | WP              | 165  | SA0             |
| 19   | DQ14            | 103  | DQ46            | 40   | $V_{\text{DD}}$        | 124  | $V_{\text{DD}}$         | 61   | NC                     | 145  | NC                     | 82   | SDA             | 166  | SA1             |
| 20   | DQ15            | 104  | DQ47            | 41   | $V_{\text{DD}}$        | 125  | CK1                     | 62   | NC                     | 146  | NC                     | 83   | SCL             | 167  | SA2             |
| 21   | CB0             | 105  | CB4             | 42   | CK0                    | 126  | A12                     | 63   | NC                     | 147  | REGE                   | 84   | $V_{\text{DD}}$ | 168  | $V_{\text{DD}}$ |

**Note:** All pin assignments are consistent with all 8-byte unbuffered versions.

## x72 ECC SDRAM DIMM Block Diagram (2 Bank, x4 SDRAMs)





## Input/Output Functional Description

| Symbol                                              | Type         | Polarity                           | Function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----------------------------------------------------|--------------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CK0 - CK3                                           | Input        | Positive Edge                      | The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock. CK0 drives the PLL. CK1, CK2 & CK3 are terminated.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| CKE0                                                | Input        | Active High                        | Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| $\overline{S}0 - \overline{S}3$                     | Input        | Active Low                         | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Physical Bank 0 is selected by $\overline{S}0$ and $\overline{S}2$ ; Bank 1 is selected by $\overline{S}0$ and $\overline{S}3$ .                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| $\overline{RAS}$ , $\overline{CAS}$ $\overline{WE}$ | Input        | Active Low                         | When sampled at the positive rising edge of the clock, $\overline{CAS}$ , $\overline{RAS}$ , and $\overline{WE}$ define the operation to be executed by the SDRAM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| BA0, 1                                              | Input        | —                                  | Selects which SDRAM bank of four is activated.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| A0 - A9, A11, A12, A10/AP                           | Input        | —                                  | During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge.<br>During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA9), A11 when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled.<br>During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, then BA0 and BA1 are used to define which bank to precharge. |
| DQ0 - DQ63, CB0 - CB7                               | Input Output | —                                  | Data and Check Bit Input/Output pins.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| DQMB0 - DQMB7                                       | Input        | Active High                        | The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high impedance state when sampled high. In Read mode, DQMB has a latency of three clock cycles in Registered mode, and controls the output buffers like an output enable. In Write mode, DQMB has a latency of one clock cycle in Registered mode. In this case, DQMB operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high.                                                                                                                                                                                                                                                                                                                          |
| V <sub>DD</sub> , V <sub>SS</sub>                   | Supply       |                                    | Power and ground for the module.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| REGE                                                | Input        | Active High (Register Mode Enable) | The Register Enable pin must be held high for proper registered mode operation (signals redriven to the SDRAMs when the clock rises, and held valid until the next rising clock).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| SA0 - 2                                             | Input        | —                                  | These signals are tied at the system planar to either V <sub>SS</sub> or V <sub>DD</sub> to configure the SPD EEPROM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| SDA                                                 | Input Output | —                                  | This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus time to V <sub>DD</sub> to act as a pull up.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| SCL                                                 | Input        | —                                  | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V <sub>DD</sub> to act as a pull up.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| WP                                                  | Input        | Active High                        | This signal is pulled low on the DIMM to enable data to be written into the last 128 bytes of the SPD EEPROM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

## Serial Presence Detect (Part 1 of 2)

| Byte # | Description                                                                    | SPD Entry Value                                   | Serial PD Data Entry (Hexadecimal) | Notes |
|--------|--------------------------------------------------------------------------------|---------------------------------------------------|------------------------------------|-------|
| 0      | Number of Serial PD Bytes Written during Production                            | 128                                               | 80                                 |       |
| 1      | Total Number of Bytes in Serial PD device                                      | 256                                               | 08                                 |       |
| 2      | Fundamental Memory Type                                                        | SDRAM                                             | 04                                 |       |
| 3      | Number of Row Addresses on Assembly                                            | 13                                                | 0D                                 |       |
| 4      | Number of Column Addresses on Assembly                                         | 11                                                | 0B                                 |       |
| 5      | Number of DIMM Banks                                                           | 2                                                 | 02                                 |       |
| 6 - 7  | Data Width of Assembly                                                         | x72                                               | 4800                               |       |
| 8      | Assembly Voltage Interface Levels                                              | LVTTL                                             | 01                                 |       |
| 9      | SDRAM Device Cycle Time (CL = 3)                                               | 7.5ns                                             | 75                                 | 1, 2  |
| 10     | SDRAM Device Access Time from Clock at CL=3                                    | 5.4ns                                             | 54                                 |       |
| 11     | DIMM Configuration Type                                                        | ECC                                               | 02                                 |       |
| 12     | Assembly Refresh Rate/Type                                                     | SR/1X(7.813μs)                                    | 82                                 |       |
| 13     | SDRAM Device Width                                                             | x4                                                | 04                                 |       |
| 14     | Error Checking SDRAM Device Width                                              | x4                                                | 04                                 |       |
| 15     | SDRAM Device Attr: Min Clk Delay, Random Col Access                            | 1 Clock                                           | 01                                 |       |
| 16     | SDRAM Device Attributes: Burst Lengths Supported                               | 1, 2, 4, 8                                        | 0F                                 |       |
| 17     | SDRAM Device Attributes: Number of Device Banks                                | 4                                                 | 04                                 |       |
| 18     | SDRAM Device Attributes: $\overline{\text{CAS}}$ Latency                       | 2, 3                                              | 06                                 |       |
| 19     | SDRAM Device Attributes: $\overline{\text{CS}}$ Latency                        | 0                                                 | 01                                 |       |
| 20     | SDRAM Device Attributes: $\overline{\text{WE}}$ Latency                        | 0                                                 | 01                                 |       |
| 21     | SDRAM Module Attributes                                                        | Registered/Buffered with PLL                      | 1F                                 |       |
| 22     | SDRAM Device Attributes: General                                               | Write-1/Read Burst, Precharge All, Auto-Precharge | 0E                                 |       |
| 23     | Minimum Clock Cycle at CLX-1 (CL = 2)                                          | 15.0ns                                            | F0                                 | 1, 2  |
| 24     | Maximum Data Access Time ( $t_{AC}$ ) from Clock at CLX-1 (CL = 2)             | 9.0ns                                             | 90                                 |       |
| 25     | Minimum Clock Cycle Time at CLX-2 (CL = 1)                                     | N/A                                               | 00                                 |       |
| 26     | Maximum Data Access Time ( $t_{AC}$ ) from Clock at CLX-2 (CL = 1)             | N/A                                               | 00                                 |       |
| 27     | Minimum Row Precharge Time ( $t_{RP}$ )                                        | 20.0ns                                            | 14                                 |       |
| 28     | Minimum Row Active to Row Active delay ( $t_{RRD}$ )                           | 15ns                                              | 0F                                 |       |
| 29     | Minimum $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay ( $t_{RCD}$ ) | 20.0ns                                            | 14                                 |       |
| 30     | Minimum $\overline{\text{RAS}}$ Pulse width ( $t_{RAS}$ )                      | 45.0ns                                            | 2D                                 |       |
| 31     | Module Bank Density                                                            | 512MB                                             | 80                                 |       |

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM  $\overline{\text{CAS}}$  latency).
2. Minimum application clock cycle time is 7.5ns (133MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. "R" = Alphanumeric revision code, A-Z, 0-9.
5. rr = ASCII coded revision code byte "R".
6. ww = Binary coded decimal week code, 01-51 (Decimal) ' 01-34 (Hex).
7. yy = Binary coded decimal year code, 0-00 (Decimal) ' 00-63 (Hex).
8. ss = Serial number data byte, 00-FF (Hex).
9. These values apply to PC100 applications only.



## Serial Presence Detect (Part 2 of 2)

| Byte #    | Description                                        | SPD Entry Value             | Serial PD Data Entry (Hexadecimal)     | Notes |
|-----------|----------------------------------------------------|-----------------------------|----------------------------------------|-------|
| 32        | Address and Command Setup Time Before Clock        | 1.5ns                       | 15                                     |       |
| 33        | Address and Command Hold Time After Clock          | 0.8ns                       | 08                                     |       |
| 34        | Data Input Setup Time Before Clock                 | 1.5ns                       | 15                                     |       |
| 35        | Data Input Hold Time After Clock                   | 0.8ns                       | 08                                     |       |
| 36 - 61   | Reserved                                           | Undefined                   | 00                                     |       |
| 62        | SPD Revision                                       | JEDEC 2                     | 02                                     |       |
| 63        | Checksum for bytes 0 - 62                          | Checksum data               | cc                                     | 3     |
| 64 - 71   | Manufacturers' JEDEC ID Code                       | IBM                         | A400000000000000                       |       |
| 72        | Assembly Manufacturing Location                    | Toronto, Canada             | 91                                     |       |
|           |                                                    | Vimercate, Italy            | 53                                     |       |
| 73 - 90   | Assembly Part Number                               | ASCII '13M13734BC "R" -75AY | 31334D31333733344243rr<br>373541592020 | 4, 5  |
| 91 - 92   | Assembly Revision Code                             | "R" plus ASCII Blank        | rr20                                   | 5     |
| 93 - 94   | Assembly Manufacturing Date                        | Year/Week code              | yyww                                   | 6, 7  |
| 95 - 98   | Assembly Serial Number                             | Serial Number               | ssssssss                               | 8     |
| 99 - 125  | Reserved                                           | Undefined                   | Not Specified                          |       |
| 126       | Module Supports Clock Frequency                    | 100MHz                      | 64                                     | 9     |
| 127       | Attributes for clock frequency defined in Byte 126 | CLK0, CL = 3, Con AP        | 85                                     | 9     |
| 128 - 255 | Open for Customer Use                              | Undefined                   | 00                                     |       |

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9. These values apply to PC100 applications only.

## Absolute Maximum Ratings

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                    | Parameter                       |                  | Rating              | Units | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|------------------|---------------------|-------|-------|
| V <sub>DD</sub>                                                                                                                                                                                                                                                                                                                                                                                           | Power Supply Voltage            |                  | -0.3 to +4.6        |       |       |
| V <sub>IN</sub>                                                                                                                                                                                                                                                                                                                                                                                           | Input Voltage                   | SDRAM Devices    | -1.0 to +4.6        | V     | 1     |
|                                                                                                                                                                                                                                                                                                                                                                                                           |                                 | Serial PD Device | -0.3 to +6.5        |       |       |
|                                                                                                                                                                                                                                                                                                                                                                                                           |                                 | Register         | 0 - V <sub>DD</sub> |       |       |
|                                                                                                                                                                                                                                                                                                                                                                                                           |                                 | PLL              | 0 - V <sub>DD</sub> |       |       |
| V <sub>OUT</sub>                                                                                                                                                                                                                                                                                                                                                                                          | Output Voltage                  | SDRAM Devices    | -1.0 to +4.6        |       |       |
|                                                                                                                                                                                                                                                                                                                                                                                                           |                                 | Serial PD Device | -0.3 to +6.5        |       |       |
| T <sub>A</sub>                                                                                                                                                                                                                                                                                                                                                                                            | Operating Temperature (ambient) |                  | 0 to +70            | °C    | 1     |
| T <sub>STG</sub>                                                                                                                                                                                                                                                                                                                                                                                          | Storage Temperature             |                  | -55 to +125         | °C    | 1     |
| P <sub>D</sub>                                                                                                                                                                                                                                                                                                                                                                                            | Power Dissipation               |                  | 23.8                | W     | 1, 2  |
| I <sub>OUT</sub>                                                                                                                                                                                                                                                                                                                                                                                          | Short Circuit Output Current    |                  | 50                  | mA    | 1     |
| F <sub>OP</sub>                                                                                                                                                                                                                                                                                                                                                                                           | Operating Frequency             | Min.             | 66                  | MHz   |       |
|                                                                                                                                                                                                                                                                                                                                                                                                           |                                 | Max.             | 133                 |       |       |
| 1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. |                                 |                  |                     |       |       |
| 2. Maximum power is calculated assuming both physical banks on the DIMM are in Auto Refresh mode.                                                                                                                                                                                                                                                                                                         |                                 |                  |                     |       |       |

## Recommended DC Operating Conditions ( $T_A = 0$ to $70^\circ\text{C}$ )

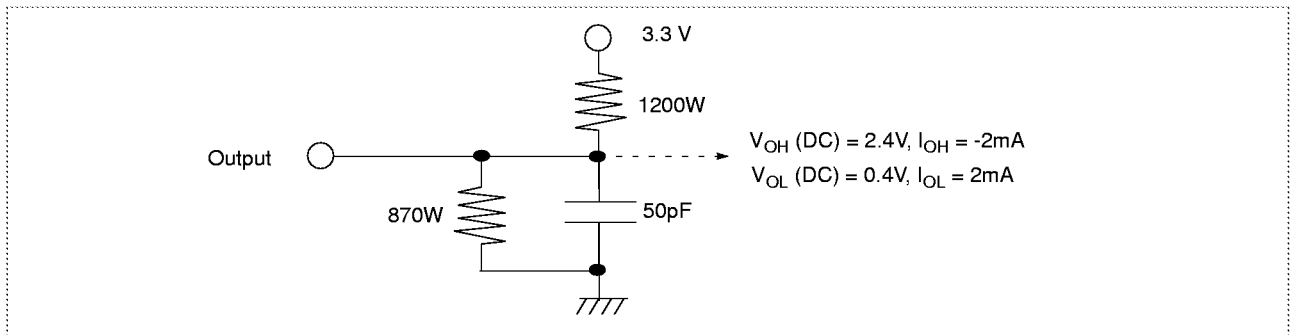
| Symbol                                   | Parameter          | Rating |      |                | Units | Notes |
|------------------------------------------|--------------------|--------|------|----------------|-------|-------|
|                                          |                    | Min.   | Typ. | Max.           |       |       |
| $V_{DD}$                                 | Supply Voltage     | 3.0    | 3.3  | 3.6            | V     | 1     |
| $V_{IH}$                                 | Input High Voltage | 2.0    | —    | $V_{DD} + 0.3$ | V     | 1     |
| $V_{IL}$                                 | Input Low Voltage  | -0.3   | —    | 0.8            | V     | 1     |
| 1. All voltages referenced to $V_{SS}$ . |                    |        |      |                |       |       |



## Capacitance ( $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$ , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

| Symbol    | Parameter                                                                                                                           | Organization | Units |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------|--------------|-------|
|           |                                                                                                                                     | x72 Max.     |       |
| $C_{I1}$  | Input Capacitance (A0 - A9, A10/AP, A11, A12, BA0, BA1, $\overline{WE}$ , $\overline{RAS}$ , $\overline{CAS}$ , $\overline{CKE0}$ ) | 19           | pF    |
| $C_{I2}$  | Input Capacitance ( $\overline{S0}$ - $\overline{S3}$ )                                                                             | 15           | pF    |
| $C_{I3}$  | Input Capacitance (DQMB0 - DQMB7)                                                                                                   | 14           | pF    |
| $C_{I4}$  | Input Capacitance (REGE)                                                                                                            | 10           | pF    |
| $C_{I5}$  | Input Capacitance (CK0)                                                                                                             | 28           | pF    |
| $C_{I6}$  | Input Capacitance (CK1, CK2, AND CK3)                                                                                               | 24           | pF    |
| $C_{I7}$  | Input Capacitance (SA0 - SA2, SCL, WP)                                                                                              | 9            | pF    |
| $C_{IO1}$ | Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)                                                                                    | 20           | pF    |
| $C_{IO2}$ | Input/Output Capacitance (SDA)                                                                                                      | 11           | pF    |

## DC Output Load Circuit



## Input/Output Characteristics ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

| Symbol     | Parameter                                                                                                                 | x72                        |          | Units         | Notes |
|------------|---------------------------------------------------------------------------------------------------------------------------|----------------------------|----------|---------------|-------|
|            |                                                                                                                           | Min.                       | Max.     |               |       |
| $I_{I(L)}$ | Input Leakage Current, any input<br>( $0.0\text{V} \leq V_{IN} \leq 3.6\text{V}$ ), All Other Pins<br>Not Under Test = 0V | Address and Control Inputs |          | $\mu\text{A}$ |       |
|            |                                                                                                                           | 10                         | 10       |               |       |
| $I_{O(L)}$ | Output Leakage Current<br>( $D_{OUT}$ is disabled, $0.0\text{V} \leq V_{OUT} \leq 3.6\text{V}$ )                          | DQ0-63, CB0 - 7            |          | $\mu\text{A}$ |       |
|            |                                                                                                                           | -4                         | +4       |               |       |
| $V_{OH}$   | Output Level<br>Output "H" Level Voltage ( $I_{OUT} = -2.0\text{mA}$ )                                                    | SDA                        |          | V             | 1     |
|            |                                                                                                                           | -1                         | +1       |               |       |
| $V_{OL}$   | Output Level<br>Output "L" Level Voltage ( $I_{OUT} = +2.0\text{mA}$ )                                                    | 2.4                        | $V_{DD}$ |               |       |
|            |                                                                                                                           | 0.0                        | 0.4      |               |       |

1. See DC output load circuit.

## Operating, Standby, and Refresh Currents ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

| Parameter                                                                    | Symbol<br>Physical Bank 0/<br>Physical Bank 1 | Test Condition                                                                                                              | Speed<br>-75A | Units | Notes |
|------------------------------------------------------------------------------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|---------------|-------|-------|
| Burst Operating Mode/Active Standby                                          | $I_{CC4}/I_{CC3}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 4180          | mA    | 1, 2  |
| Burst Operating Mode/Precharge Standby                                       | $I_{CC4}/I_{CC2}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 3640          | mA    | 1, 2  |
| Burst Operating Mode/Auto Refresh                                            | $I_{CC4}/I_{CC5}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 6250          | mA    | 1, 2  |
| Non-burst Operating Mode/Active Standby                                      | $I_{CC1}/I_{CC3}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 3550          | mA    | 1, 2  |
| Non-burst Operating Mode/Precharge Standby                                   | $I_{CC1}/I_{CC2}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 3010          | mA    | 1, 2  |
| Non-burst Operating Mode/Auto Refresh                                        | $I_{CC1}/I_{CC5}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 5620          | mA    | 1     |
| Active Standby/Active Standby                                                | $I_{CC3}/I_{CC3}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 2470          | mA    |       |
| Active Standby/Precharge Standby                                             | $I_{CC3}/I_{CC2}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 1930          | mA    |       |
| Active Standby/Auto Refresh                                                  | $I_{CC3}/I_{CC5}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 4540          | mA    | 1     |
| Precharge Standby/Precharge Standby                                          | $I_{CC2}/I_{CC2}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 1390          | mA    |       |
| Precharge Standby/Auto Refresh                                               | $I_{CC2}/I_{CC5}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 4000          | mA    | 1     |
| Auto Refresh/Auto Refresh                                                    | $I_{CC5}/I_{CC5}$                             | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 6610          | mA    | 1     |
| Active Standby Power Down/Active Standby Power Down                          | $I_{CC3p}/I_{CC3p}$                           | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 526           | mA    |       |
| Active Standby Power Down/Precharge Standby Power Down                       | $I_{CC3p}/I_{CC2p}$                           | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 454           | mA    |       |
| Precharge Standby Power Down/Precharge Standby Power Down                    | $I_{CC2p}/I_{CC2p}$                           | $\text{CKE} \leq V_{IL}(\text{max})$ , $t_{CK} = \text{min}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$      | 382           | mA    |       |
| Precharge Standby Non-power Down/Precharge Standby Non-power Down (NO CLOCK) | $I_{CC2S}/I_{CC2S}$                           | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{Infinity}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$ | 231           | mA    |       |
| Precharge Standby Power Down/Precharge Standby Power Down (NO CLOCK)         | $I_{CC2PS}/I_{CC2PS}$                         | $\text{CKE} \geq V_{IH}(\text{min})$ , $t_{CK} = \text{Infinity}$ ,<br>$\overline{S0} - \overline{S3} = V_{IH}(\text{min})$ | 87            | mA    |       |

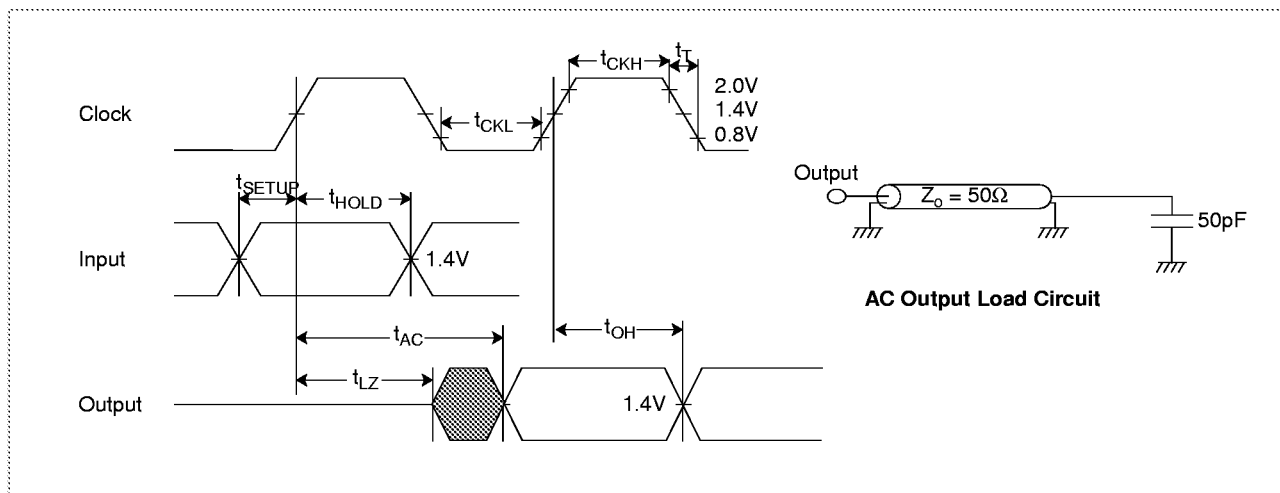
1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of  $t_{CK}$  and  $t_{RC}$ . Input signals are changed once during  $t_{CK}(\text{min})$ .  $t_{CK}(\text{min}) = 7.5\text{ns}$ .

2. The specified values are obtained with the output open.

## AC Characteristics ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

1. An initial pause of  $200\mu\text{s}$ , with CKE0 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. AC timing tests have  $V_{IL} = 0.8\text{V}$  and  $V_{IH} = 2.0\text{V}$  with the timing referenced to the  $1.4\text{V}$  crossover point.
3. The Transition time is measured between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ).
4. AC measurements assume  $t_T = 1.2\text{ns}$  (1 Volt/ns rise time).
5. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
6. A 1 ms stabilization time is required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal.
7. All timings are specified at the input receiver of the signal. This allows times to be specified at the end of a transmission line versus at the DIMM connector which may display significant reflections. Refer to the SDRAM and register device specifications for non-skew adjusted timings.

## AC Output Characteristics Diagram



## Clock and Clock Enable Parameters

| Symbol                                                                                                                                                                                                                                                                                                                                                                                                    | Parameter                                            | -75A max.<br>(Device CL<br>$t_{RCD}$ , $t_{RP}=3, 3, 3$ ) |      | Units | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------|-----------------------------------------------------------|------|-------|-------|
|                                                                                                                                                                                                                                                                                                                                                                                                           |                                                      | Min.                                                      | Max. |       |       |
| $t_{CK4}$                                                                                                                                                                                                                                                                                                                                                                                                 | Clock Cycle Time, DIMM $\overline{CAS}$ Latency = 4  | 7.5                                                       | 1000 | ns    | 1     |
| $t_{AC4}$                                                                                                                                                                                                                                                                                                                                                                                                 | Clock Access Time, DIMM $\overline{CAS}$ Latency = 4 | —                                                         | 5.65 | ns    | 1, 2  |
| $t_{CKH}$                                                                                                                                                                                                                                                                                                                                                                                                 | Clock High Pulse Width                               | 2.5                                                       | —    | ns    | 3     |
| $t_{CKL}$                                                                                                                                                                                                                                                                                                                                                                                                 | Clock Low Pulse Width                                | 2.5                                                       | —    | ns    | 3     |
| $t_{CES}$                                                                                                                                                                                                                                                                                                                                                                                                 | Clock Enable Setup Time                              | 1.65                                                      | —    | ns    | 1     |
| $t_{CEH}$                                                                                                                                                                                                                                                                                                                                                                                                 | Clock Enable Hold Time                               | 0.35                                                      | —    | ns    | 1     |
| $t_{SB}$                                                                                                                                                                                                                                                                                                                                                                                                  | Power Down Mode Entry Time                           | 0                                                         | 7.5  | ns    |       |
| $t_T$                                                                                                                                                                                                                                                                                                                                                                                                     | Transition Time (Rise and Fall)                      | 0.5                                                       | 10   | ns    |       |
| 1. DIMM $\overline{CAS}$ latency = device CL [clock cycles] + 1 for Register mode.<br>2. Access time is measured at 1.4V. See AC output load circuit.<br>3. $t_{CKH}$ is the pulse width of CLK measured from the positive edge to the negative edge referenced to $V_{IH}$ (min). $t_{CKL}$ is the pulse width of CLK measured from the negative edge to the positive edge referenced to $V_{IL}$ (max). |                                                      |                                                           |      |       |       |

## Common Parameters

| Symbol                                                                                                                                                                                                                             | Parameter                                                   | -75A |        | Units | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------|------|--------|-------|-------|
|                                                                                                                                                                                                                                    |                                                             | Min. | Max.   |       |       |
| $t_{CS}$                                                                                                                                                                                                                           | Command Setup Time                                          | 1.65 |        | ns    | 1     |
| $t_{CH}$                                                                                                                                                                                                                           | Command Hold Time                                           | 0.35 |        | ns    | 1     |
| $t_{AS}$                                                                                                                                                                                                                           | Address and Bank Select Setup Time                          | 1.65 |        | ns    | 1     |
| $t_{AH}$                                                                                                                                                                                                                           | Address and Bank Select Hold Time                           | 0.35 |        | ns    | 1     |
| $t_{RCD}$                                                                                                                                                                                                                          | $\overline{RAS}$ to $\overline{CAS}$ Delay                  | 20.0 |        | ns    | 1     |
| $t_{RC}$                                                                                                                                                                                                                           | Bank Cycle Time                                             | 67.5 |        | ns    | 1     |
| $t_{RAS}$                                                                                                                                                                                                                          | Active Command Period                                       | 45   | 100000 | ns    | 1     |
| $t_{RP}$                                                                                                                                                                                                                           | Precharge Time                                              | 20.0 |        | ns    | 1     |
| $t_{RRD}$                                                                                                                                                                                                                          | Bank to Bank Delay Time                                     | 15   |        | ns    | 1     |
| $t_{CCD}$                                                                                                                                                                                                                          | $\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank) | 1    |        | CLK   |       |
| 1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows: the number of clock cycles = specified value of timing/clock period (count fractions as a whole number). |                                                             |      |        |       |       |



## Mode Register Set Cycle

| Symbol                                                                                                                                                                                                                             | Parameter                    | -75A |      | Units | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|------|------|-------|-------|
|                                                                                                                                                                                                                                    |                              | Min. | Max. |       |       |
| $t_{RSC}$                                                                                                                                                                                                                          | Mode Register Set Cycle Time | 2    | —    | CLK   | 1     |
| 1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows: the number of clock cycles = specified value of timing/clock period (count fractions as a whole number). |                              |      |      |       |       |

## Refresh Cycle

| Symbol                                                                                                                                                                                                                                                                                         | Parameter                     | -75A |       | Units   | Notes |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------|------|-------|---------|-------|
|                                                                                                                                                                                                                                                                                                |                               | Min. | Max.  |         |       |
| $t_{REF}$                                                                                                                                                                                                                                                                                      | Refresh Period                | —    | 64    | ms      | 1, 2  |
| $t_{REFI}$                                                                                                                                                                                                                                                                                     | Average Refresh Interval Time | —    | 7.813 | $\mu$ s |       |
| $t_{REFC}$                                                                                                                                                                                                                                                                                     | Row Refresh Cycle Time        | 75   | —     | ns      |       |
| $t_{SREX}$                                                                                                                                                                                                                                                                                     | Self Refresh Exit Time        | 10   | —     | ns      | 3     |
| 1. 4096 cycles.<br>2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake up” the device.<br>3. Self Refresh exit is asynchronous, requiring 10ns to ensure initiation. Self Refresh exit is complete in 10ns + $t_{RC}$ . |                               |      |       |         |       |

## Read Cycle

| Symbol                                                                                                           | Parameter                       | -75A |      | Units | Notes |
|------------------------------------------------------------------------------------------------------------------|---------------------------------|------|------|-------|-------|
|                                                                                                                  |                                 | Min. | Max. |       |       |
| $t_{OH}$                                                                                                         | Data Out Hold Time              | 2.45 |      | ns    |       |
| $t_{LZ}$                                                                                                         | Data Out to Low Impedance Time  | 0.6  |      | ns    |       |
| $t_{HZ3}$                                                                                                        | Data Out to High Impedance Time | 0.6  | 6.6  | ns    | 1     |
| $t_{DQZ}$                                                                                                        | DQM Data Out Disable Latency    | 3    |      | CLK   |       |
| 1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels. |                                 |      |      |       |       |

## Write Cycle

| Symbol     | Parameter                                               | -75A |      | Units |
|------------|---------------------------------------------------------|------|------|-------|
|            |                                                         | Min. | Max. |       |
| $t_{DS}$   | Data In Setup Time                                      | 1.75 |      | ns    |
| $t_{DH}$   | Data In Hold Time                                       | 1.05 |      | ns    |
| $t_{DPL}$  | Data input to Precharge                                 | 15   |      | ns    |
| $t_{DAL3}$ | Data in to Active Delay ( $\overline{CAS}$ Latency = 3) | 5    |      | CLK   |
| $t_{DQW}$  | DQM Write Mask Latency                                  | 1    |      | CLK   |



## Presence Detect Read and Write Cycle

| Symbol       | Parameter                                                     | Min. | Max. | Units   | Notes |
|--------------|---------------------------------------------------------------|------|------|---------|-------|
| $f_{SCL}$    | SCL Clock Frequency                                           |      | 100  | KHz     |       |
| $T_I$        | Noise Suppression Time Constant at SCL, SDA Inputs            |      | 100  | ns      |       |
| $t_{AA}$     | SCL Low to SDA Data Out Valid                                 | 0.3  | 3.5  | $\mu$ s |       |
| $t_{BUF}$    | Time the Bus Must Be Free before a New Transmission Can Start | 4.7  |      | $\mu$ s |       |
| $t_{HD:STA}$ | Start Condition Hold Time                                     | 4.0  |      | $\mu$ s |       |
| $t_{LOW}$    | Clock Low Period                                              | 4.7  |      | $\mu$ s |       |
| $t_{HIGH}$   | Clock High Period                                             | 4.0  |      | $\mu$ s |       |
| $t_{SU:STA}$ | Start Condition Setup Time (for a Repeated Start Condition)   | 4.7  |      | $\mu$ s |       |
| $t_{HD:DAT}$ | Data in Hold Time                                             | 0    |      | $\mu$ s |       |
| $t_{SU:DAT}$ | Data in Setup Time                                            | 250  |      | ns      |       |
| $t_r$        | SDA and SCL Rise Time                                         |      | 1    | $\mu$ s |       |
| $t_f$        | SDA and SCL Fall Time                                         |      | 300  | ns      |       |
| $t_{SU:STO}$ | Stop Condition Setup Time                                     | 4.7  |      | $\mu$ s |       |
| $t_{DH}$     | Data Out Hold Time                                            | 300  |      | ns      |       |
| $t_{WR}$     | Write Cycle Time                                              |      | 15   | ms      | 1     |

1. The write cycle time ( $t_{WR}$ ) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

## Wiring and Topology

This section contains the information needed to understand the timing relationships presented in AC Characteristics beginning on page 11. Each timing parameter is measured at the first receiving device (SDRAM DQ pin for input data, register pin for address and control, and PLL Clk input pin for clock). This section will enable the user to understand the pin numbers on the DIMM, the net structures, and the loading associated with these devices. For detailed timing analysis, contact the IBM Marketing Representative for simulation models. Modeling is strongly recommended to determine delay adders of the entire net structure.

## Pin Assignments for the 256Mb SDRAM 2 High Stack Package (Dual CS Pin)

| TOP VIEW           |    |    |                   |
|--------------------|----|----|-------------------|
| V <sub>DD</sub>    | 1  | 66 | V <sub>SS</sub>   |
| NC                 | 2  | 65 | NC                |
| V <sub>DDQ</sub>   | 3  | 64 | V <sub>SSQ</sub>  |
| NC                 | 4  | 63 | NC                |
| DQ0                | 5  | 62 | DQ3               |
| V <sub>SSQ</sub>   | 6  | 61 | V <sub>DDQ</sub>  |
| NC                 | 7  | 60 | NC                |
| NC                 | 8  | 59 | NC                |
| V <sub>DDQ</sub>   | 9  | 58 | V <sub>SSQ</sub>  |
| NC                 | 10 | 57 | NC                |
| DQ1                | 11 | 56 | DQ2               |
| V <sub>SSQ</sub>   | 12 | 55 | V <sub>DDQ</sub>  |
| NC                 | 13 | 54 | NC                |
| NC                 | 14 | 53 | NC                |
| V <sub>DDQ</sub>   | 15 | 52 | V <sub>SSQ</sub>  |
| NC                 | 16 | 51 | NC                |
| NC                 | 17 | 50 | NC                |
| V <sub>DD</sub>    | 18 | 49 | NC                |
| NC                 | 19 | 48 | V <sub>SS</sub>   |
| NC                 | 20 | 47 | DQM               |
| $\overline{WE}$    | 21 | 46 | NC                |
| $\overline{CAS}$   | 22 | 45 | CK                |
| $\overline{RAS}$   | 23 | 44 | CKE0 <sup>3</sup> |
| $\overline{CS0}^1$ | 24 | 43 | CKE1 <sup>4</sup> |
| $\overline{CS1}^2$ | 25 | 42 | A12               |
| BS0                | 26 | 41 | A11               |
| BS1                | 27 | 40 | A9                |
| A10/AP             | 28 | 39 | A8                |
| A0                 | 29 | 38 | A7                |
| A1                 | 30 | 37 | A6                |
| A2                 | 31 | 36 | A5                |
| A3                 | 32 | 35 | A4                |
| V <sub>DD</sub>    | 33 | 34 | V <sub>SS</sub>   |

66-pin Plastic TSOJ 400mil

32Mbit x 4 I/O x 4 Bank (2 High Stack)

Notes

1.  $\overline{CS0}$  selects the lower SDRAM in the stack.
2.  $\overline{CS1}$  selects the upper SDRAM in the stack.
3. CKE0 controls the clock for the lower SDRAM.
4. CKE1 controls the clock for the upper SDRAM.

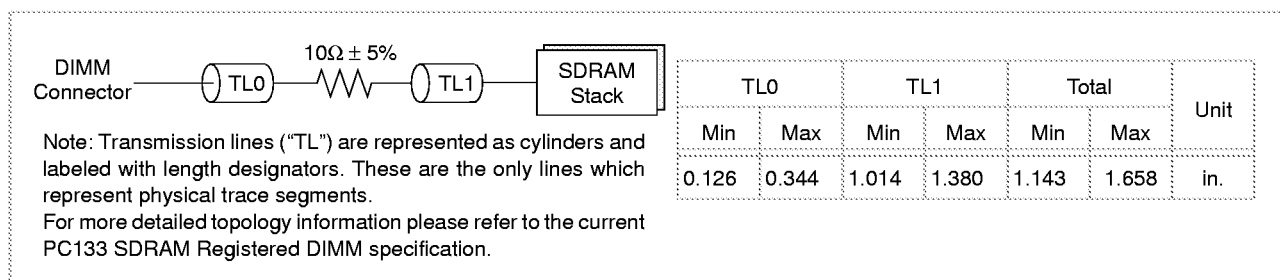
The table below describes the physical DQ wiring information for each SDRAM on the DIMM. Note that the DQ wiring is different from that described in the Block Diagram on page 4; the DQs are scrambled within the same device for wiring optimization.

## Data Wiring Cross Reference

| DQ SDRAM Designator | DQ SDRAM Pin Number | Device position to DIMM Tab Data I/O <sup>1</sup> |            |            |            |            |            |            |            |            |            |             |             |             |             |             |             |             |             |
|---------------------|---------------------|---------------------------------------------------|------------|------------|------------|------------|------------|------------|------------|------------|------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                     |                     | D0/<br>D18                                        | D1/<br>D19 | D2/<br>D20 | D3/<br>D21 | D4/<br>D22 | D5/<br>D23 | D6/<br>D24 | D7/<br>D25 | D8/<br>D26 | D9/<br>D27 | D10/<br>D28 | D11/<br>D29 | D12/<br>D30 | D13/<br>D31 | D14/<br>D32 | D15/<br>D33 | D16/<br>D34 | D17/<br>D35 |
| DQ0                 | 5                   | 3                                                 | 7          | 11         | 15         | CB2        | 18         | 23         | 27         | 31         | 32         | 36          | 40          | 45          | CB5         | 48          | 52          | 56          | 60          |
| DQ1                 | 11                  | 2                                                 | 6          | 10         | 14         | CB3        | 19         | 22         | 26         | 30         | 33         | 37          | 41          | 44          | CB4         | 49          | 53          | 57          | 61          |
| DQ2                 | 56                  | 1                                                 | 5          | 9          | 12         | CB0        | 17         | 21         | 25         | 29         | 34         | 38          | 42          | 46          | CB7         | 50          | 54          | 58          | 62          |
| DQ3                 | 62                  | 0                                                 | 4          | 8          | 13         | CB1        | 16         | 20         | 24         | 28         | 35         | 39          | 43          | 47          | CB6         | 51          | 55          | 59          | 63          |

1. These numbers can be associated with the corresponding DIMM tab pin by referencing the DIMM connector pinout on page 3 of this specification. Example: DQ14 at the DIMM tab (pin 19) is wired to SDRAM device position D3, pin 11.

## Data Topology

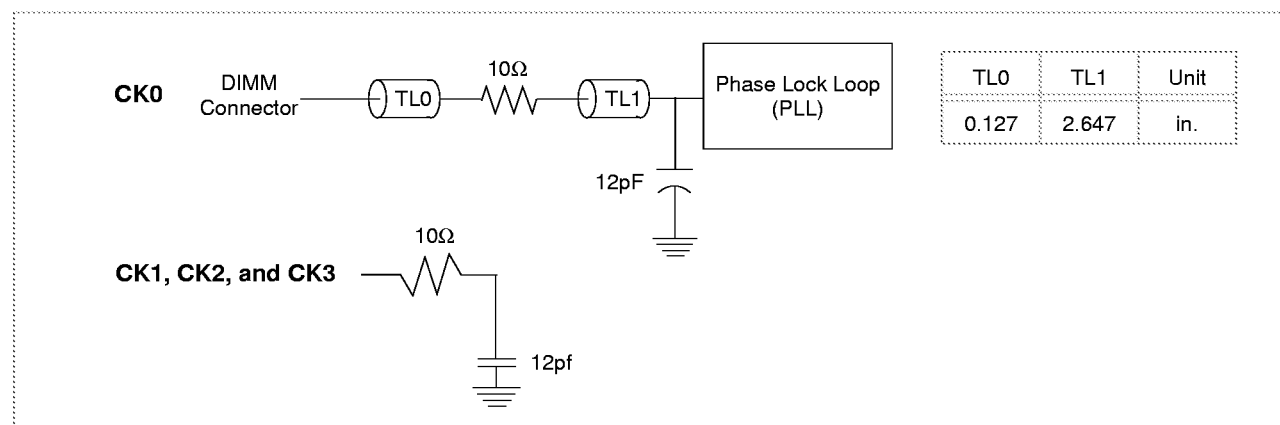


The table below describes the input wiring for each clock on the DIMM.

## Clock Input Wiring

| CK0                     | CK1            | CK2            | CK3            |
|-------------------------|----------------|----------------|----------------|
| PLL CLK Input<br>Pin 24 | Termination RC | Termination RC | Termination RC |

## Clock Topology





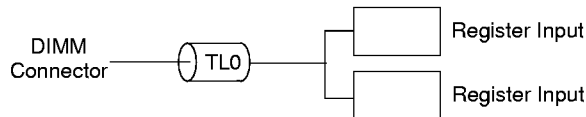


The table below describes the address and control information for each signal on the DIMM. Note that several signals are double loaded at the input of the register.

### Register Input Wiring

| Register Pin number | Register 1 Signal | Register 2 Signal | Register 3 Signal |
|---------------------|-------------------|-------------------|-------------------|
| 30                  | CLK               | CLK               | CLK               |
| 31                  | CAS               | NC                | DQMB0             |
| 33                  | RAS               | NC                | DQMB4             |
| 34                  | A1                | BS1               | DQMB1             |
| 36                  | A0                | A11               | DQMB5             |
| 37                  | A3                | A10               | A12               |
| 38                  | A2                | BS0               | A12               |
| 40                  | A5                | A8                | S0                |
| 41                  | A4                | A9                | S1                |
| 42                  | A7                | A6                | WE                |
| 43                  | A6                | A7                | WE                |
| 44                  | A9                | A4                | S3                |
| 45                  | A8                | A5                | S2                |
| 47                  | BS0               | A2                | DQMB6             |
| 48                  | A10               | A3                | DQMB2             |
| 49                  | A11               | A0                | NC                |
| 51                  | BS1               | A1                | NC                |
| 52                  | CKE0              | RAS               | DQMB7             |
| 54                  | CKE0              | CAS               | DQMB3             |

### Address/Control Signal Topology



| TL0   |       | Unit |
|-------|-------|------|
| Min   | Max   |      |
| 0.199 | 1.223 | in.  |

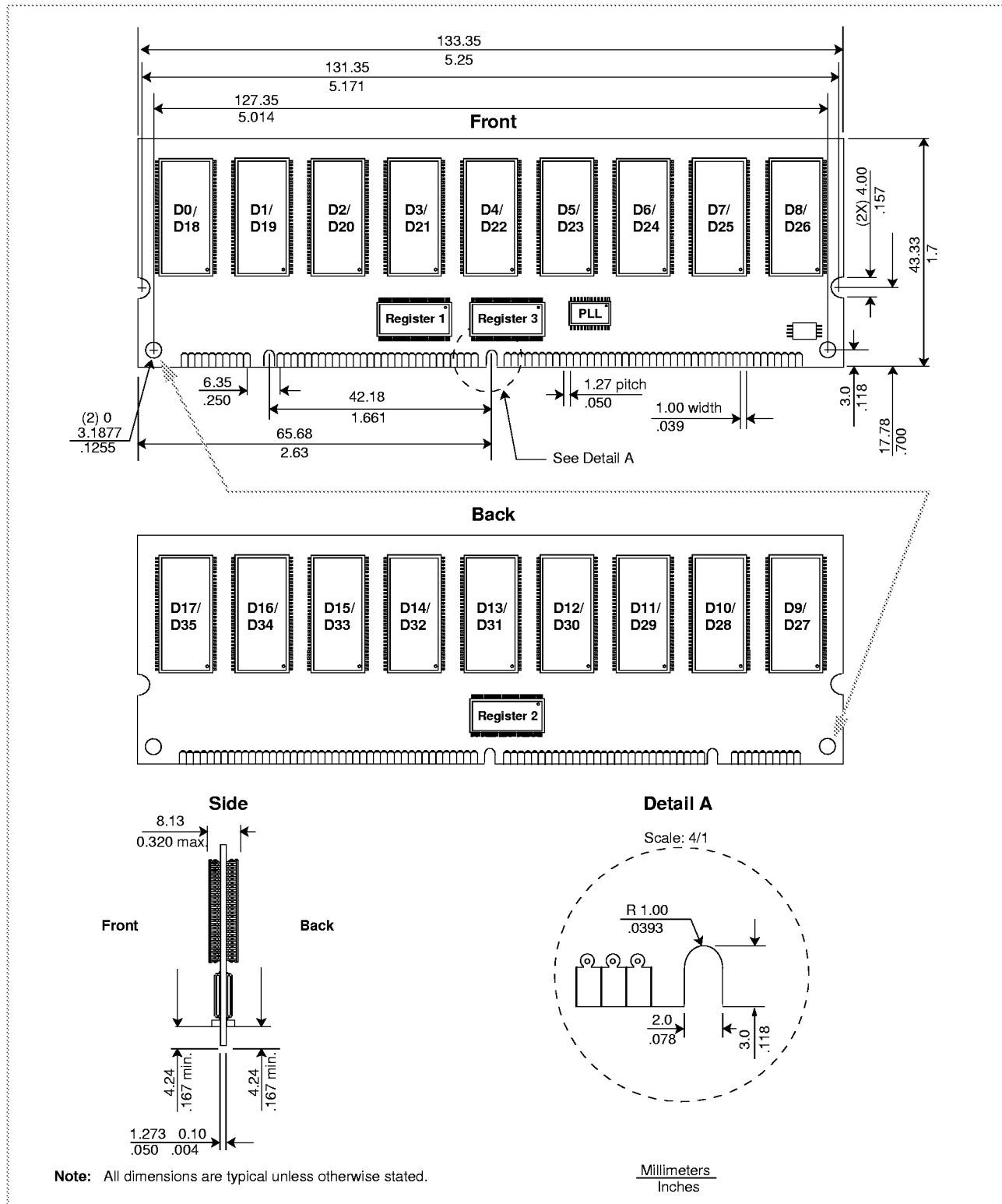
Note: Each Signal has two register input loads with the exception of DQMBs and Chip Selects (s0-S3) which have one. For more detailed topology information please refer to the current PC133 SDRAM Registered DIMM specification.

### Functional Description and Timing Diagrams

Refer to the IBM PC133 256Mb Synchronous DRAM datasheet (Document 29L0000.E36980) for the functional description and timing diagrams for buffered-mode operation.

Refer to the IBM Application Notes *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

## Layout Drawing





## Revision Log

| Rev  | Contents of Modification |
|------|--------------------------|
| 4/99 | Initial release.         |
| 8/99 | Removed Preliminary      |



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