19-2862; Rev 1; 2/05

750mW Audio Amplifiers with Headphone Amp, Microphone Preamp, and Input Mux

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General Description

The MAX9765/MAX9766/MAX9767 family combines speaker, headphone, and microphone amplifiers, all in a small thin QFN package. The MAX9765 is targeted at stereo speaker playback applications and includes a stereo bridge-tied load (BTL) speaker amp, stereo headphone amp, single-ended output mic amp, input MUX, and I²C control. The MAX9766 is targeted at mono speaker playback applications and includes a mono BTL speaker amp, stereo headphone amp, differential output mic amp, input MUX, and I²C control. The MAX9767 is targeted at applications that do not require a headphone amp and includes a stereo BTL speaker amp, differential output mic amp, and parallel control.

These devices operate from a single 2.7V to 5.5V supply. A high 95dB PSRR allows these devices to operate from noisy supplies without additional power conditioning. An ultra-low 0.003% THD+N ensures clean, low distortion amplification of the audio signal. Patented click-and-pop suppression eliminates audible transients on power and shutdown cycles.

In speaker mode, the amplifiers can deliver up to 750mW of continuous average power into a 4Ω load. In headphone mode, the amplifier can deliver up to 65mW of continuous average power into a 16Ω load. The gain of the amplifiers is externally set, allowing maximum flexibility in optimizing output levels for a given load. The MAX9765/MAX9766 also feature a 2:1 input multiplexer, allowing multiple audio sources to be selected. The various functions are controlled by either an I²C-compatible (MAX9765/MAX9766) or simple parallel control interface (MAX9767).

All devices include two low-noise microphone preamps, a differential amp for internal microphones, and a single-ended amplifier for additional external microphones. A microphone bias output is provided, reducing external component count.

The MAX9765/MAX9766/MAX9767 are available in a thermally efficient 32-pin thin QFN package (5mm × 5mm × 0.8mm). All devices have short-circuit and thermal-overload protection (OVP) and are specified over the extended -40°C to +85°C temperature range.

Applications

PDA Audio Systems
Notebooks
Tablet PCs
Digital Cameras
Cell Phones

Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification defined by Philips.

Features

- **750mW BTL Stereo Speaker Amplifier**
- **65mW Stereo Headphone Amplifier**
- **2.7V to 5.5V Single-Supply Operation**
- **Patented Click-and-Pop Suppression**
- **Low 0.003% THD+N**
- **Low Quiescent Current: 13mA**
- **Low-Power Shutdown Mode: 5µA**
- **MUTE Function**
- **Headphone Sense Input**
- **Stereo 2:1 Input Multiplexer**
- **Optional 2-Wire, I²C-Compatible, or Parallel Interface**
- **Small 32-Pin Thin QFN (5mm × 5mm × 0.8mm) Package**

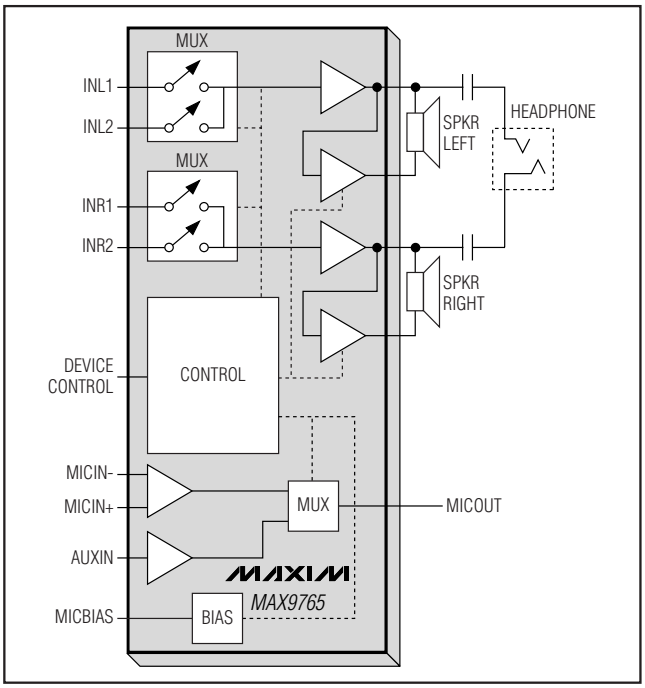
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9765ETJ	-40°C to +85°C	32 Thin QFN-EP*
MAX9766ETJ	-40°C to +85°C	32 Thin QFN-EP*
MAX9767ETJ	-40°C to +85°C	32 Thin QFN-EP*

**EP = Exposed paddle.*

Pin Configurations and Functional Diagrams appear at end of data sheet.

Simplified Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....+6V
SV_{DD} to GND .....+6V
SV_{DD} to V_{DD} .....-0.3V
PV_{DD} to V_{DD} .....±0.3V
PGND to GND .....±0.3V
All Other Pins to GND .....-0.3V to (V_{DD} + 0.3V)
Output Short-Circuit Duration (to V_{DD} or GND) .....Continuous
Continuous Input Current (into any pin except power-supply and output pins) .....±20mA

Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 26.3mW/°C above +70°C) ...2105.3mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = 3.0V, GND = 0, HPS = MUTE = GND, $\overline{SHDN}$ = 3V, C_{BIAS} = 1µF, R_{IN} = R_F = 15kΩ, R_L = ∞. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}/PV_{DD}	Inferred from PSRR test		2.7		5.5	V
Quiescent Supply Current (I_{VDD} + I_{PVDD})	I_{DD}	Speaker mode	MAX9765/MAX9767		12	28	mA
			MAX9766		7	17	
		Headphone mode, HPS = V_{DD}			7	17	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND			5	18	µA
Switching Time	t_{SW}	Gain or input switching (MAX9765/MAX9766)			10		µs
Turn-On/Turn-Off Time	$t_{ON/OFF}$	C_{BIAS} = 1µF, settled to 90%			250		ms
		C_{BIAS} = 0.1µF, settled to 90%			25		
Input Bias Current	I_{BIAS}				50		nA
Thermal Shutdown Threshold					150		°C
Thermal Shutdown Hysteresis					8		°C
Output Short-Circuit Current		To V_{DD} or GND			1.2		A
STANDBY SUPPLY (SV_{DD})							
Standby Current	I_{SVDD}	V_{BIAS} = 1.25V, V_{DD} = 0V			230	400	µA
		V_{BIAS} = 1.5V, V_{DD} = 3V				5	
OUTPUT AMPLIFIERS (SPEAKER MODE)							
Output Offset Voltage	V_{OS}	V_{OUT_+} - V_{OUT_-}, A_V = 1V/V			10	45	mV
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 5.5V		72	85		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}			72		
Output Power	P_{OUT}	f_{IN} = 1kHz, THD+N = 1%, T_A = +25°C (Note 2)	R_L = 8Ω		450		mW
			R_L = 4Ω	400	750		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz	P_{OUT} = 200mW, R_L = 8Ω		0.033		%
			P_{OUT} = 400mW, R_L = 4Ω		0.065		
Signal-to-Noise Ratio	SNR	R_L = 8Ω, $V_{OUT_}$ = 1.4V_{RMS}, BW = 22Hz to 22kHz			89		dB

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Capacitive Load Drive	C_L	No sustained oscillations			400		pF
Slew Rate	SR				1.4		V/µs
Crosstalk		f_{IN} = 10kHz			73		dB
OUTPUT AMPLIFIERS (HEADPHONE MODE)							
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 5.5V			95		dB
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}			75		
		f = 20kHz, V_{RIPPLE} = 200mV_{P-P}			50		
Output Power	P_{OUT}	f_{IN} = 1kHz, THD+N = 1%, T_A = +25°C (Note 2)	R_L = 32Ω		40		mW
			R_L = 16Ω	35	65		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, BW = 22Hz to 22kHz	V_{OUT} = 0.7V_{RMS}, R_L = 10kΩ		0.002		%
			P_{OUT} = 15mW, R_L = 32Ω		0.005		
			P_{OUT} = 30mW, R_L = 16Ω		0.004		
Signal-to-Noise Ratio	SNR	R_L = 8Ω, $V_{OUT_}$ = 1.4V_{RMS}, BW = 20Hz to 22kHz			89		dB
Slew Rate	SR				0.7		V/µs
Maximum Capacitive Load Drive	C_L	No sustained oscillations			200		pF
Crosstalk		f_{IN} = 10kHz			79		dB
BIAS VOLTAGE (BIAS)							
BIAS Voltage	V_{BIAS}			1.4	1.5	1.6	V
Output Resistance	R_{BIAS}				50		kΩ
MICROPHONE AMPLIFIER GENERAL							
Output Voltage Swing	V_{OUT}	R_L = 100kΩ	V_{DD} - V_{OH}		35	70	mV
			V_{OL} - GND		50	400	
		R_L = 2kΩ	V_{DD} - V_{OH}		80	150	
			V_{OL} - GND		70	400	
Slew Rate	SR	A_V = 10dB			0.6		V/µs
Output Short-Circuit Current		To V_{DD} or GND			10		mA
Maximum Capacitive Load Drive	C_L	No sustained oscillations			50		pF
DIFFERENTIAL INPUT AMPLIFIER (MICIN+, MICIN-)							
Input Offset Voltage	V_{OS}				2	5	mV
Input Noise-Voltage Density	e_N	f_{IN} = 1kHz	A_V = 20dB		31		nV/√Hz
			A_V = 40dB		11.6		
Total Harmonic Distortion Plus Noise	THD+N	V_{DD} = 3V, V_{OUT} = 0.35V_{RMS}, A_V = 10dB, f_{IN} = 1kHz, BW = 22Hz to 22kHz			0.01		%
Small-Signal Bandwidth	BW_{-3dB}	A_V = 40dB, V_{OUT} = 100mV_{P-P}			300		kHz
Input Resistance	R_{IN}	MICIN_ to GND			100		kΩ

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Resistance Matching	R_{MATCH}				1		%
Differential Gain Accuracy	A_{VDIFF}	MAX9765, A_V = 4dB to 39dB			2	4	%
		MAX9766, A_V = 10dB to 45dB			2	4	
		MAX9767, A_V = 10dB, 20dB, 30dB			2	4	
Common-Mode Rejection Ratio	CMRR	A_V = 10dB, f_{IN} = 1kHz, V_{CM} = 200mV_{P-P}, R_S = 2kΩ			60		dB
Power-Supply Rejection Ratio	PSRR	A_V = 10dB, output referred	V_{DD} = 2.7V to 5.5V	62	80		dB
			f = 1kHz, V_{RIPPLE} = 200mV_{P-P}		80		
			f = 20kHz, V_{RIPPLE} = 200mV_{P-P}		68		
Common-Mode Input Voltage Range	V_{CM}				1		V
SINGLE-ENDED INPUT AMPLIFIER (AUXIN)							
Input Offset Voltage	V_{OS}				4	10	mV
Input Noise-Voltage Density	e_N	A_V = 20dB, f_{IN} = 1kHz			73		nV/√Hz
Total Harmonic Distortion Plus Noise	THD+N	A_V = 10dB, f_{IN} = 1kHz, BW = 22Hz to 22kHz, V_{OUT} = 0.7V_{RMS}			0.01		%
Small-Signal Bandwidth	BW_{-3dB}	A_V = 20dB, V_{OUT} = 100mV_{P-P}			200		kHz
Input Resistance	R_{IN}				100		kΩ
Voltage Gain Accuracy	A_V				4		%
Power-Supply Rejection Ratio	PSRR	A_V = 10dB, output referred	V_{DD} = 2.7V to 5.5V	65	80		dB
			f = 1kHz, V_{RIPPLE} = 200mV_{P-P}		76		
			f = 20kHz, V_{RIPPLE} = 200mV_{P-P}		58		
MICROPHONE BIAS OUTPUT (MICBIAS)							
Microphone Bias Output Voltage	$V_{MICBIAS}$	V_{DD} = 2.7V to 5.5V, I_{LOAD} = 500µA		2.4	2.5	2.6	V
Output Noise-Voltage Density	e_N	f = 1kHz			52		nV/√Hz
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.7V to 5.5V		63	72		dB
		f_{IN} = 1kHz, V_{RIPPLE} = 200mV_{P-P}			70		
DIGITAL INPUTS (MUTE, $\overline{SHDN}$, INT/$\overline{EXT}$)							
Input Voltage High	V_{IH}			2			V
Input Voltage Low	V_{IL}					0.8	V
Input Leakage Current	I_{IN}					±1	µA
MAX9767 MICGAIN INPUT (TRI-STATE PIN))							
Input Voltage High	V_{IH}				V_{DD}		V
Input Voltage Low	V_{IL}				GND		V
Input Voltage Mid	V_{IZ}				FLOAT		V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = 3.0V, GND = 0, HPS = MUTE = GND, $\overline{SHDN}$ = 3V, C_{BIAS} = 1µF, R_{IN} = R_F = 15kΩ, R_L = ∞. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HEADPHONE SENSE INPUT (HPS)						
Input Voltage High	V_{IH}		0.9 x V_{DD}			V
Input Voltage Low	V_{IL}				0.7 x V_{DD}	V
Input Leakage Current	I_{IN}				±1	µA
2-WIRE SERIAL INTERFACE (SCL, SDA, ADD) (MAX9765/MAX9766)						
Input Voltage High	V_{IH}	V_{DD} > 3.6V	3			V
		V_{DD} ≤ 3.6V	2			
Input Voltage Low	V_{IL}				0.8	V
Input Hysteresis				0.2		V
Input High Leakage Current	I_{IH}	V_{IN} = 3V			±1	µA
Input Low Leakage Current	I_{IL}	V_{IN} = 0V			±1	µA
Input Capacitance	C_{IN}			10		pF
Output Voltage Low	V_{OL}	I_{OL} = 3mA			0.4	V
Output Current High	I_{OH}	V_{OH} = 3V			1	µA
TIMING CHARACTERISTICS (MAX9765/MAX9766)						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
Clock Period Low	t_{LOW}		1.3			µs
Clock Period High	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	(Note 3)	0		0.9	µs
Receive SCL/SDA Rise Time	t_R	(Note 4)	20 + 0.1C_B		300	ns
Receive SCL/SDA Fall Time	t_F	(Note 4)	20 + 0.1C_B		300	ns
Transmit SDA Fall Time	t_F	(Note 4)	20 + 0.1C_B		250	ns
Pulse Width of Suppressed Spike	t_{SP}	(Note 5)		50		ns

Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.

Note 2: P_{OUT} limits are tested by a combination of electrical and guaranteed by design.

Note 3: A device must provide a hold time of at least 300ns for the SDA signal to bridge the undefined region of SCL's falling edge.

Note 4: C_B = total capacitance of one of the bus lines in picofarads. Device tested with C_B = 400pF. 1kΩ pullup resistors connected from SDA/SCL to V_{DD}.

Note 5: Input filters on SDA, SCL, and ADD suppress noise spikes less than 50ns.

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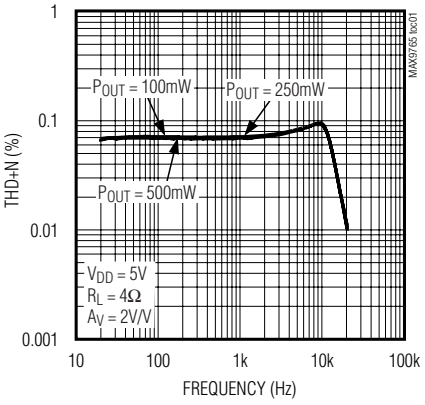
Typical Operating Characteristics

(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SPEAKER MODE)



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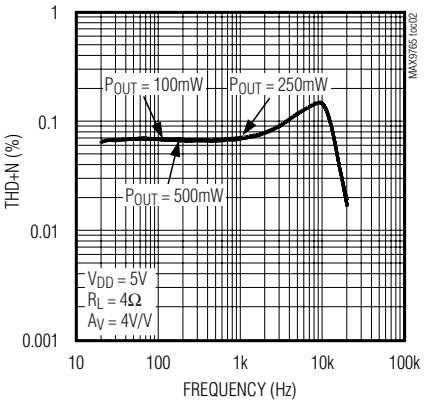

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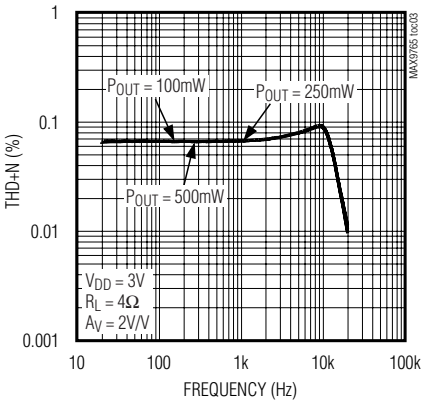

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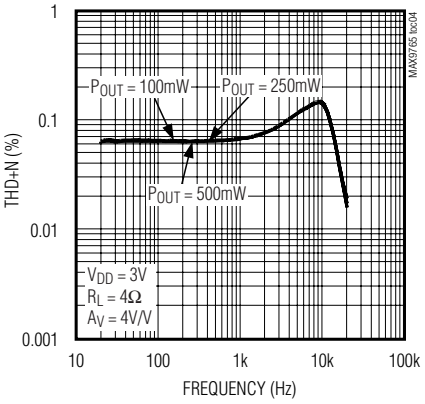

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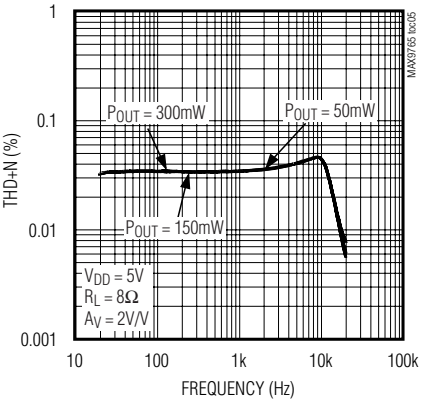

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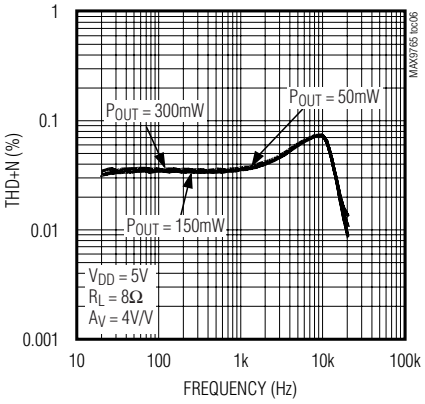

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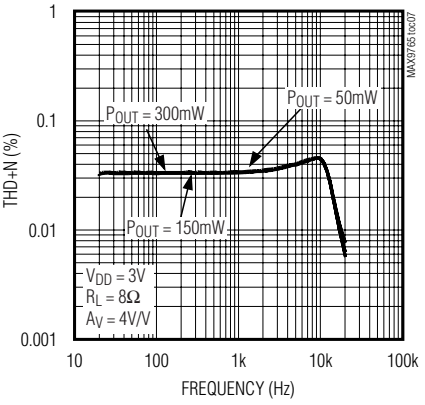

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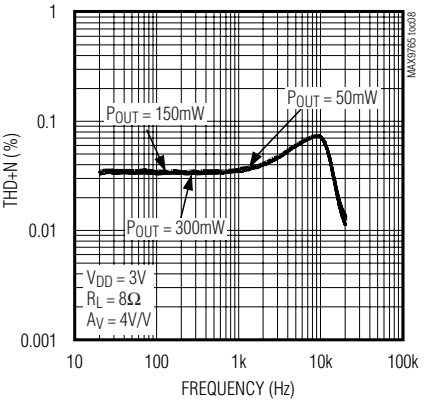
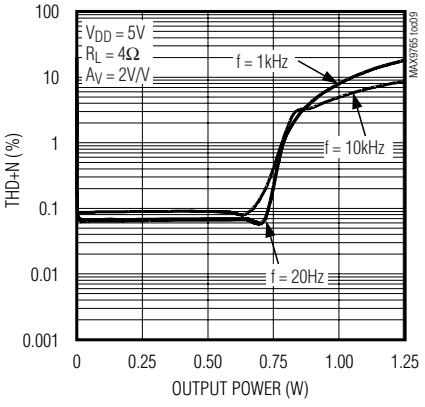


TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



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Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

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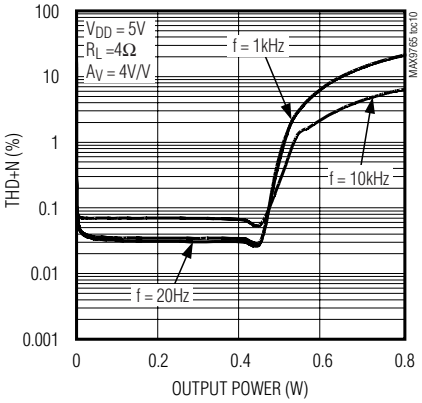

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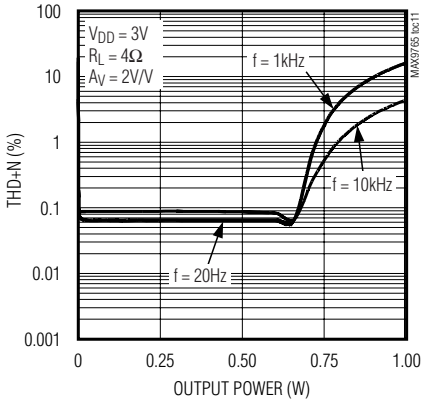

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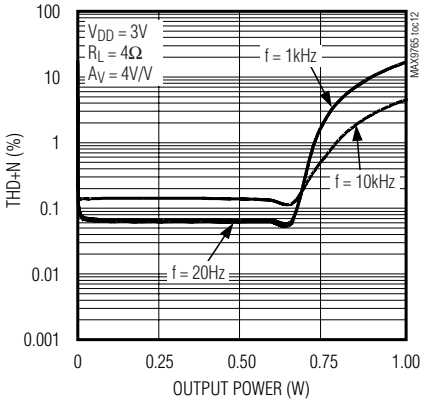

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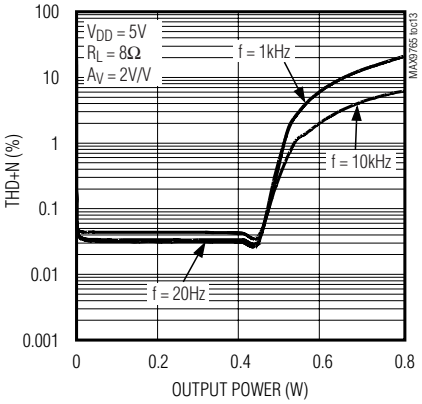

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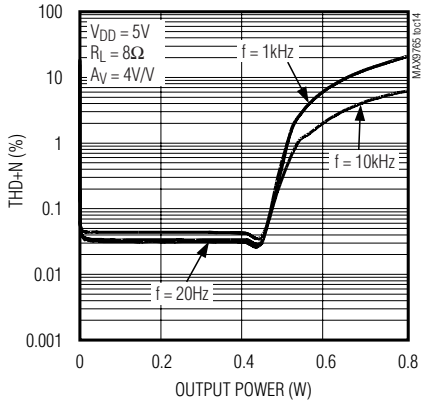
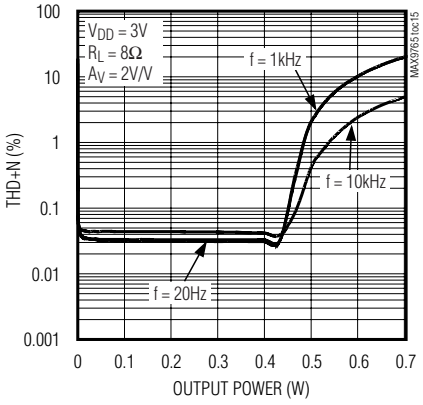
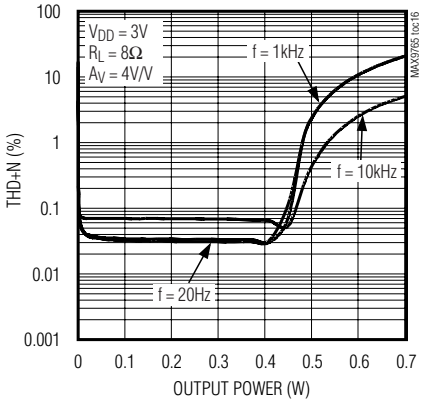


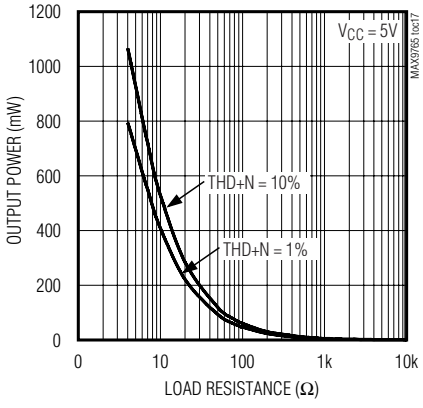
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



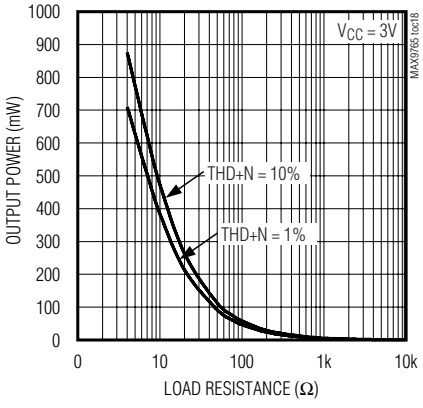
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (SPEAKER MODE)



OUTPUT POWER vs. LOAD RESISTANCE (SPEAKER MODE)



OUTPUT POWER vs. LOAD RESISTANCE (SPEAKER MODE)



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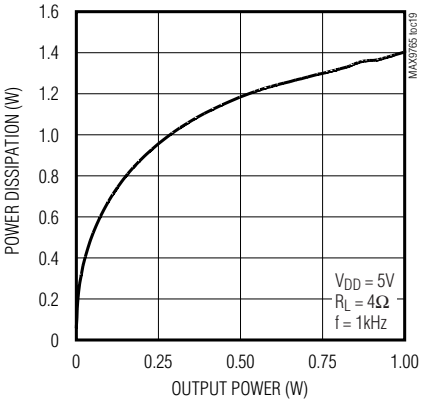
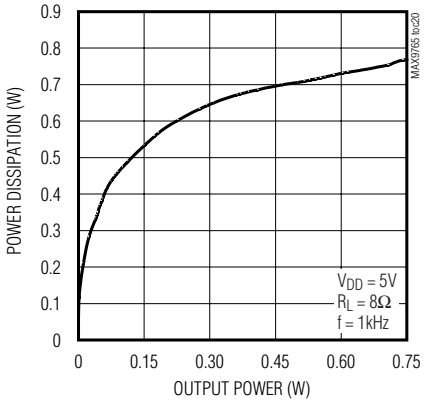
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

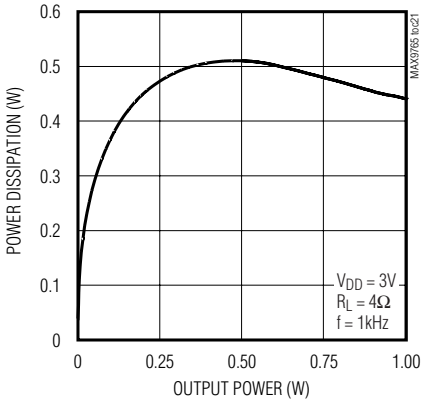
POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



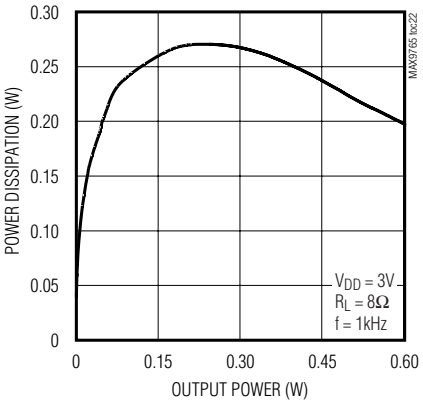
POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



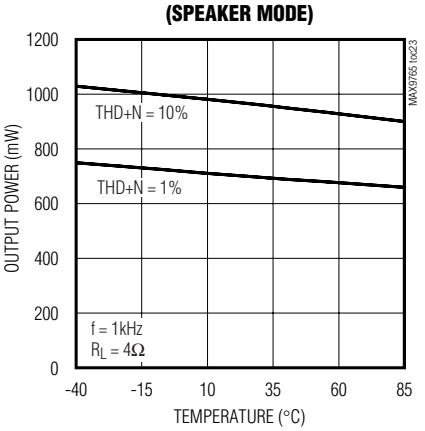
POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



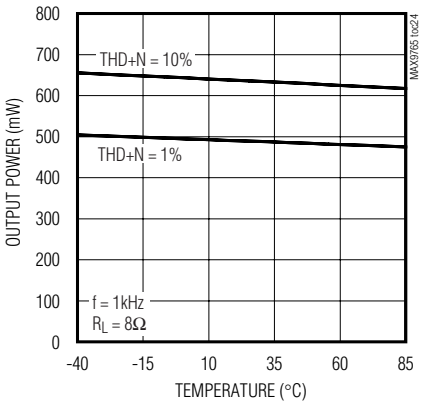
POWER DISSIPATION vs. OUTPUT POWER (SPEAKER MODE)



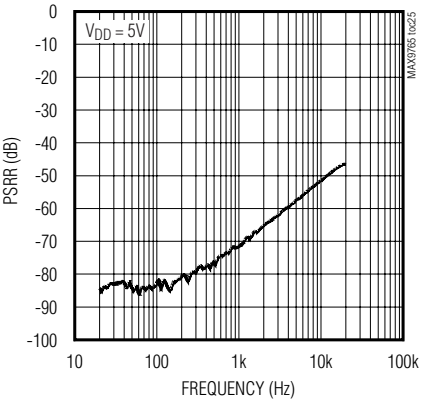
OUTPUT POWER vs. TEMPERATURE (SPEAKER MODE)



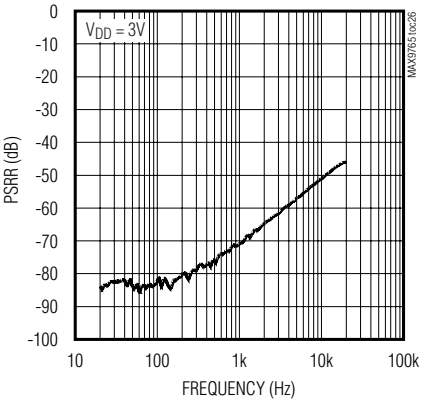
OUTPUT POWER vs. TEMPERATURE (SPEAKER MODE)



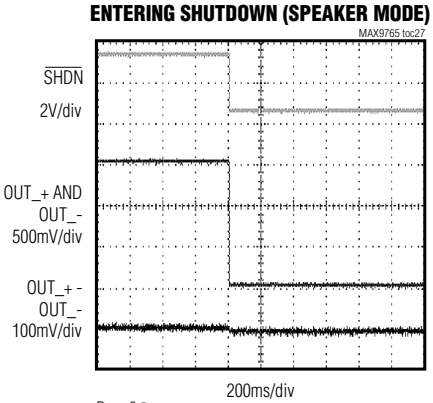
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SPEAKER MODE)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SPEAKER MODE)



ENTERING SHUTDOWN (SPEAKER MODE)



RL = 8Ω
INPUT AC-COUPLED TO GND

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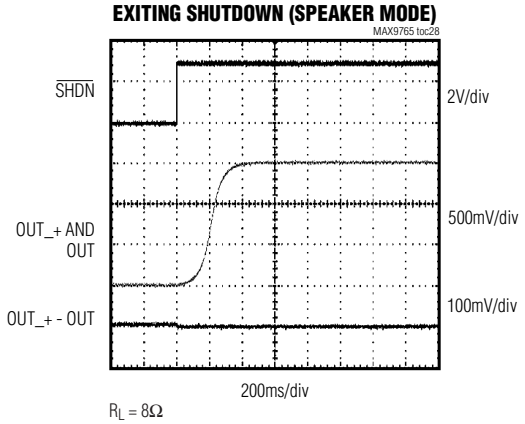
Typical Operating Characteristics (continued)

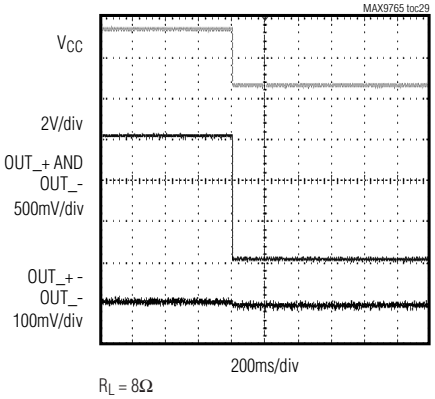
(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

EXITING SHUTDOWN (SPEAKER MODE)



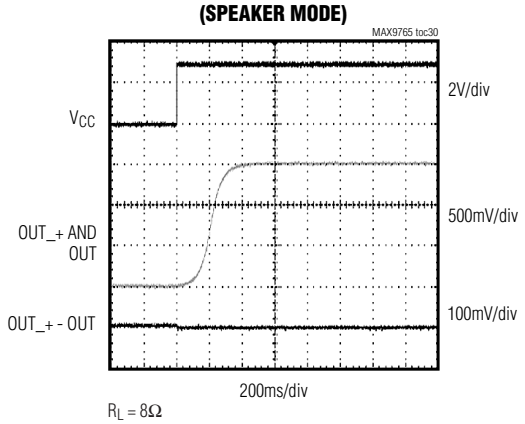
R_L = 8Ω
INPUT AC-COUPLED TO GND
C_{BIAS} = 1µF

ENTERING POWER-DOWN (SPEAKER MODE)



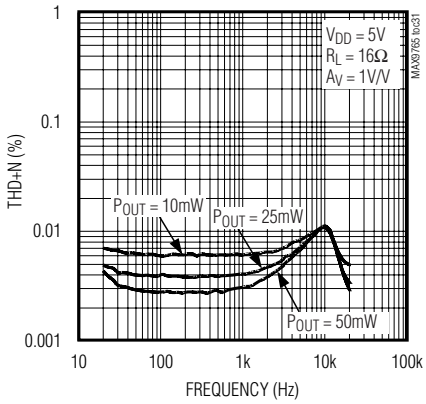
R_L = 8Ω
INPUT AC-COUPLED TO GND

POWER-UP (SPEAKER MODE)

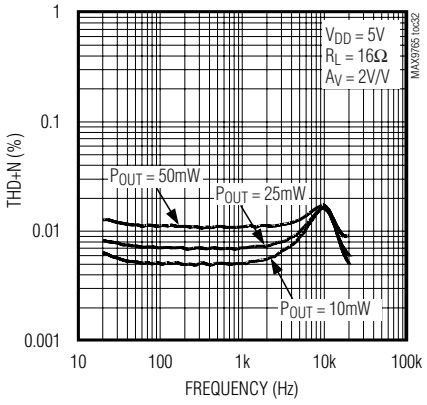


R_L = 8Ω
INPUT AC-COUPLED TO GND
C_{BIAS} = 1µF

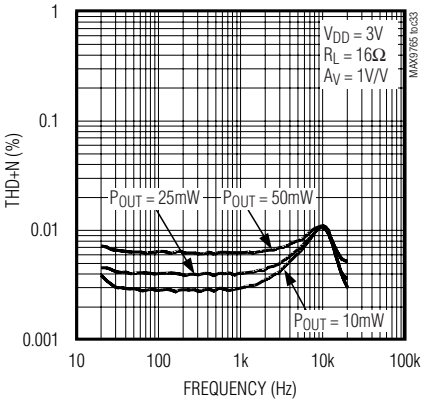
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



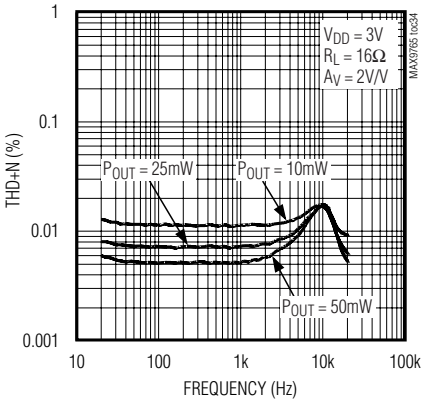
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



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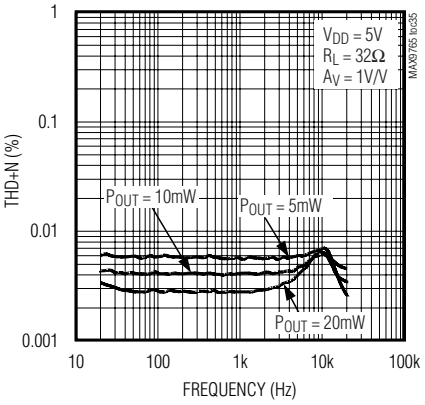
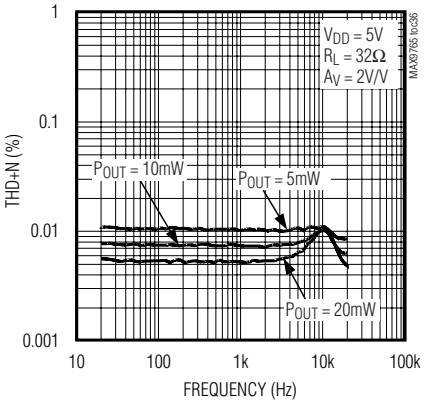
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

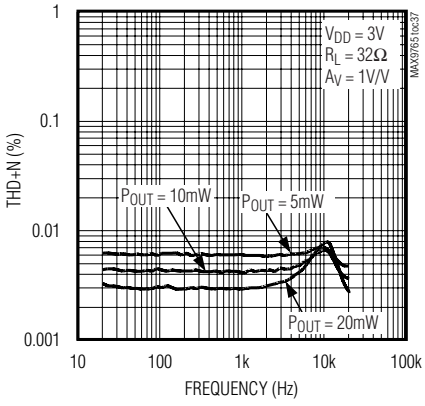
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



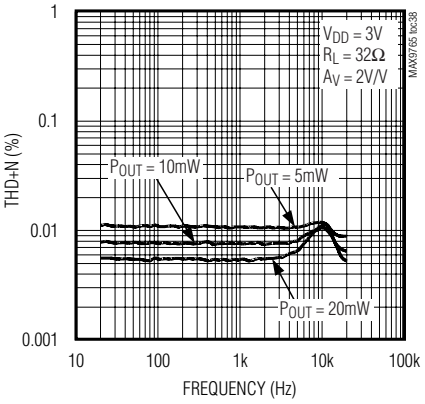
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



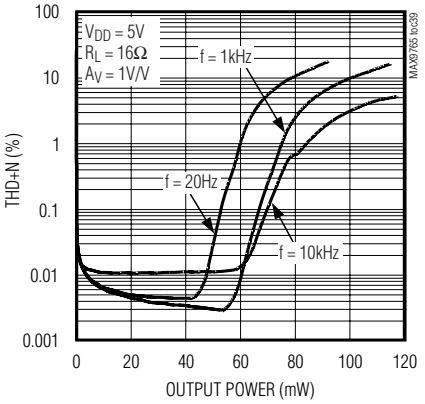
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



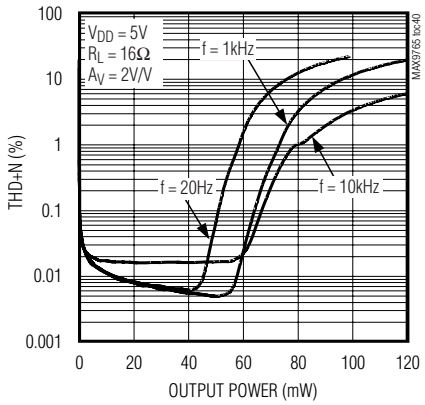
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (HEADPHONE MODE)



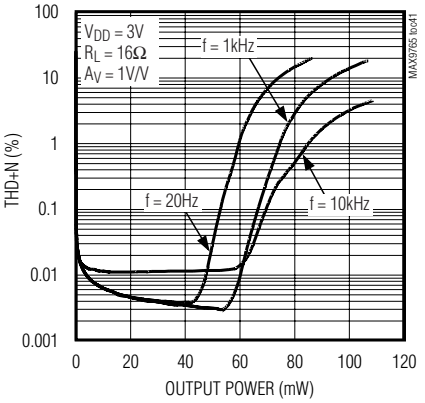
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



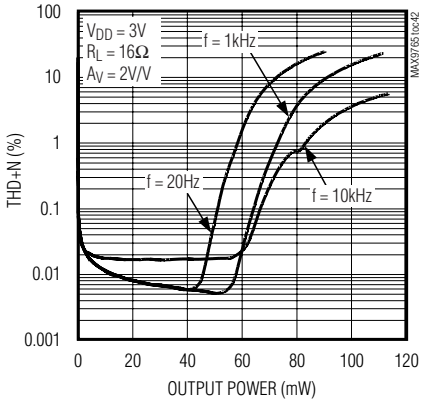
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



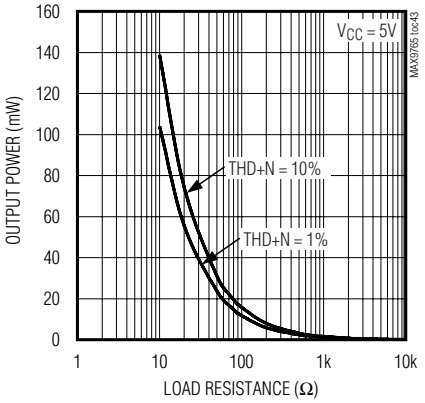
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER (HEADPHONE MODE)



OUTPUT POWER vs. LOAD RESISTANCE (HEADPHONE MODE)



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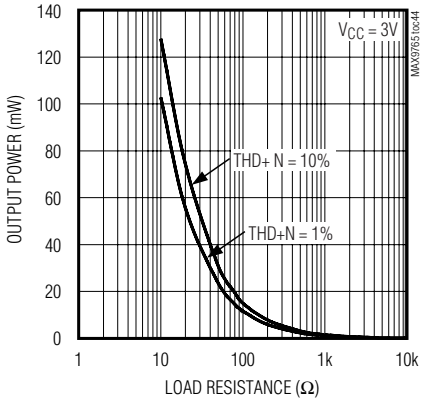
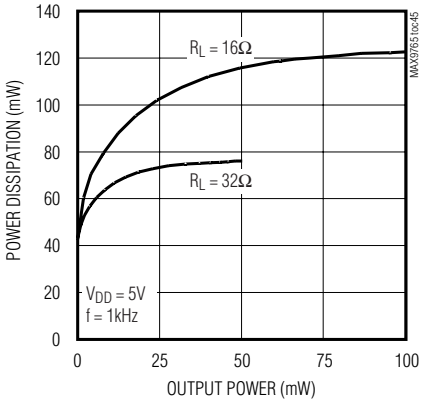
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

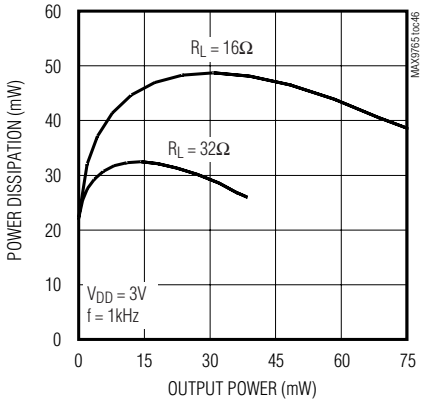
OUTPUT POWER vs. LOAD RESISTANCE (HEADPHONE MODE)



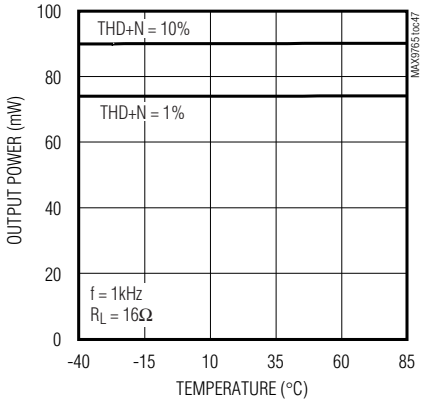
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



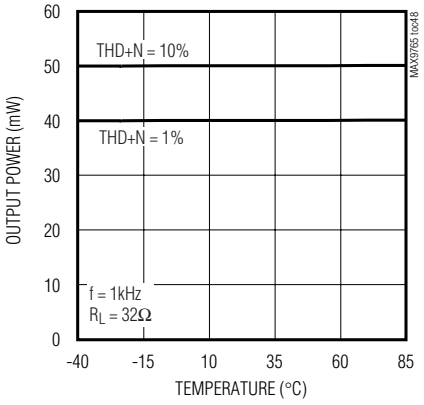
POWER DISSIPATION vs. OUTPUT POWER (HEADPHONE MODE)



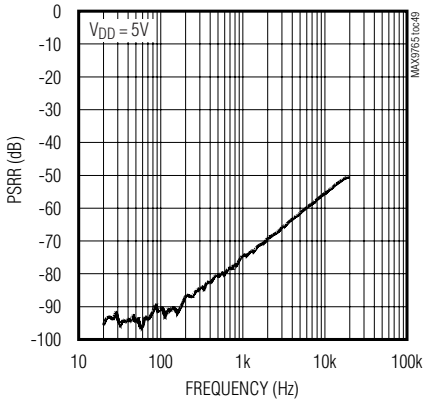
OUTPUT POWER vs. TEMPERATURE (HEADPHONE MODE)



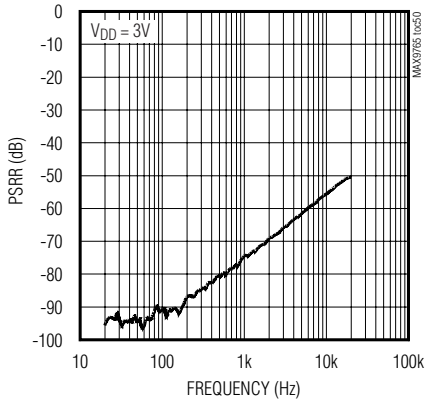
OUTPUT POWER vs. TEMPERATURE (HEADPHONE MODE)



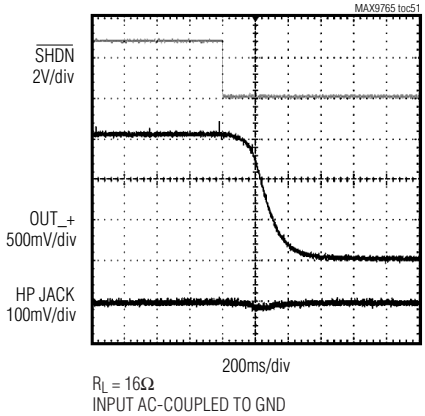
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (HEADPHONE MODE)



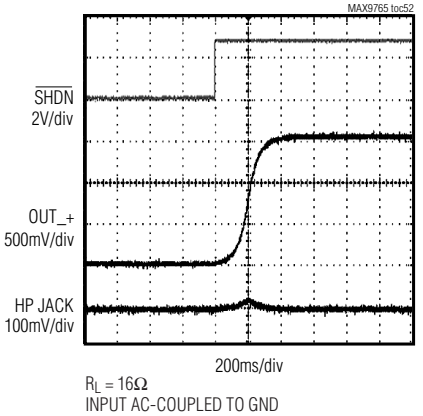
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (HEADPHONE MODE)



ENTERING SHUTDOWN (HEADPHONE MODE)



EXITING SHUTDOWN (HEADPHONE MODE)



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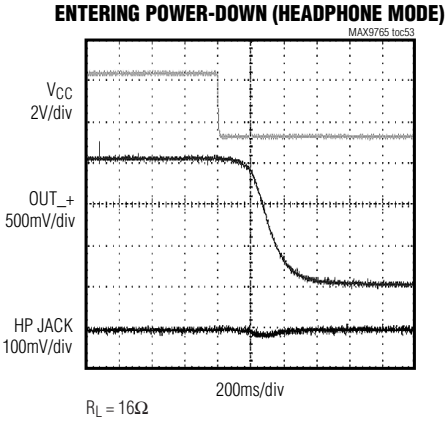
Typical Operating Characteristics (continued)

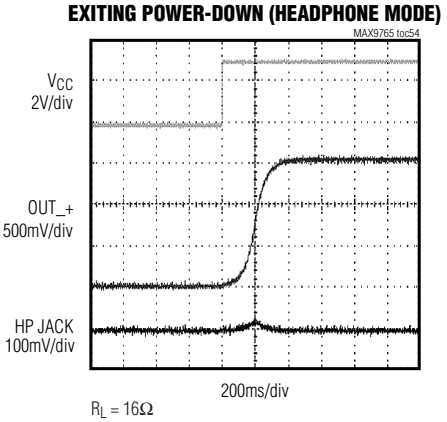
(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

ENTERING POWER-DOWN (HEADPHONE MODE)



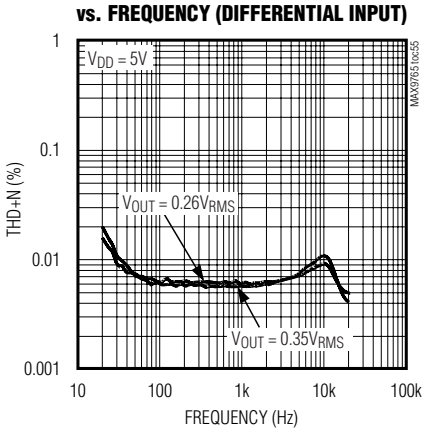
R_L = 16Ω
INPUT AC-COUPLED TO GND

EXITING POWER-DOWN (HEADPHONE MODE)

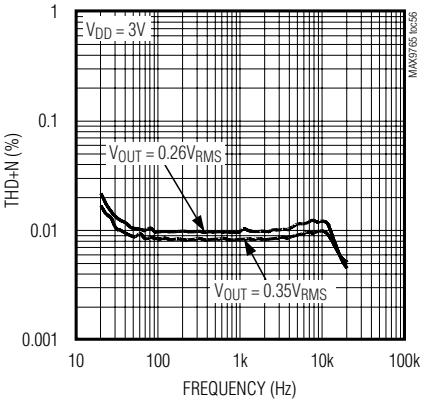


R_L = 16Ω
INPUT AC-COUPLED TO GND

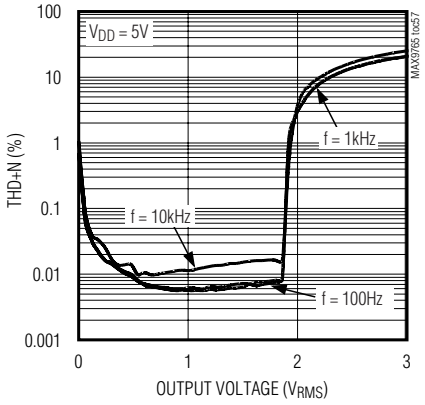
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIFFERENTIAL INPUT)



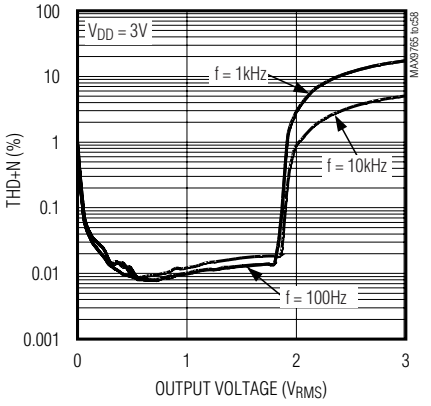
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (DIFFERENTIAL INPUT)



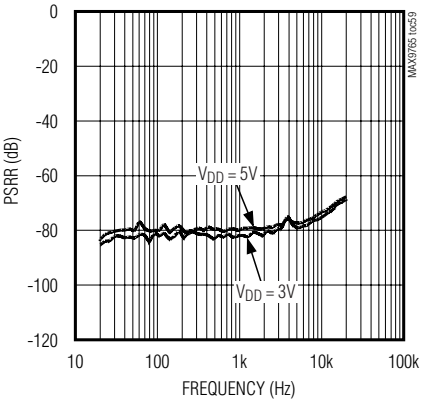
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT AMPLITUDE (DIFFERENTIAL INPUT)



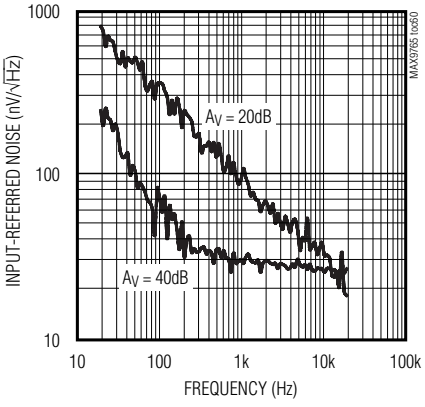
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT AMPLITUDE (DIFFERENTIAL INPUT)



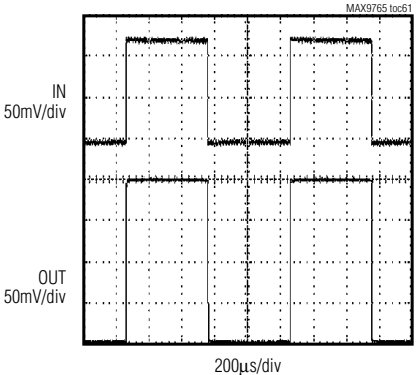
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DIFFERENTIAL INPUT)



INPUT-REFERRED NOISE (DIFFERENTIAL MICROPHONE AMPLIFIER)



DIFFERENTIAL MICROPHONE AMPLIFIER SMALL-SIGNAL TRANSIENT RESPONSE



A_V = 4dB
f_{IN} = 1kHz

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Typical Operating Characteristics (continued)

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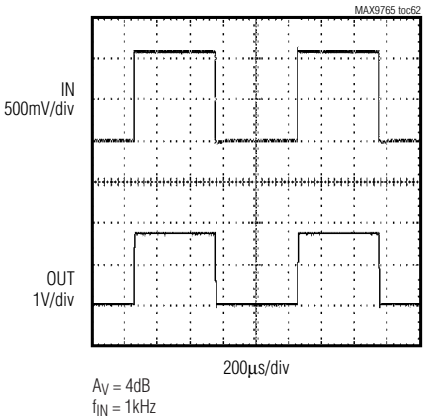
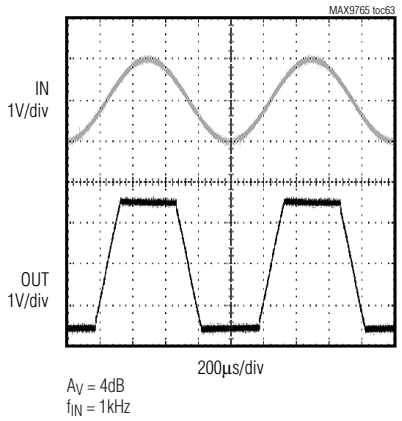
(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

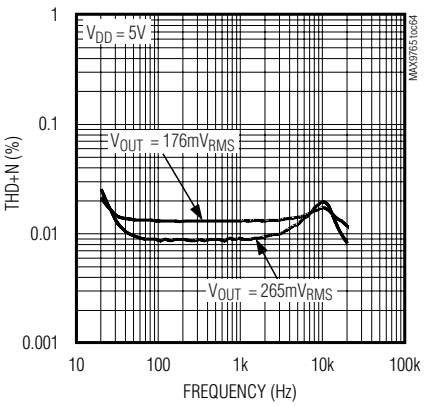
DIFFERENTIAL MICROPHONE AMPLIFIER LARGE-SIGNAL TRANSIENT RESPONSE



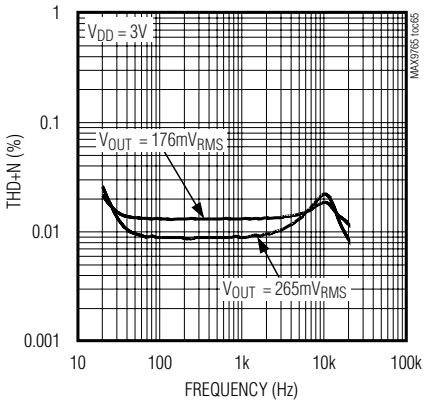
DIFFERENTIAL MICROPHONE AMPLIFIER OVERDRIVEN OUTPUT



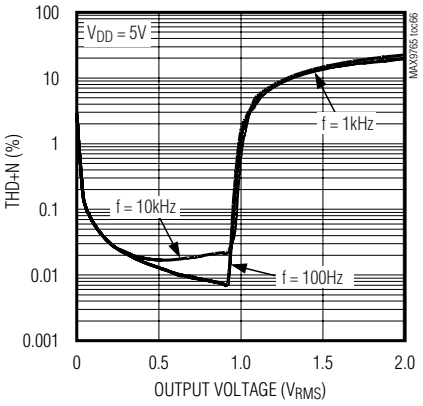
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SINGLE-ENDED INPUT)



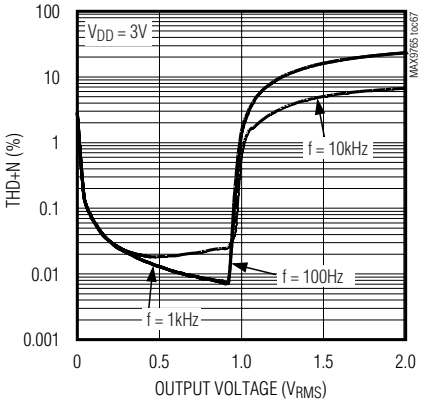
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY (SINGLE-ENDED INPUT)



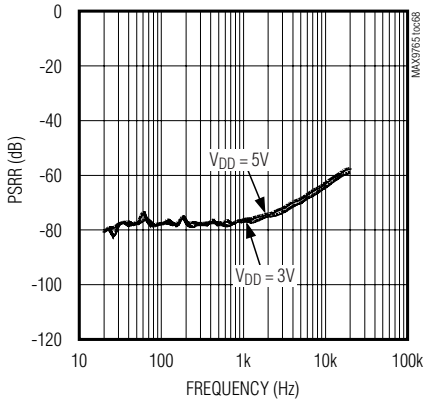
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT AMPLITUDE (SINGLE-ENDED INPUT)



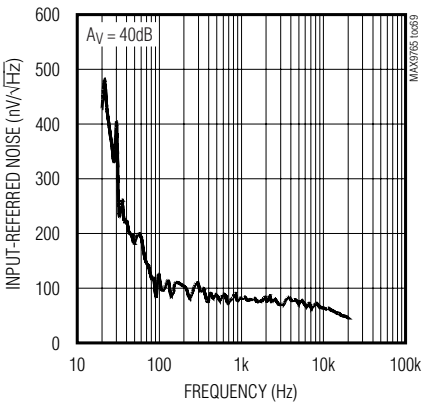
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT AMPLITUDE (SINGLE-ENDED INPUT)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (SINGLE-ENDED INPUT)



INPUT-REFERRED NOISE (SINGLE-ENDED INPUT MICROPHONE AMPLIFIER)



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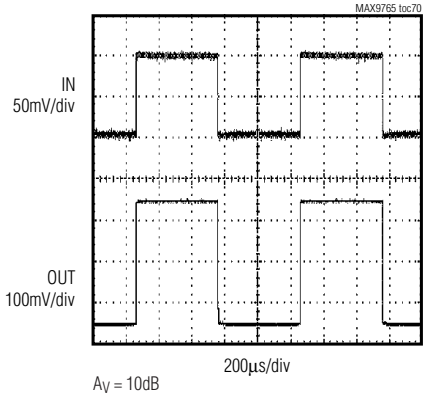
Typical Operating Characteristics (continued)

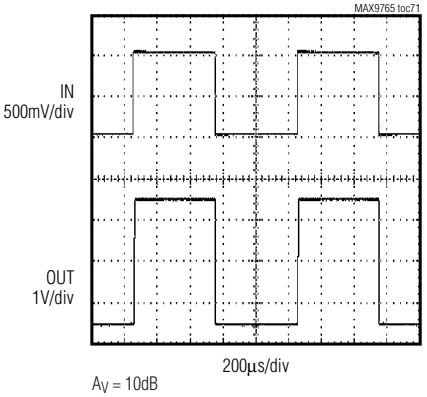
(V_{DD} = PV_{DD} = 5V, BW = 22Hz to 22kHz, T_A = +25°C, unless otherwise noted.)

SINGLE-ENDED MICROPHONE AMPLIFIER SMALL-SIGNAL TRANSIENT RESPONSE



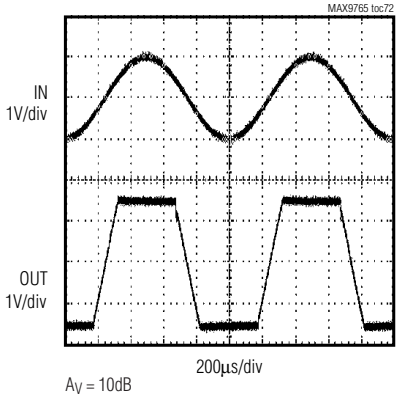
A_V = 10dB
f_{IN} = 1kHz

SINGLE-ENDED MICROPHONE AMPLIFIER LARGE-SIGNAL TRANSIENT RESPONSE



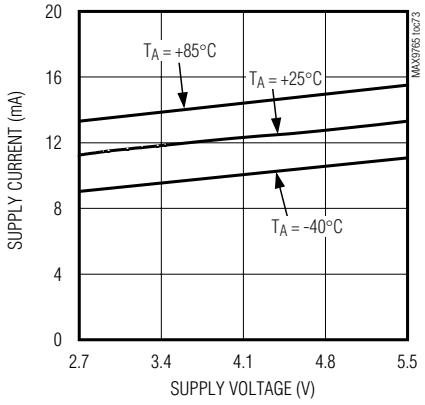
A_V = 10dB
f_{IN} = 1kHz

SINGLE-ENDED MICROPHONE AMPLIFIER OVERDRIVEN OUTPUT

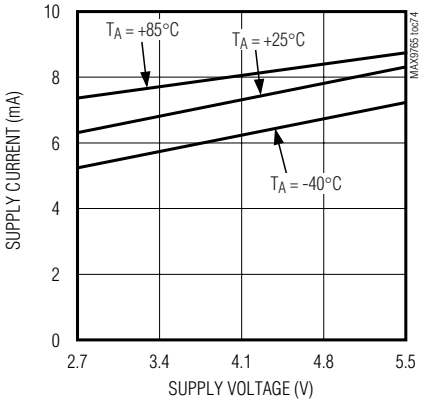


A_V = 10dB
f_{IN} = 1kHz

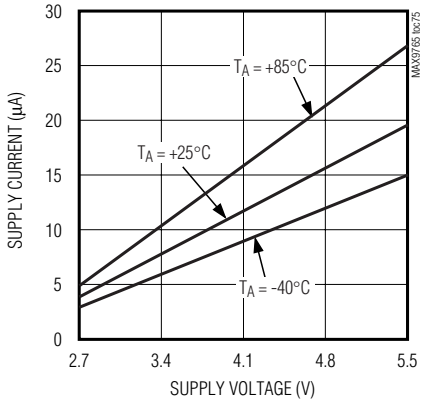
SUPPLY CURRENT vs. SUPPLY VOLTAGE (SPEAKER MODE)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (HEADPHONE MODE)



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



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Pin Description

PIN			NAME	FUNCTION
MAX9765	MAX9766	MAX9767		
1	1	1	$\overline{SHDN}$	Active-Low Shutdown. Connect $\overline{SHDN}$ to V_{DD} for normal operation.
2, 7, 18	2, 7, 18	2, 7, 8, 18, 23, 24, 27, 32	N.C.	No Connection. Not internally connected.
3	3	6	OUTL+	Left-Channel Bridged Amplifier Positive Output. OUTL+ also serves as the left-channel headphone amplifier output.
4, 21	4, 21	4, 21	PV_{DD}	Output Amplifier Power Supply. Connect PV_{DD} to V_{DD}.
5, 20	5, 20	5, 20	PGND	Power Ground. Connect PGND to GND.
6	6	3	OUTL-	Left-Channel Bridged Amplifier Negative Output
8	8	—	INL2	Left-Channel Input 2
9	9	—	INL1	Left-Channel Input 1
10	10	10	MICIN+	Differential Microphone Amplifier Noninverting Input
11	11	11	MICIN-	Differential Microphone Amplifier Inverting Input
12	12	12	AUXIN	Single-Ended Microphone Amplifier Input
13	13	13	V_{DD}	Power Supply
14	14	14	SV_{DD}	Standby Power Supply. Connect to a standby power supply that is always on, or connect to V_{DD} through a Schottky diode and bypass with a 220µF capacitor to GND. Short to V_{DD} if clickless operation is not essential.
15	15	15	MICBIAS	Microphone Bias Output. Bypass MICBIAS with a 1µF capacitor to GND.
16	—	—	MICOUT	Microphone Amplifier Output
17	17	—	GAINR	Right-Channel Gain Set
19	—	19	OUTR-	Right-Channel Bridged Amplifier Negative Output
22	22	22	OUTR+	Right-Channel Bridged Amplifier Positive Output. OUTR+ also serves as the right-channel headphone amplifier output.
23	—	—	ADD	Address Select. A logic high sets the address LSB to 1, a logic low sets the address LSB to 0.
24	24	—	SDA	Bidirectional Serial Data I/O
25	25	—	SCL	Serial Clock Line
26, 29	26, 29	29	GND	Ground
27	27	—	INR2	Right-Channel Input 2
28	28	—	INR1	Right-Channel Input 1
30	30	—	HPS	Headphone Sense Input
31	31	31	BIAS	DC Bias Bypass. See *BIAS Capacitor* section for capacitor selection. Connect C_{BIAS} capacitor from BIAS to GND.
32	32	—	GAINL	Left-Channel Gain Set
—	16	16	MICOUT+	Microphone Amplifier Positive Output

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Pin Description (continued)

PIN			NAME	FUNCTION
MAX9765	MAX9766	MAX9767		
—	19	17	MICOUT-	Microphone Amplifier Negative Output
—	23	—	GAINM	Mono Mode Gain Set
—	—	9	INL	Left-Channel Input
—	—	25	$\overline{INT}$/EXT	Internal (Differential) or External (Single-Ended) Input Select. Drive $\overline{INT}$/EXT low to select internal or high to select external microphone amplifier.
—	—	26	MICGAIN	Microphone Amplifier Gain Set. Tri-State Pin. Connect to V_{DD} for gain = 10dB, float for gain = 20dB, and to GND for gain = 30dB.
—	—	28	INR	Right-Channel Input
—	—	30	MUTE	Mute Input
—	—	—	EP	Exposed Pad. Connect to ground plane of PC board to optimize heatsinking.

Detailed Description

The MAX9765/MAX9766/MAX9767 feature 750mW BTL speaker amplifiers, 65mW headphone amplifiers, input multiplexers, headphone sensing, differential and single-ended input microphone amplifiers, and comprehensive click-and-pop suppression. The MAX9765/MAX9766 are controlled through an I²C-compatible, 2-wire serial interface. The MAX9767 is controlled through three logic inputs: MUTE, $\overline{SHDN}$, $\overline{INT}$ (see the *Selector Guide*). The MAX9765 family features exceptional PSRR (95dB at 1kHz), allowing these devices to operate from noisy digital supplies without the need for a linear regulator.

The speaker amplifiers use a BTL configuration. The MAX9765/MAX9766 main amplifiers are composed of an input amplifier and an output amplifier. Resistor R_{IN} sets the input amplifier's gain, and resistor R_F sets the output amplifier's gain. The output of these two amplifiers serves as the input to a slave amplifier configured as an inverting unity-gain follower. This results in two outputs, identical in magnitude, but 180° out of phase. The overall gain of the speaker amplifiers is twice the product of the two amplifier gains (see the *Gain-Setting Resistor* section). A unique feature of this architecture is that there is no phase inversion from input to output. The MAX9767 does not use a two-stage input amplifier and therefore has phase inversion from input to output.

When configured as a headphone (single-ended) amplifier, the slave amplifier is disabled, muting the speaker and the main amplifier drives the headphone. The MAX9765/MAX9766/MAX9767 can deliver 700mW of continuous average power into a 4Ω load with less than 1% THD+N in speaker mode. The MAX9765/MAX9766 can deliver 70mW of continuous average power into a 16Ω load with less than 1% THD+N in headphone mode. The speaker amplifiers also feature thermal-overload and short-circuit current protection.

All devices feature microphone amplifiers with both differential and single-ended inputs. Differential input is intended for use with internal microphones. Single-ended input is intended for use with external (auxiliary) microphones. The differential input configuration is particularly effective when layout constraints force the microphone amplifier to be physically remote from the ECM microphone and/or the rest of the audio circuitry. The MAX9766/MAX9767 feature a complementary output, creating an ideal interface with CODECs and other devices with differential inputs. All devices also feature an internal microphone bias generator.

Amplifier Common-Mode Bias

These devices feature an internally generated common-mode bias voltage of 1.5V referenced to GND. BIAS provides both click-and-pop suppression and sets the DC bias level for the audio signal. BIAS is internally connected to the noninverting input of each speaker amplifier (see the *Typical Application Circuit*). Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section.

Input Multiplexer

The MAX9765/MAX9766 feature a 2:1 input multiplexer on the front end of each amplifier. The multiplexer is controlled by bit 1 in the control register. A logic low

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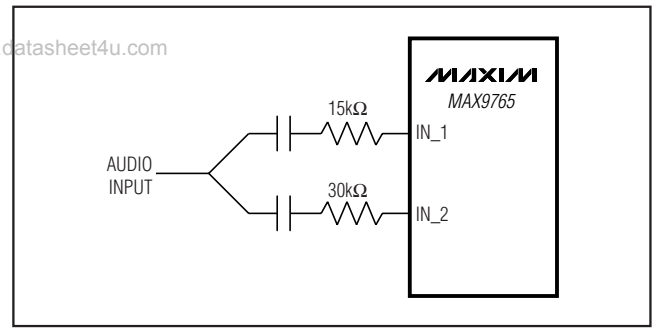

Figure 1. Using the Input Multiplexer for Gain Setting

selects input IN_1 and a logic high selects input IN_2. Both right- and left-channel multiplexers are controlled by the same input.

The input multiplexer can also be used to further expand the number of gain options available from the MAX9765/MAX9766. Connect the audio source to the device through two different input resistors for multiple gain configurations (Figure 1). Additionally, the input multiplexer allows a speaker equalization network to be switched into the speaker signal path. This is typically useful in optimizing acoustic response from speakers with small physical dimensions.

Mono Mode

The mono MAX9766 incorporates a mixer/attenuator (see the *Functional Diagram*). In speaker (mono) mode, the mixer/attenuator combines the two stereo inputs (INL_ and INR_) and attenuates the resultant signal by a factor of 2. This allows for full reproduction of a stereo signal through a single speaker while maintaining optimum headroom. The resistor connected between GAINM and OUTL+ sets the device gain in speaker mode. This allows the speaker amplifier to have a different gain and feedback network from the headphone amplifier.

Headphone Sense Disable Input

The headphone sensing function can be disabled by the HPS_D bit (MAX9765/MAX9766). HPS_D bit determines whether the device is in automatic-detection mode, or fixed-mode operation.

Headphone Sense Input (HPS)

When the MAX9765/MAX9766 are in automatic headphone-detection mode, the state of the headphone sense input (HPS) determines the operating mode of the device. A voltage on HPS less than 0.7 × V_{DD} sets the device to speaker mode. A voltage greater than 0.9 × V_{DD} disables the inverting bridge amplifier (OUT_-), which mutes the speaker amplifier and sets the device into headphone mode.

Connect HPS to the control pin of a 3-wire headphone jack as shown in Figure 2. With no headphone present, the resistive voltage-divider created by R1 and R2 sets the voltage on HPS to 44mV, setting the device to speaker mode. When a headphone plug is inserted into the jack, the control pin is disconnected from the tip contact, and HPS is pulled to V_{DD} through R1, setting the device into headphone mode. Place a resistor in series with the control pin and HPS (R3) to prevent any audio signal from coupling into HPS when the device is in speaker mode.

Shutdown

The MAX9765/MAX9766/MAX9767 feature a 5µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. The drive and microphone amplifiers and the bias circuitry are disabled, the amplifier outputs (OUT_/MIC_) go high impedance, and BIAS and MICBIAS are driven to GND. The digital section of the MAX9765/MAX9766 remains active when the device is shut down through the interface. A logic high on bit 0 of the SHDN register places the MAX9765/MAX9766 in shutdown. A logic low enables the device. A logic low on the $\overline{SHDN}$ input places the devices into shutdown mode, disables the interface, and resets the I^2C registers to a default state. A logic high on $\overline{SHDN}$ enables the device. A logic high on $\overline{SHDN}$ enables the devices.

MUTE

All devices feature a mute mode. When the device is muted, the input is disconnected from the amplifiers. MUTE only affects the power amplifiers, and does not shut down the device. The MAX9765/MAX9766 MUTE mode is selected by writing to the MUTE register (see Command Byte Definitions). The left and right channels can be independently muted. The MAX9767 features an active-high MUTE input that mutes both channels.

$\overline{INT}$/EXT

The MAX9767 microphone amplifier input configuration is controlled by the $\overline{INT}$/EXT input. A logic low In $\overline{INT}$/EXT selects internal (differential) microphone mode. A logic high selects external (single-ended) mode.

Click-and-Pop Suppression

The MAX9765/MAX9766/MAX9767 feature Maxim's patented comprehensive click-and-pop suppression. During startup and shutdown, the common-mode bias voltage of the amplifiers is slowly ramped to and from the DC bias point using an S-shaped waveform. In

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headphone mode, this waveform shapes the frequency spectrum, minimizing the amount of audible components present at the headphone. In speaker mode, the BTL amplifiers start up in the same fashion as in headphone mode. When entering shutdown, both amplifier outputs ramp to GND quickly and simultaneously. The devices can also be connected to a standby power source that ensures that the device undergoes its full shutdown cycle even after power has been removed. The value of the capacitor on the BIAS pin affects the click-and-pop energy. For optimum click/pop performance, use a 1µF capacitor.

Standby Power Supply (SV_{DD})

The MAX9765/MAX9766/MAX9767 feature a patented system that provides clickless power-down when power is removed from the device. SV_{DD} is an **optional** secondary supply that powers the device through its shutdown cycle when V_{DD} is removed. During this cycle, the amplifier output DC level slowly ramps to GND, ensuring clickless power-down. If clickless power-down is required, connect SV_{DD} to either a secondary power supply that is always on, or connect a reservoir capacitor from SV_{DD} to GND. SV_{DD} does not need to be connected to either a secondary power supply or reservoir capacitor for normal device operation. If click-and-pop suppression during power-down is not required, connect SV_{DD} to V_{DD} directly.

The clickless power-down cycle only occurs when the device is in headphone mode. The speaker mode is inherently clickless, the differential architecture cancels the DC shift across the speaker. The MAX9765/MAX9766/MAX9767 BTL outputs are pulled to GND quickly and simultaneously, resulting in no audible components. If the MAX9765/MAX9766/MAX9767 are only used as speaker amplifiers, then reservoir capacitors or secondary supplies are not necessary.

When using a reservoir capacitor, a 220µF capacitor provides optimum charge storage for the shutdown cycle for all conditions. If a smaller reservoir capacitor is desired, decrease the size of C_{BIAS}. A smaller C_{BIAS} causes the output DC level to decay at a faster rate, increasing the audible content at the speaker, but reducing the duration of the shutdown cycle.

Digital Interface

The MAX9765/MAX9766 feature an I^2C/SMBus-compatible 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX9765/MAX9766 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX9765/MAX9766 are transmit/receive

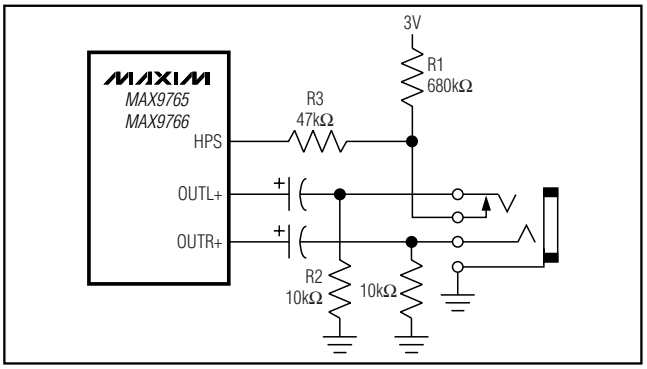

Figure 2. HPS Configuration Circuit

slave-only devices, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL to permit that transfer.

A master device communicates to the MAX9765/MAX9766 by transmitting the proper address followed by a command and/or data words. Each transmit sequence is framed by a START (S) or REPEATED START (S_r) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9765/MAX9766 SDA and SCL amplifiers are open-drain outputs requiring a pullup resistor to generate a logic-high voltage. Series resistors in line with SDA and SCL are optional. These series resistors protect the input stages of the devices from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I^2C bus is not busy.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the MAX9765/MAX9766. The master terminates transmission by issuing the STOP condition; this frees the bus. If a REPEATED START condition is generated instead of a STOP

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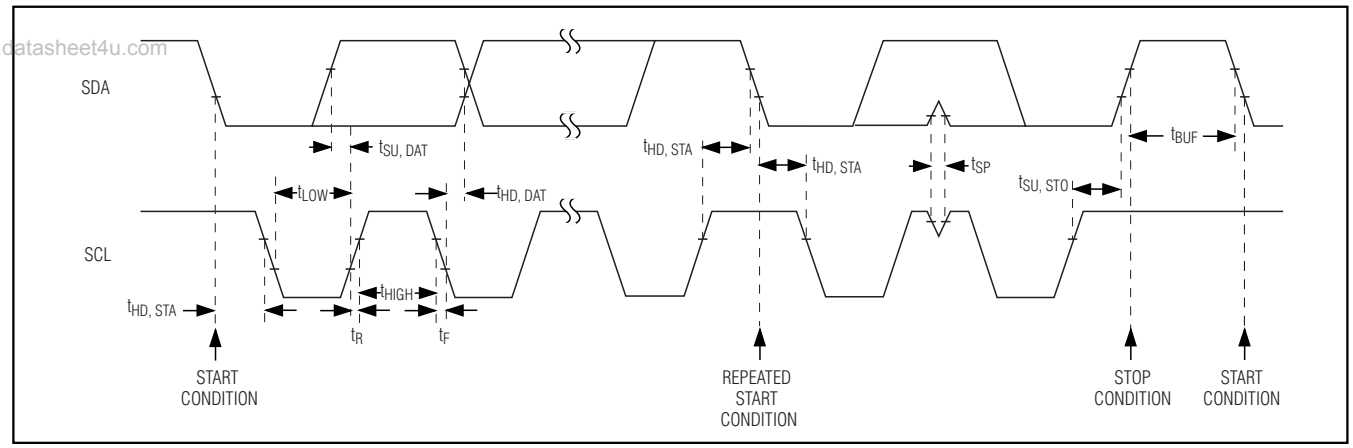

Figure 3. 2-Wire Serial Interface Timing Diagram

condition, the bus remains active. When a STOP condition or incorrect address is detected, the MAX9765/MAX9766 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

Early STOP Conditions

The MAX9765/MAX9766 recognize a STOP condition at any point during the transmission except if a STOP condition occurs in the same high pulse as a START condition (Figure 5). This condition is not a legal I^2C format; at least one clock pulse must separate any START and STOP conditions.

REPEATED START Conditions

A REPEATED START (S_r) condition may indicate a change of data direction on the bus. Such a change occurs when a command word is required to initiate a read operation. S_r may also be used when the bus master is writing to several I^2C devices and does not want to relinquish control of the bus. The MAX9765/MAX9766 serial interface supports continuous write operations with or without an S_r condition separating them. Continuous read operations require S_r conditions because of the change in direction of data flow.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data word. The receiving device always generates ACK. The MAX9765/MAX9766 generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. When transmitting data, the MAX9765/MAX9766 wait for the receiving device to generate an ACK. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

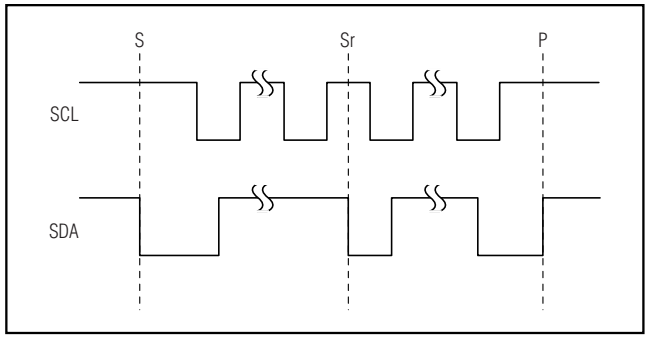

Figure 4. START/STOP Conditions

Slave Address

The bus master initiates communication with a slave device by issuing a START condition followed by a 7-bit slave address (Figure 6). When idle, the MAX9765/MAX9766 wait for a START condition followed by its slave address. The serial interface compares each address value bit-by-bit, allowing the interface to power down immediately if an incorrect address is detected. The LSB of the address word is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit. R/$\overline{\text{W}}$ indicates whether the master is writing to or reading from the MAX9765/MAX9766 (R/$\overline{\text{W}}$ = 0 selects the write condition, R/$\overline{\text{W}}$ = 1 selects the read condition). After receiving the proper address, the MAX9765/MAX9766 issue an ACK by pulling SDA low for one clock cycle.

The MAX9765 has a factory/user-programmed address (Table 2). The MAX9766 has a factory-programmed address: 1001011.

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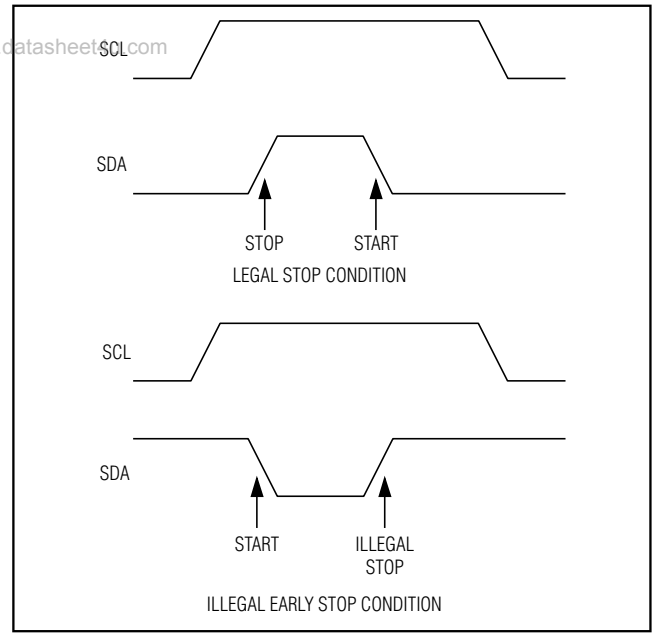

Figure 5. Early STOP Condition

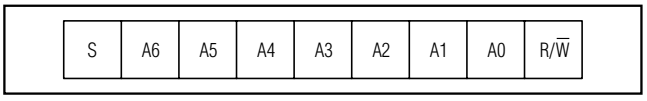

Figure 6. Slave Address Byte Definition

Write Data Format

There are three registers that configure the MAX9765/MAX9766: the MUTE register, SHDN register, and control register. In write data mode (R/$\overline{W}$ = 0), the register address and data byte follow the device address (Figure 7).

MUTE Register

The MUTE register (01hex) is a read/write register that sets the MUTE status of the device. Bit 3 (MUTEL) of the MUTE register controls the left channel, bit 4 (MUTER) controls the right channel. A logic high mutes the respective channel, a logic low brings the channel out of mute.

SHDN Register

The SHDN register (02hex) is a read/write register that controls the power-up state of the device. A logic high in bit 0 of the SHDN register shuts down the device; a logic low turns on the device. A logic high is required in bits 2 to 7 to reset all registers to their default register settings.

Table 1. HPS Setting (MAX9765/MAX9766)

HPS_D BIT	HPS	SPKR/ HP BIT	MODE
0	0	X	BTL
0	1	X	SE
1	X	0	BTL
1	X	1	SE

Table 2. I²C Slave Addresses

ADD CONNECTION	I²C ADDRESS
GND	100 1000
V_{DD}	100 1001
SDA	100 1010
SCL	100 1011

Table 3. MUTE Register Format

REGISTER ADDRESS		0000 0001	
BIT	NAME	VALUE	DESCRIPTION
7	X	Don't Care	—
6	X	Don't Care	—
5	X	Don't Care	—
4	MUTER	0*	Unmute right channel
		1	Mute right channel
3	MUTEL	0*	Unmute left channel
		1	Mute left channel
2	X	Don't Care	—
1	X	Don't Care	—
0	X	Don't Care	—

**Default state.*

Control Register

The control register (03hex) is a read/write register that determines the device configuration. Bit 1 (IN$\overline{1}$/IN2) controls the input multiplexer, a logic high selects input 1, a logic low selects input 2. Bit 2 (HPS_EN) controls the headphone sensing. A logic low configures the device in automatic headphone detection mode. A logic high disables the HPS input. Bit 3 (INT/EXT) controls the microphone amplifier inputs. A logic low selects differential (internal) input mode. A logic high selects single-ended (external) input mode. Bit 4 (SPKR/HP) selects the amplifier operating mode when

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Table 4. SHDN Register Format

REGISTER ADDRESS		0000 0010	
BIT	NAME	VALUE	DESCRIPTION
7	RESET	0*	—
		1	Reset device
6	RESET	0*	—
		1	Reset device
5	RESET	0*	—
		1	Reset device
4	RESET	0*	—
		1	Reset device
3	RESET	0*	—
		1	Reset device
2	RESET	0*	—
		1	Reset device
1	X	Don't Care	—
0	SHDN	0*	Normal operation
		1	Shutdown

**Default state.*

Table 5. Control Register Format

REGISTER ADDRESS		0000 0011	
BIT	NAME	VALUE	DESCRIPTION
7	MG2		Microphone amplifier gain set; 3-bit code sets the gain of the microphone amplifiers (Table 6)
6	MG1		
5	MG0		
4	SPKR/HP	0*	Speaker mode selected
		1	Headphone mode selected
3	$\overline{INT}$/EXT	0*	Differential input selected
		1	Single-ended input selected
2	HPS_D	0*	Automatic headphone detection enabled
		1	Automatic headphone detection disabled (HPS ignored)
1	$\overline{IN1}$/IN2	0*	Input 1 selected
		1	Input 2 selected
0	X	Don't Care	—

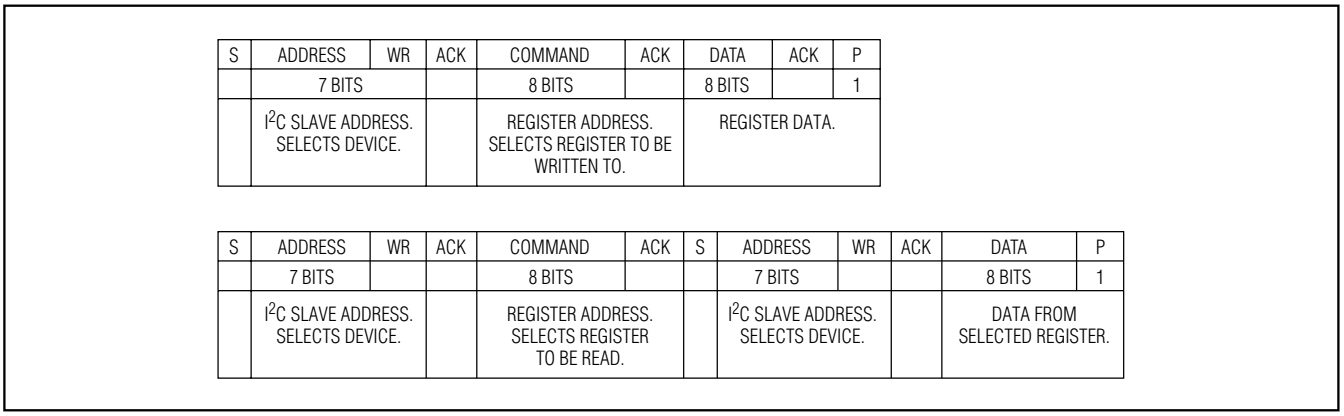

Figure 7. Write/Read Data Format Example

HPS_EN = 1. A logic high selects speaker mode, a logic low selects headphone mode. Bits 5 to 7 (MG0-2) control the gain of the microphone amplifiers (Table 5).

Read Data Format

In read mode (R/$\overline{W}$ = 1), the MAX9765/MAX9766 write the contents of the selected register to the bus. The direction of the data flow reverses following the address acknowledge by the MAX9765/MAX9766. The master device reads the contents of all registers, including the read-only status register. Table 7 shows the status register format. Figure 7 shows an example read data sequence.

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Table 6. Microphone Gain Setting

MG2	MG1	MG0	MAX9765 DIFF GAIN (dB)	MAX9766 DIFF GAIN (dB)	SINGLE-ENDED GAIN (dB)
0*	0*	0*	4	10	10
0	0	1	9	15	15
0	1	0	14	20	20
0	1	1	19	25	25
1	0	0	24	30	29
1	0	1	29	35	34
1	1	0	34	40	36
1	1	1	39	45	40

**Default state.*

I²C Compatibility

The MAX9765/MAX9766 are compatible with existing I²C systems. SCL and SDA are high-impedance inputs; SDA has an open drain that pulls the data line low during the ninth clock pulse. The communication protocol supports the standard I²C 8-bit communications. The general call address is ignored. The MAX9765/MAX9766 addresses are compatible with the 7-bit I²C addressing protocol only. No 10-bit formats are supported.

Applications Information

BTL Amplifiers

The MAX9765/MAX9766/MAX9767 feature speaker amplifiers designed to drive a load differentially, a configuration referred to as bridge-tied load (BTL). The BTL configuration (Figure 8) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. Thus, the devices' differential gain is twice the closed-loop gain of the input amplifier. The effective gain is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into the following equations yields four times the output power due to doubling of the output voltage:

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L}$$

Since the outputs are differential, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large, expensive, consume board space, and degrade low-frequency performance.

Single-Ended Headphone Amplifier

The MAX9765/MAX9766 can be configured as single-ended headphone amplifiers through software or by sensing the presence of a headphone plug (HPS). In headphone mode, the inverting output of the BTL amplifier is disabled, muting the speaker. The gain is 1/2 that of the device in speaker mode, and the output power is reduced by a factor of 4.

In headphone mode, the load must be capacitively coupled to the device, blocking the DC bias voltage from the load (see the *Typical Application Circuit* and the *Output-Coupling Capacitor* section*).*

Microphone Amplifiers

Differential Microphone Amplifier

The MAX9765/MAX9766/MAX9767 feature a low-noise, high CMRR, differential input microphone amplifier. The differential input structure is almost essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as notebooks and PDAs. When properly employed, the differential input architecture offers the following advantages:

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Table 7. Status Register Format

REGISTER ADDRESS		0000 0000	
BIT	**NAME**	**VALUE**	**DESCRIPTION**
7	THRM	0	Device temperature below thermal limit
		1	Device temperature exceeding thermal limit
6	AMPR-	0	OUTR- current below current limit
		1	OUTR- current exceeding current limit
5	AMPR+	0	OUTR+ current below current limit
		1	OUTR+ current exceeding current limit
4	AMPL-	0	OUTL- current below current limit
		1	OUTL- current exceeding current limit
3	AMPL+	0	OUTL+ current below current limit
		1	OUTL+ current exceeding current limit
2	HPSTS	0	Device in speaker mode
		1	Device in headphone mode
1	X	Don't Care	—
0	X	Don't Care	—

- Improved PSRR.
- Higher ground noise immunity.
- Microphone and preamplifier can be placed physically farther apart, easing PC board layout requirements.

Common-Mode Rejection Ratio

Common-mode rejection ratio (CMRR) refers to an amplifier's ability to reject any signal applied equally to both inputs. In the case of amplifying a low-level microphone signal in noisy digital environments, CMRR is a key figure of merit. In audio circuits, CMRR is given by:

$$CMRR(dB) = \frac{A_{DM}}{A_{CM}} = \frac{V_{INDIFF}}{\Delta V_{INCM}}$$

where A_{DM} is the differential gain, A_{CM} is the common-mode gain, ΔV_{INCM} is the change in input common-mode voltage (IN+ and IN- connected together), and V_{INDIFF} is the differential input voltage.

Typical input voltage magnitudes are small enough such that the output is not clipped in either differential or common-mode application. The MAX9765/MAX9766/MAX9767 differential microphone amplifier architecture CMRR actually improves as A_{DM} increases—an additional advantage to the use of differential inputs.

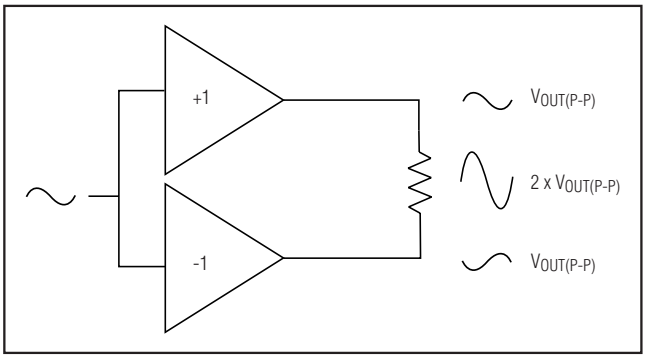

Figure 8. Bridge-Tied Load Configuration

Power Dissipation and Heat Sinking

Under normal operating conditions, the MAX9765/MAX9766/MAX9767 can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{DISSPKG(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings*

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section. For example, θ_{JA} of the QFN package is +42°C/W.

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. The maximum power dissipation for a given V_{DD} and load is given by the following equation:

$$P_{DISS(MAX)} = \frac{2V_{DD}^2}{\pi^2 R_L}$$

If the power dissipation for a given application exceeds the maximum allowed for a given package, either reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking to the device. Large output, supply, and ground PC board traces improve the maximum power dissipation in the package.

Thermal-overload protection limits total power dissipation in these devices. When the junction temperature exceeds +150°C, the thermal-protection circuitry disables the amplifier output stage. The amplifiers are enabled once the junction temperature cools by 8°C. This results in a pulsing output under continuous thermal-overload conditions as the device heats and cools.

Component Selection

Gain-Setting Resistors

External feedback components set the gain of the MAX9765/MAX9766/MAX9767. Resistor R_{IN} sets the gain of the input amplifier (A_{VIN}) and resistor R_F sets the gain of the second-stage amplifier (A_{VOUT}):

$$A_{VIN} = -\left(\frac{15k\Omega}{R_{IN}}\right),\ A_{VOUT} = -\left(\frac{R_F}{15k\Omega}\right)$$

Combining A_{VIN} and A_{VOUT}, R_{IN} and R_F set the single-ended gain of the device as follows:

$$A_V = A_{VIN} \times A_{VOUT} = -\left(\frac{15k\Omega}{R_{IN}}\right) \times -\left(\frac{R_F}{15k\Omega}\right) = +\left(\frac{R_F}{R_{IN}}\right)$$

(MAX9765/MAX9766)

$$A_{VIN} = -\frac{R_F}{R_{IN}} \quad \text{(MAX9767)}$$

As shown, the two-stage amplifier architecture results in a noninverting gain configuration, preserving relative phase through the MAX9765/MAX9766. The gain of the device in BTL mode is twice that of the single-ended mode. Choose R_{IN} between 10kΩ and 15kΩ and R_F between 15kΩ and 100kΩ.

Input Filter

The input capacitor (C_{IN}), in conjunction with R_{IN}, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose R_{IN} according to the *Gain-Setting Resistors* section. Choose the C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in an increased distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system, the actual frequency band of interest, and click-and-pop suppression. Although high-fidelity audio calls for a flat gain response between 20Hz and 20kHz, portable voice-reproduction devices such as cellular phones and two-way radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 150Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

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Output-Coupling Capacitor

The MAX9765/MAX9766/MAX9767 require output-coupling capacitors to operate in single-ended (headphone) mode. The output-coupling capacitor blocks the DC component of the amplifier output, preventing DC current from flowing to the load. The output capacitor and the load impedance form a highpass filter with a -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

As with the input capacitor, choose C_{OUT} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response.

Load impedance is a concern when choosing C_{OUT}. Load impedance can vary, changing the -3dB point of the output filter. A lower impedance increases the corner frequency, degrading low-frequency response. Select C_{OUT} such that the worst-case load/C_{OUT} combination yields an adequate response. Select capacitors with low ESR.

BIAS Capacitor

BIAS is the output of the internally generated 1.5VDC bias voltage. The BIAS bypass capacitor, C_{BIAS}, improves PSRR and THD+N by reducing power supply and other noise sources at the common-mode bias node, and also generates the clickless/popless, start-up/shutdown DC bias waveforms for the speaker amplifiers. Bypass BIAS with a 1µF capacitor to GND. Smaller capacitor values produce faster turn-on/off times and may impact the click/pop levels.

Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Place a 0.1µF ceramic capacitor from V_{DD} to GND. Add additional bulk capacitance as required by the application. Bypass PV_{DD} with a 100µF capacitor to GND. Locate bypass capacitors as close to the device as possible.

Layout and Grounding

Good PC board layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance, as well as route heat away from the device. Good grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital switching noise from coupling into the audio signal. If digital signal lines must cross over or under audio signal lines, ensure that they cross perpendicular to each other.

The MAX9765/MAX9766/MAX9767 thin QFN packages feature exposed thermal pads on their undersides. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the printed circuit board. Connect the pad to signal ground by using a large pad, or multiple vias to the ground plane.

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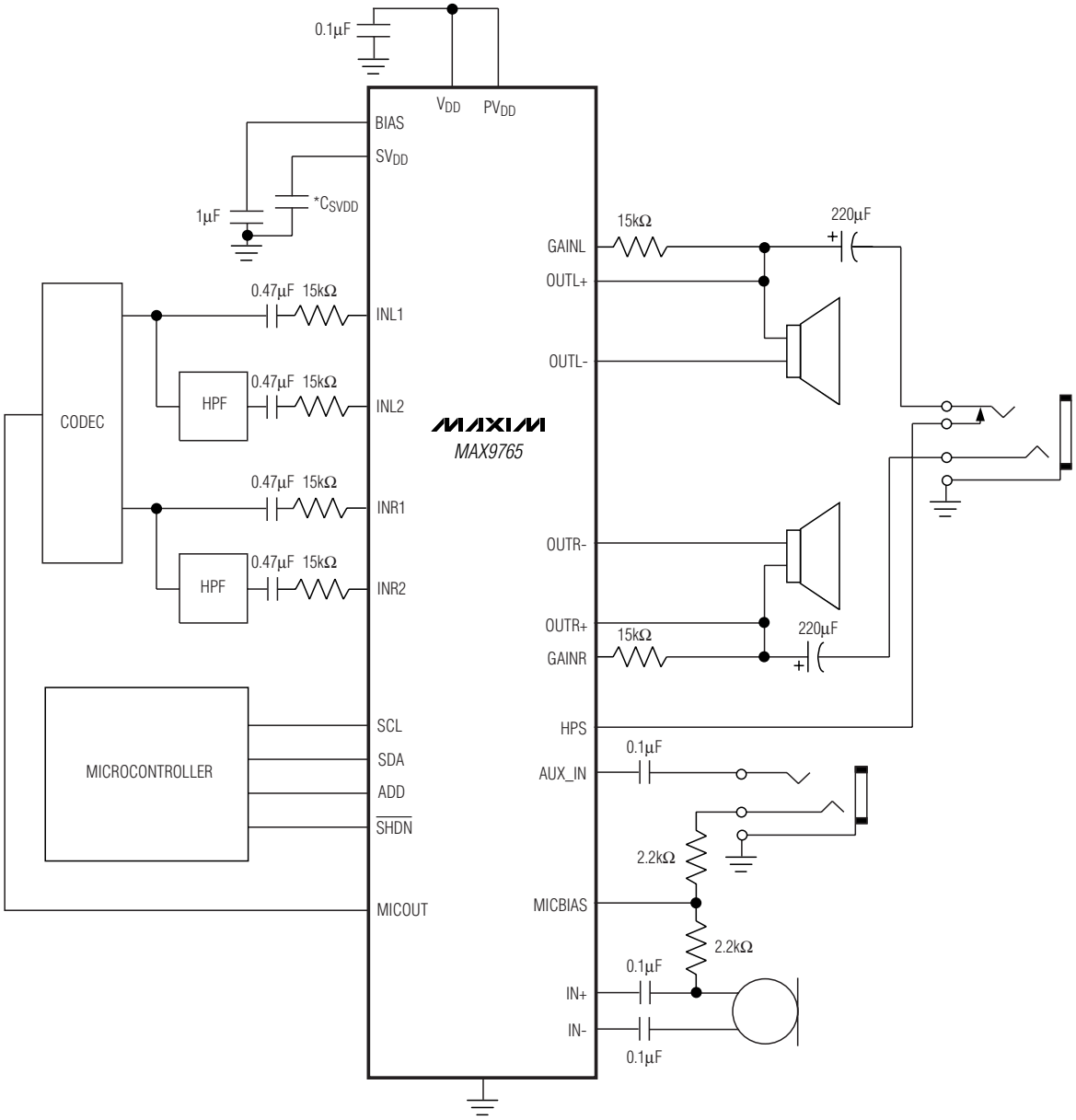
Typical Application Circuit



*C_{SVDD} IS ONLY REQUIRED IF LOW CLICK-AND-POP LEVELS ARE NECESSARY DURING POWER-DOWN.

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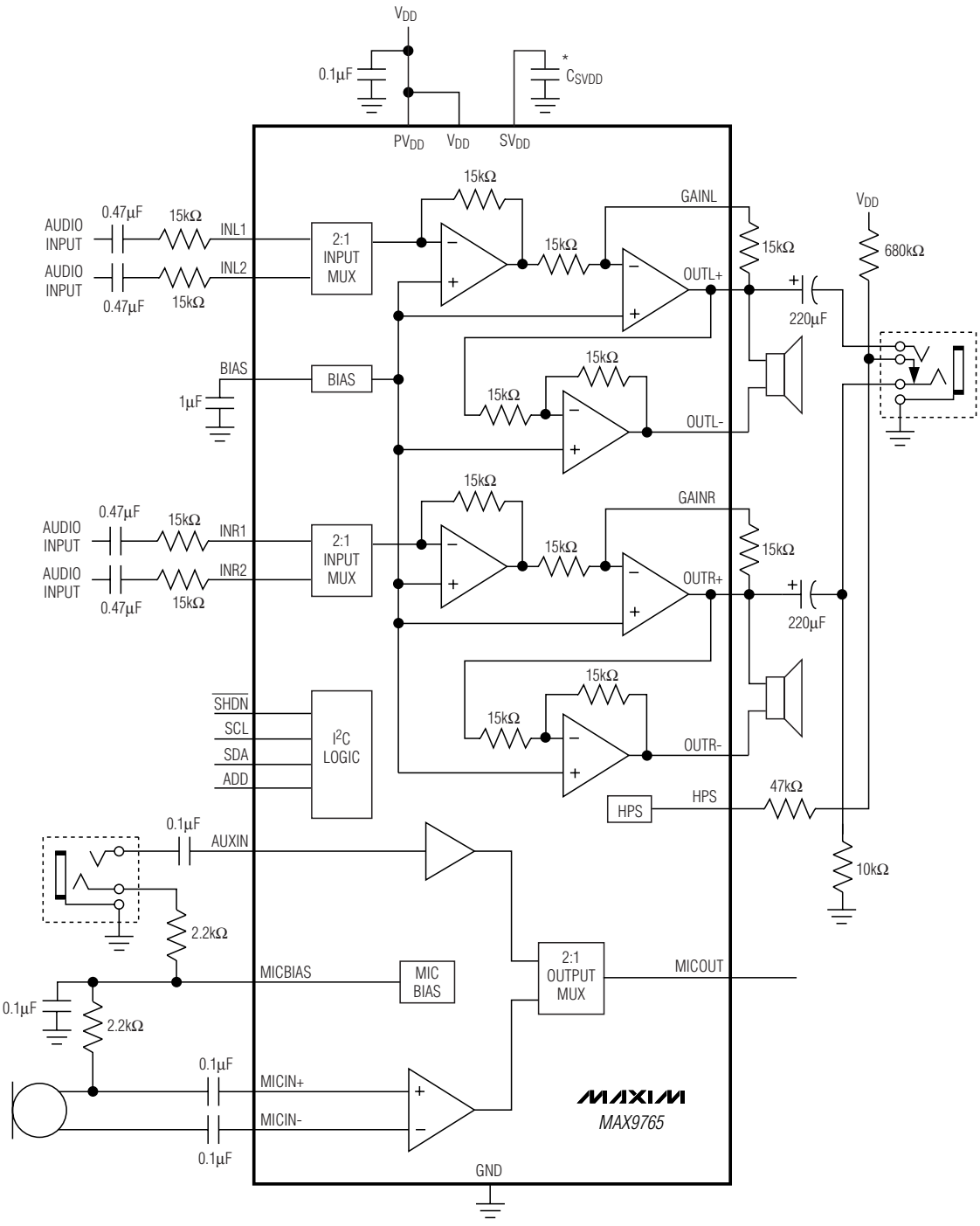
Functional Diagrams



*CSVDD IS ONLY REQUIRED IF LOW CLICK-AND-POP LEVELS ARE NECESSARY DURING POWER-DOWN.

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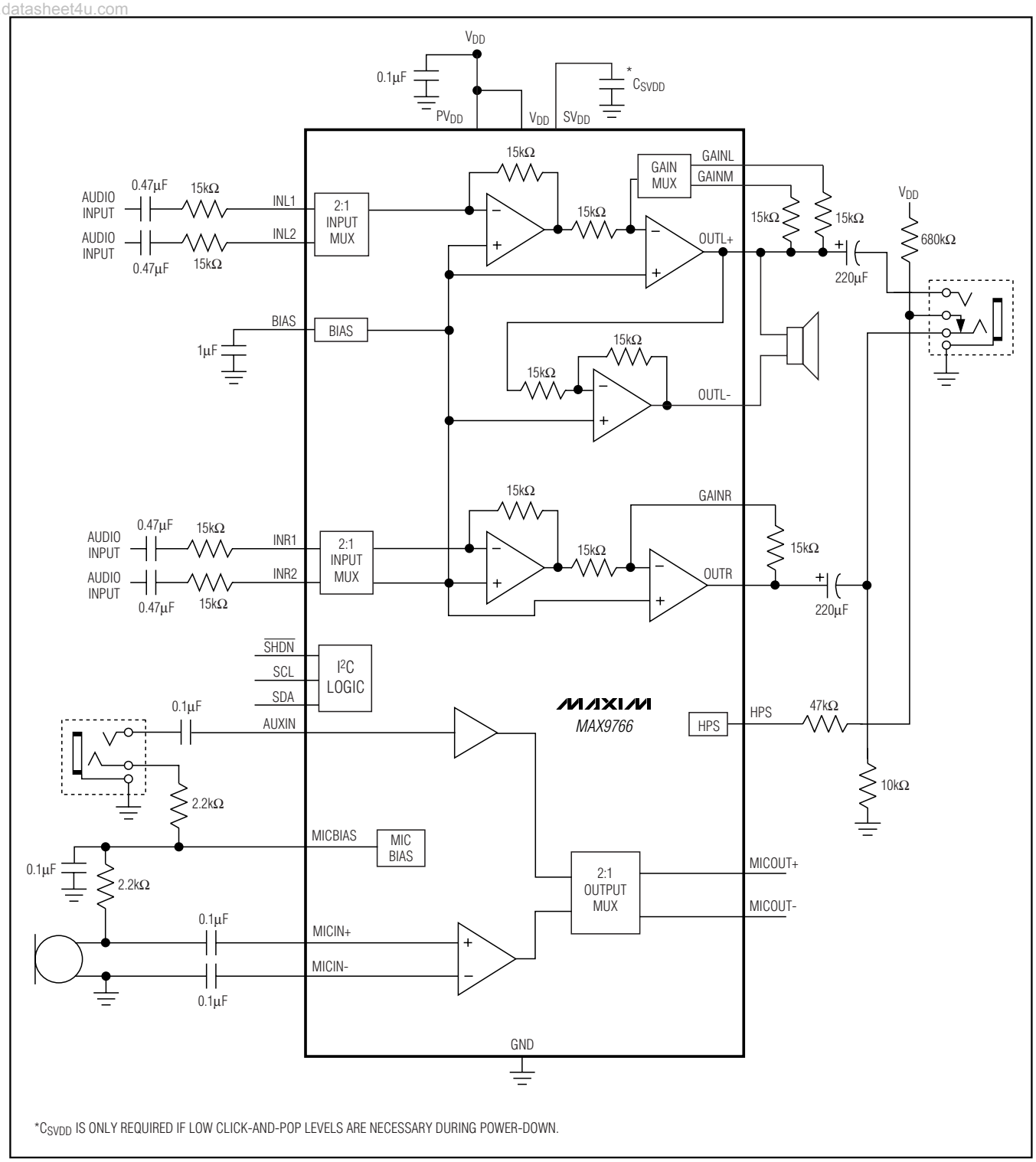
Functional Diagrams (continued)



*C_{SVDD} IS ONLY REQUIRED IF LOW CLICK-AND-POP LEVELS ARE NECESSARY DURING POWER-DOWN.

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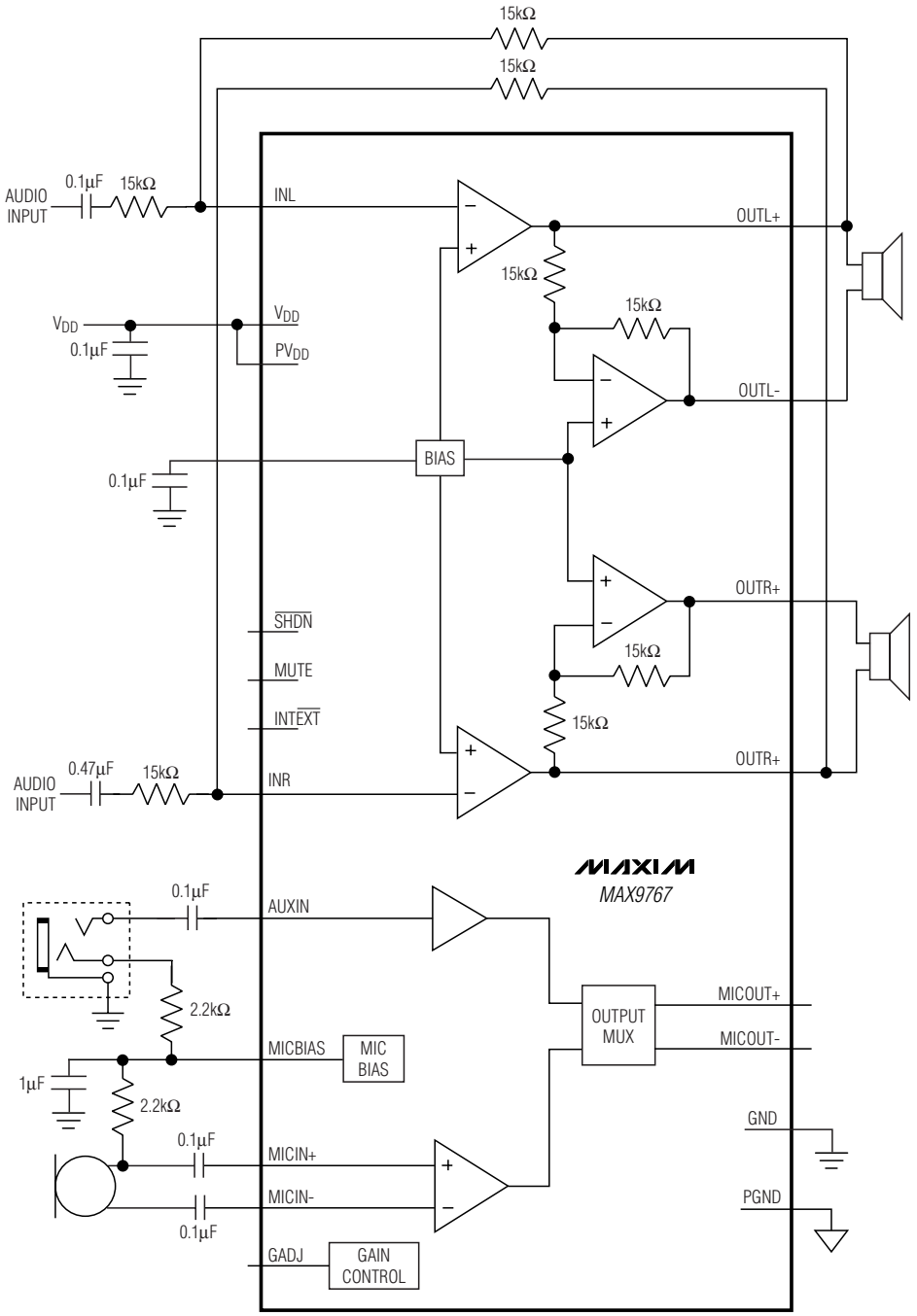
Functional Diagrams (continued)



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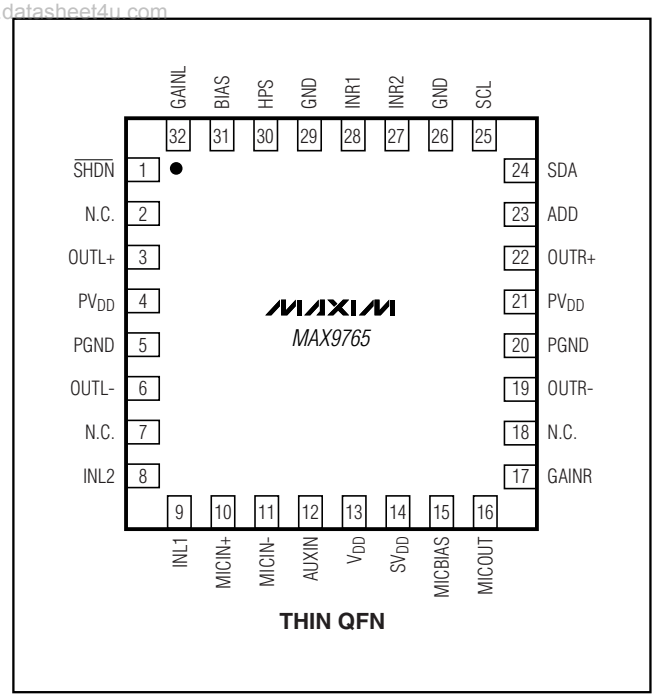
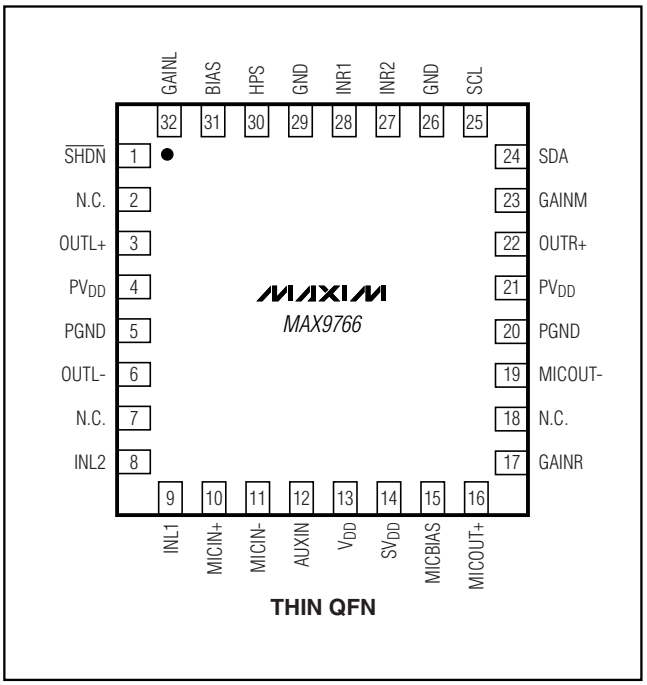
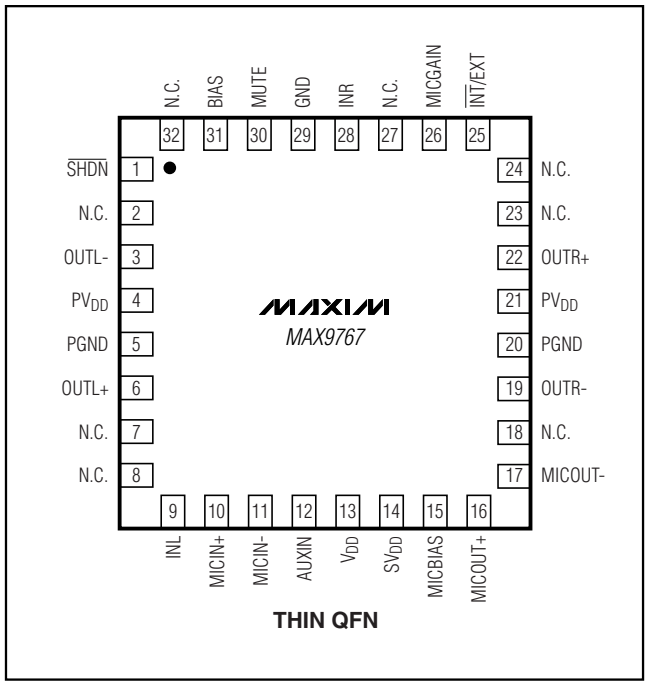
Pin Configurations



THIN QFN



THIN QFN



THIN QFN

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Selector Guide

PART	CONTROL INTERFACE	SPEAKER AMPLIFIER	INPUT MULTIPLEXER	HEADPHONE AMPLIFIER	MICROPHONE AMPLIFIER OUTPUT
MAX9765	I^2C compatible	Stereo	✓	Stereo	Single ended
MAX9766	I^2C compatible	Mono	✓	Stereo	Differential
MAX9767	Parallel	Stereo	—	—	Differential

Chip Information

MAX9765 TRANSISTOR COUNT: 4829
MAX9766 TRANSISTOR COUNT: 4533
MAX9767 TRANSISTOR COUNT: 4731
PROCESS: BiCMOS

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Package Information (continued)

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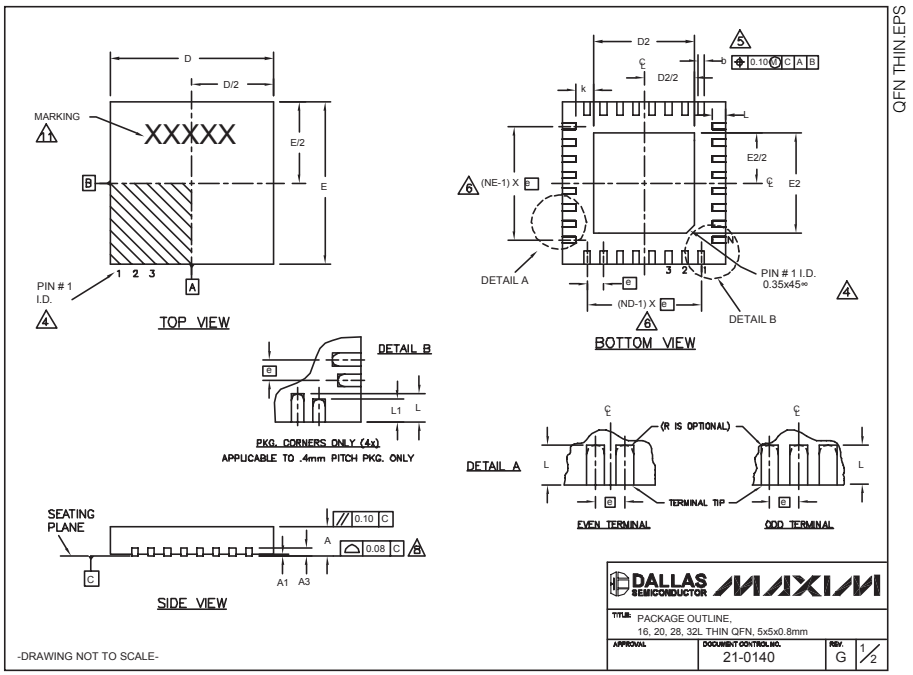
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
L1	-	-	-	-	-	-	-	-	-	-	-	-
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	Y
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	N
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
PACKAGE OUTLINE, 16, 20, 28, 32L THIN QFN, 5x5x0.8mm
21-0140
G
2/2

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