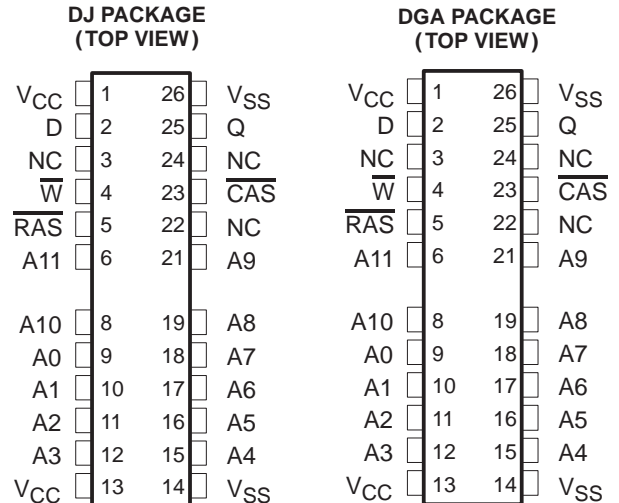


*This data sheet is applicable to all TMS416100/Ps symbolized with Revision "B" and subsequent revisions as described on page 24.*

- **Organization . . . 16 777 216 × 1**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t <sub>RAC</sub> (MAX)	ACCESS TIME t <sub>CAC</sub> (MAX)	ACCESS TIME t <sub>AA</sub> (MAX)	READ OR WRITE CYCLE (MIN)
'416100-60	60 ns	15 ns	30 ns	110 ns
'416100-70	70 ns	18 ns	35 ns	130 ns
'416100-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation for Faster Memory Access**
- **CAS-Before-RAS Refresh**
- **Long Refresh Period**
  - 4096 Cycle Refresh in 64 ms (TMS416100)
  - 256 ms for Extended Refresh Version (TMS416100P)
- **3-State Unlatched Output**
- **Low Power Dissipation (TMS416100P Only)**
  - 500-μA CMOS Standby Current
  - 500-μA Self-Refresh Current
  - 500-μA Extended Refresh Battery Backup Current
- **All Inputs, Outputs and Clocks Are TTL Compatible**
- **Operating Free-Air Temperature Range:**  
0°C to 70°C



PIN NOMENCLATURE	
A0–A11	Address Inputs
CAS	Column-Address Strobe
D	Data In
Q	Data Out
NC	No Internal Connection
RAS	Row-Address Strobe
VCC	5-V Supply
VSS	Ground
W	Write Enable

## description

The TMS416100/P series are high-speed, 16777216-bit dynamic random-access memories, organized as 16777216 words of one bit each. The TMS416100P series feature self refresh and extended refresh. They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

These devices feature maximum  $\overline{\text{RAS}}$  access times of 60 ns, 70 ns, and 80 ns. All inputs, outputs, and clocks are compatible with Series 74 TTL. All addresses and data-in lines are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416100/P are offered in 300-mil 24/26-lead plastic surface-mount SOJ packages (DJ suffix) and 24/26-lead plastic small-outline packages (DGA suffix). All packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

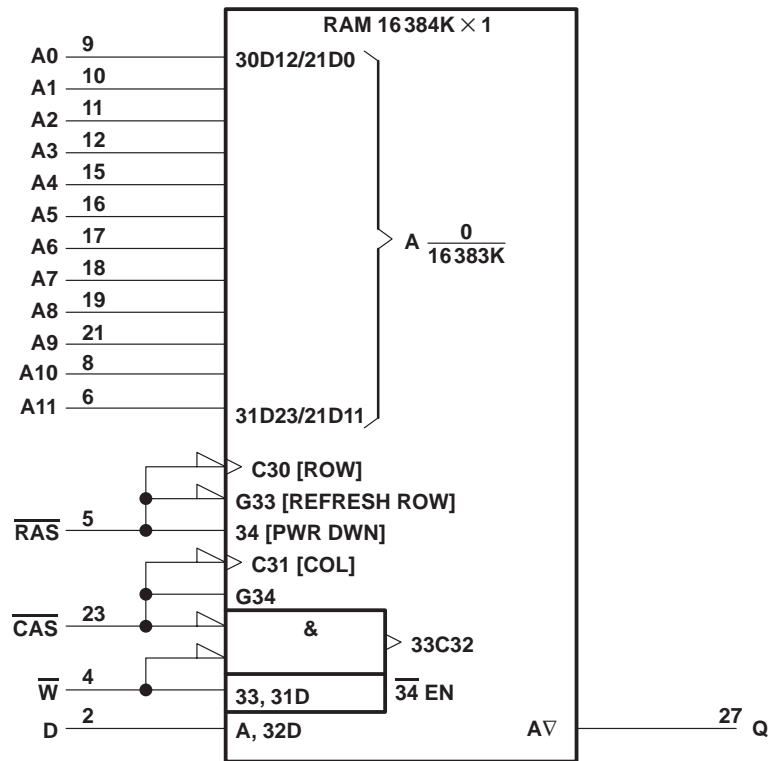


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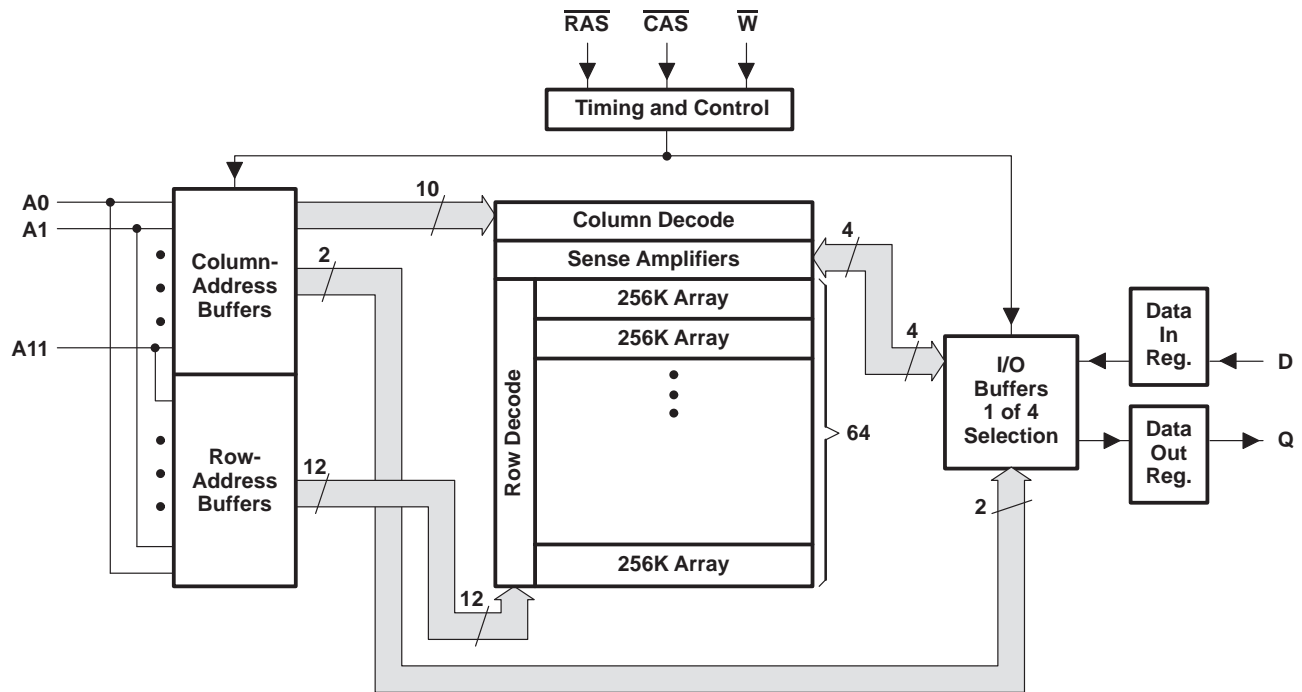
**TMS416100, TMS416100P**  
**16777216-BIT**  
**DYNAMIC RANDOM-ACCESS MEMORIES**  
 SMKS611 – FEBRUARY 1994

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
 Pin numbers shown are for the DJ and DGA packages.

## functional block diagram



## operation

### enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that can be accessed is determined by  $t_{RAS}$ , the maximum  $\overline{RAS}$ -low time.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of  $\overline{RAS}$ . The buffers act as transparent or flow-through latches while  $\overline{CAS}$  is high. The falling edge of  $\overline{CAS}$  latches the addresses and enables the output. This feature allows the TMS416100/P to operate at a higher data bandwidth than conventional page-mode parts because retrieval begins as soon as the column address is valid rather than when  $\overline{CAS}$  transitions low. This performance improvement is referred to as *enhanced page mode*. Valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of  $\overline{CAS}$ . In this case, data is obtained after  $t_{CAC}$  max (access time from  $\overline{CAS}$  low), if  $t_{AA}$  max (access time from column address) and  $t_{RAC}$  have been satisfied. In the event that the column address for the next cycle is valid at the time  $\overline{CAS}$  goes high, access time for the next cycle is determined by the later occurrence of  $t_{CPA}$  or  $t_{CAC}$ .

### address (A0–A11)

Twenty-four address bits are required to decode 1 of 16777216 storage cell locations. Twelve row-address bits are set up on inputs A0 through A11 and latched during a normal access and during  $\overline{RAS}$ -only refresh as the device requires 4096 refresh cycles. Twelve column-address bits are set up on inputs A0–A11 and latched onto the chip by  $\overline{CAS}$ . All addresses must be stable on or before the falling edges of  $\overline{RAS}$  and  $\overline{CAS}$ .  $\overline{RAS}$  is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder.  $\overline{CAS}$  is used as a chip select, activating the output buffer as well as latching the address bits into the column-address buffer.

### **write enable ( $\overline{W}$ )**

The read or write mode is selected through the write-enable ( $\overline{W}$ ) input. A logic high on the  $\overline{W}$  input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When  $\overline{W}$  goes low prior to  $\overline{CAS}$  (early write), data out remains in the high-impedance state for the entire cycle, permitting common I/O operation.

### **data in (D)**

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of  $\overline{CAS}$  or  $\overline{W}$  strobes data into the on-chip data latch. In an early-write cycle,  $\overline{W}$  is brought low prior to  $\overline{CAS}$  and the data is strobed in by  $\overline{CAS}$  with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle,  $\overline{CAS}$  is already low and the data is strobed in by  $\overline{W}$  with setup and hold times referenced to this signal.

### **data out (Q)**

The 3-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. The output is in the high-impedance (floating) state until  $\overline{CAS}$  is brought low. In a read cycle, the output becomes valid at the latest occurrence of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$ , or  $t_{CPA}$  and remains valid while  $\overline{CAS}$  is low.  $\overline{CAS}$  going high returns it to the high-impedance state.

### **refresh**

A refresh operation must be performed at least once every 64 ms to retain data. This can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A  $\overline{RAS}$ -only operation can be used by holding  $\overline{CAS}$  at the high (inactive) level, conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a  $\overline{RAS}$ -only refresh. Hidden refresh can be performed by holding  $\overline{CAS}$  at  $V_{IL}$  after a read operation and cycling  $\overline{RAS}$  after a specified precharge period, similar to a  $\overline{RAS}$ -only refresh cycle except with  $\overline{CAS}$  held low. Valid data is maintained at the output throughout the hidden refresh cycle. An internal address provides the refresh address during hidden refresh.

### **$\overline{CAS}$ -before- $\overline{RAS}$ refresh**

$\overline{CAS}$ -before- $\overline{RAS}$  (CBR) refresh is utilized by bringing  $\overline{CAS}$  low earlier than  $\overline{RAS}$  (see parameter  $t_{CSR}$ ) and holding it low after  $\overline{RAS}$  falls (see parameter  $t_{CHR}$ ). For successive  $\overline{CAS}$ -before- $\overline{RAS}$  refresh cycles,  $\overline{CAS}$  remains low while cycling  $\overline{RAS}$ . For this mode of refresh, the external addresses are ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500  $\mu A$  refresh current is available on the TMS416100P. Data integrity is maintained using  $\overline{CAS}$ -before- $\overline{RAS}$  refresh with a period of 62.5  $\mu s$  while holding  $\overline{RAS}$  low for less than 1  $\mu s$ . To minimize current consumption, all input levels need to be at CMOS levels ( $V_{IL} \leq 0.2 V$ ,  $V_{IH} \leq V_{CC} - 0.2 V$ ).

### **power up**

To achieve proper device operation, an initial pause of 200  $\mu s$  followed by a minimum of eight initialization cycles is required after full  $V_{CC}$  level is achieved. These eight initialization cycles need to include at least one refresh ( $\overline{RAS}$ -only or  $\overline{CAS}$ -before- $\overline{RAS}$ ) cycle.

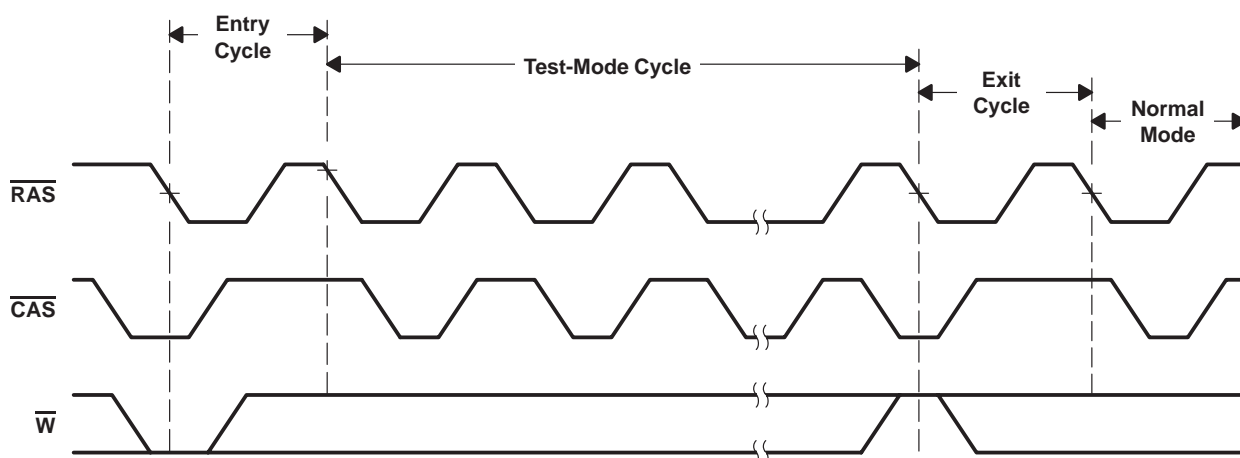
### self refresh (TMS416100P)

The self-refresh mode is entered by dropping  $\overline{\text{CAS}}$  low prior to  $\overline{\text{RAS}}$  going low.  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  are both held low for a minimum of 100  $\mu\text{s}$ . The chip is then refreshed by an on-board oscillator. No external address is required because the CBR counter is used to keep track of the address. To exit the self-refresh mode, both  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  are brought high to satisfy  $t_{\text{CHS}}$ . Upon exiting the self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. This ensures the DRAM is fully refreshed.

### test mode

The test mode is initiated with a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle while simultaneously holding the  $\overline{\text{W}}$  input low (WCBR). The entry cycle performs an internal refresh cycle while internally setting the device to perform parallel read or write on subsequent cycles. While in the test mode, any data sequence can be performed. The device exits the test mode if a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  (CBR) refresh cycle with  $\overline{\text{W}}$  held high or a  $\overline{\text{RAS}}$ -only refresh (ROR) cycle is performed.

The device is configured as 1024K  $\times$  16 bits with a 16-bit parallel read-and-write data path in the test mode. Column addresses A0, A1, A10, and A11 are not used. During a read cycle, all 16 bits of the internal data bus are compared. If all bits are in the same data state, the output pin goes high. If one or more bits disagree, the output pin goes low. Test time is reduced by a factor of 16, compared to normal memory mode.



NOTE: The states of  $\overline{\text{W}}$ , data input, and address are defined by the type of cycle used during test mode.

**Figure 1. Test-Mode Cycle**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	– 1 V to 7 V
Input voltage range (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range	– 55°C to 125°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to  $V_{SS}$ .

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	2.4		6.5	V
$V_{IL}$ Low-level input voltage (see Note 2)	–1		0.8	V
$T_A$ Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	'416100-60 '416100P-60		'416100-70 '416100P-70		'416100-80 '416100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = – 5 mA		2.4		2.4		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4.2 mA		0.4		0.4		V
I <sub>I</sub>	Input current (leakage)†	V <sub>I</sub> = 0 V to 6.5 V All other pins = 0 V to V <sub>CC</sub>		± 10		± 10		μA
I <sub>O</sub>	Output current (leakage)†	V <sub>O</sub> = 0 V to V <sub>CC</sub> , $\overline{\text{CAS}}$ high		± 10		± 10		μA
I <sub>CC1</sub>	Read- or write-cycle current (see Notes 3 and 5)	V <sub>CC</sub> = 5.5 V, Minimum cycle		80		70		mA
I <sub>CC2</sub>	Standby current	After 1 memory cycle, RAS and CAS high, V <sub>IH</sub> = 2.4 V (TTL)		2		2		mA
		After 1 memory cycle, RAS and CAS high, V <sub>IH</sub> = V <sub>CC</sub> – 0.2 V (CMOS)	'416100	1		1		mA
			'416100P	500		500		μA
I <sub>CC3</sub>	Average refresh current (RAS-only or CBR) (see Notes 3 and 5)†	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ( $\overline{\text{RAS}}$ -only); RAS low after CAS low (CBR)		80		70		mA
I <sub>CC4</sub>	Average page current (see Notes 4 and 5)†	RAS low, $\overline{\text{CAS}}$ cycling		70		60		mA
I <sub>CC6</sub>	Self-refresh current (‘416100P only)	$\overline{\text{CAS}}$ and $\overline{\text{RAS}}$ < 0.2 V, Measured after t <sub>RASS</sub> min		500		500		μA
I <sub>CC7</sub>	Standby current, output enable (see Note 5)†	RAS = V <sub>IH</sub> , $\overline{\text{CAS}}$ = V <sub>IL</sub> , Data out = enabled		5		5		mA
I <sub>CC10</sub>	Extended-refresh battery backup (‘416100P only)	t <sub>RC</sub> = 62.5 μs, t <sub>RAS</sub> ≤ 1 μs, V <sub>CC</sub> – 0.2 V ≤ V <sub>IH</sub> ≤ 6.5 V, 0 V ≤ V <sub>IL</sub> ≤ 0.2 V, W and $\overline{\text{OE}}$ = V <sub>IH</sub> , Address and data stable		500		500		μA

† Minimum cycle, V<sub>CC</sub> = 5.5 V

- NOTES: 3. Measured with a maximum of one address change while  $\overline{\text{RAS}}$  = V<sub>IL</sub>  
4. Measured with a maximum of one address change while CAS = V<sub>IH</sub>  
5. Measured with no load connected

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**capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)**

PARAMETER		MIN	MAX	UNIT
C <sub>i(A)</sub>	Input capacitance, address inputs		5	pF
C <sub>i(D)</sub>	Input capacitance, data inputs		5	pF
C <sub>i(RC)</sub>	Input capacitance, strobe inputs		7	pF
C <sub>i(W)</sub>	Input capacitance, write-enable input		7	pF
C <sub>o</sub>	Output capacitance		7	pF

NOTE 6: V<sub>CC</sub> = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature**

PARAMETER		'416100-60 '416100P-60		'416100-70 '416100P-70		'416100-80 '416100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AA</sub>	Access time from column address		30		35		40	ns
t <sub>CAC</sub>	Access time from $\overline{\text{CAS}}$ low		15		18		20	ns
t <sub>CPA</sub>	Access time from column precharge		35		40		45	ns
t <sub>RAC</sub>	Access time from $\overline{\text{RAS}}$ low		60		70		80	ns
t <sub>CLZ</sub>	$\overline{\text{CAS}}$ to output in low-impedance state	0		0		0		ns
t <sub>OH</sub>	Output disable time, start of $\overline{\text{CAS}}$ high	3		3		3		ns
t <sub>OFF</sub>	Output disable time after $\overline{\text{CAS}}$ high (see Note 7)	0	15	0	18	0	20	ns

NOTE 7: t<sub>OFF</sub> is specified when the output is no longer driven.





**timing requirements over recommended ranges of supply voltage and operating free-air temperature**

		'416100-60 '416100P-60		'416100-70 '416100P-70		'416100-80 '416100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Cycle time, random read or write (see Note 8)	110		130		150		ns
t <sub>RWC</sub>	Cycle time, read-write (see Note 8)	130		153		175		ns
t <sub>PC</sub>	Cycle time, page-mode read or write (see Notes 8 and 9)	40		45		50		ns
t <sub>PRWC</sub>	Cycle time, page-mode read-write (see Note 8)	60		68		75		ns
t <sub>RASP</sub>	Pulse duration, page-mode, $\overline{\text{RAS}}$ low (see Note 10)	60	100 000	70	100 000	80	100 000	ns
t <sub>RAS</sub>	Pulse duration, nonpage-mode, $\overline{\text{RAS}}$ low (see Note 10)	60	10 000	70	10 000	80	10 000	ns
t <sub>CAS</sub>	Pulse duration, $\overline{\text{CAS}}$ low (see Note 11)	15	10 000	18	10 000	20	10 000	ns
t <sub>CP</sub>	Pulse duration, $\overline{\text{CAS}}$ high	10		10		10		ns
t <sub>RP</sub>	Pulse duration, $\overline{\text{RAS}}$ high (precharge)	40		50		60		ns
t <sub>WP</sub>	Pulse duration, $\overline{\text{W}}$ low	10		10		10		ns
t <sub>ASC</sub>	Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>ASR</sub>	Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t <sub>DS</sub>	Setup time, data (see Note 12)	0		0		0		ns
t <sub>RCS</sub>	Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t <sub>CWL</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	15		18		20		ns
t <sub>RWL</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	15		18		20		ns
t <sub>WCS</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low (early-write operation only)	0		0		0		ns
t <sub>WRP</sub>	Setup time, $\overline{\text{W}}$ high before $\overline{\text{RAS}}$ low (CAS-before-RAS refresh only)	10		10		10		ns
t <sub>WTS</sub>	Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ low (test mode only)	10		10		10		ns
t <sub>CAH</sub>	Hold time, column address after $\overline{\text{CAS}}$ low	10		15		15		ns
t <sub>DH</sub>	Hold time, data (see Note 12)	10		15		15		ns
t <sub>RAH</sub>	Hold time, row address after $\overline{\text{RAS}}$ low	10		10		10		ns
t <sub>RCH</sub>	Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 13)	0		0		0		ns
t <sub>RRH</sub>	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 13)	0		0		0		ns
t <sub>WCH</sub>	Hold time, $\overline{\text{W}}$ low after $\overline{\text{CAS}}$ low (early-write operation only)	10		15		15		ns
t <sub>WRH</sub>	Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ low (CAS-before-RAS refresh only)	10		10		10		ns
t <sub>WTH</sub>	Hold time, $\overline{\text{W}}$ low after $\overline{\text{RAS}}$ low (test mode only)	10		10		10		ns
t <sub>RHCP</sub>	Hold time, $\overline{\text{RAS}}$ high from $\overline{\text{CAS}}$ precharge	35		40		45		ns
t <sub>CHS</sub>	Hold time, $\overline{\text{CAS}}$ low after $\overline{\text{RAS}}$ high (self refresh)	– 50		– 50		– 50		ns

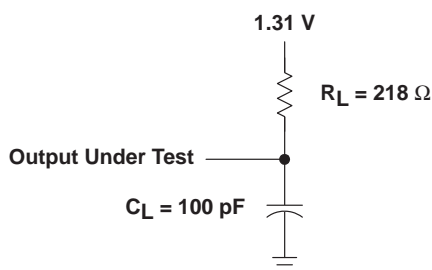
- NOTES: 8. All cycle times assume t<sub>T</sub> = 5 ns.  
9. To assure t<sub>PC</sub> min, t<sub>ASC</sub> should be greater than or equal to t<sub>CP</sub>.  
10. In a read-write cycle, t<sub>RWD</sub> and t<sub>RWL</sub> must be observed.  
11. In a read-write cycle, t<sub>CWD</sub> and t<sub>CWL</sub> must be observed.  
12. Referenced to the later of  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$  in write operations  
13. Either t<sub>RRH</sub> or t<sub>RCH</sub> must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

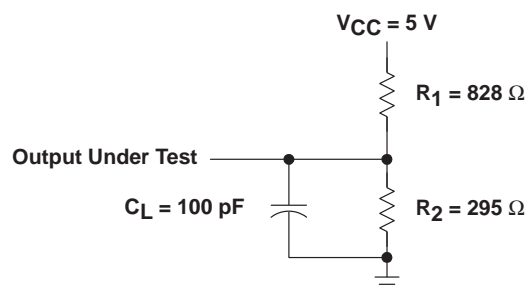
		'416100-60 '416100P-60		'416100-70 '416100P-70		'416100-80 '416100P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>AWD</sub>	Delay time, column address to $\overline{W}$ low (read-write operation only)	30		35		40		ns
t <sub>CHR</sub>	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ( $\overline{CAS}$ -before- $\overline{RAS}$ refresh only)	10		10		10		ns
t <sub>CRP</sub>	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t <sub>CSH</sub>	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t <sub>CSR</sub>	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ( $\overline{CAS}$ -before- $\overline{RAS}$ refresh only)	5		5		5		ns
t <sub>CWD</sub>	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-write operation only)	15		18		20		ns
t <sub>RAD</sub>	Delay time, $\overline{RAS}$ low to column address (see Note 14)	15	30	15	35	15	40	ns
t <sub>RAL</sub>	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t <sub>CAL</sub>	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t <sub>RCD</sub>	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	20	45	20	52	20	60	ns
t <sub>RPC</sub>	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t <sub>RSR</sub>	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t <sub>RWD</sub>	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-write operation only)	60		70		80		ns
t <sub>CPW</sub>	Delay time, $\overline{W}$ low after $\overline{CAS}$ precharge (read-write operation only)	35		40		45		ns
t <sub>RASS</sub>	Pulse duration, self-refresh entry from $\overline{RAS}$ low	100		100		100		μs
t <sub>RPS</sub>	Pulse duration, $\overline{RAS}$ precharge after self refresh	110		130		150		ns
t <sub>TAA</sub>	Access time from address (test mode)	35		40		45		ns
t <sub>TCPA</sub>	Access time from column precharge (test mode)	40		45		50		ns
t <sub>TRAC</sub>	Access time from $\overline{RAS}$ (test mode)	65		75		85		ns
t <sub>REF</sub>	Refresh time interval	'416100		64		64		ms
		'416100P		256		256		ms
t <sub>T</sub>	Transition time	3	30	3	30	3	30	ns

NOTE 14: The maximum value is specified only to assure access time.

## PARAMETER MEASUREMENT INFORMATION



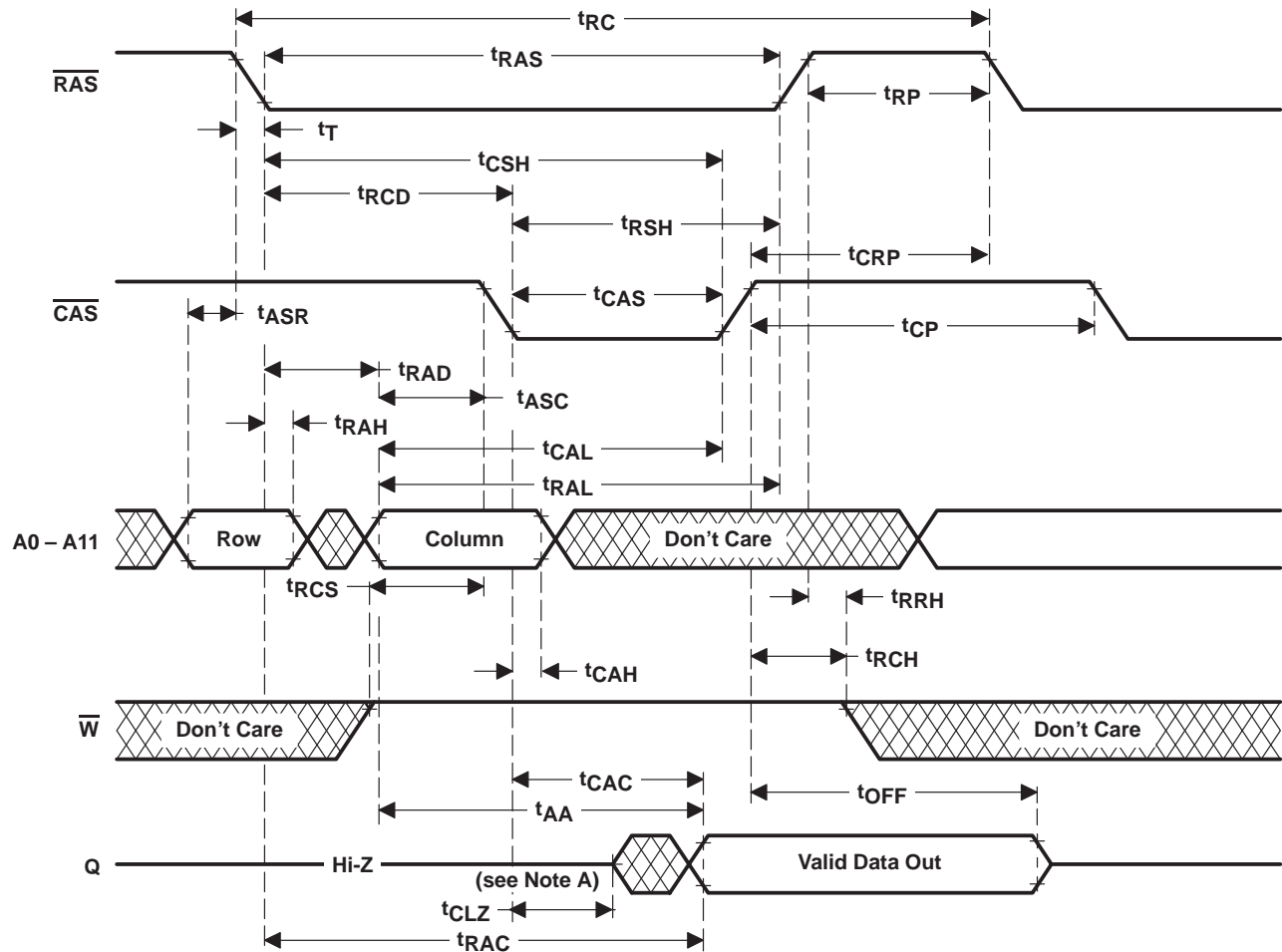
(a) LOAD CIRCUIT



(b) ALTERNATE LOAD CIRCUIT

Figure 2. Load Circuits

# PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from 3-state to an invalid data state prior to the specified access time.

Figure 3. Read-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

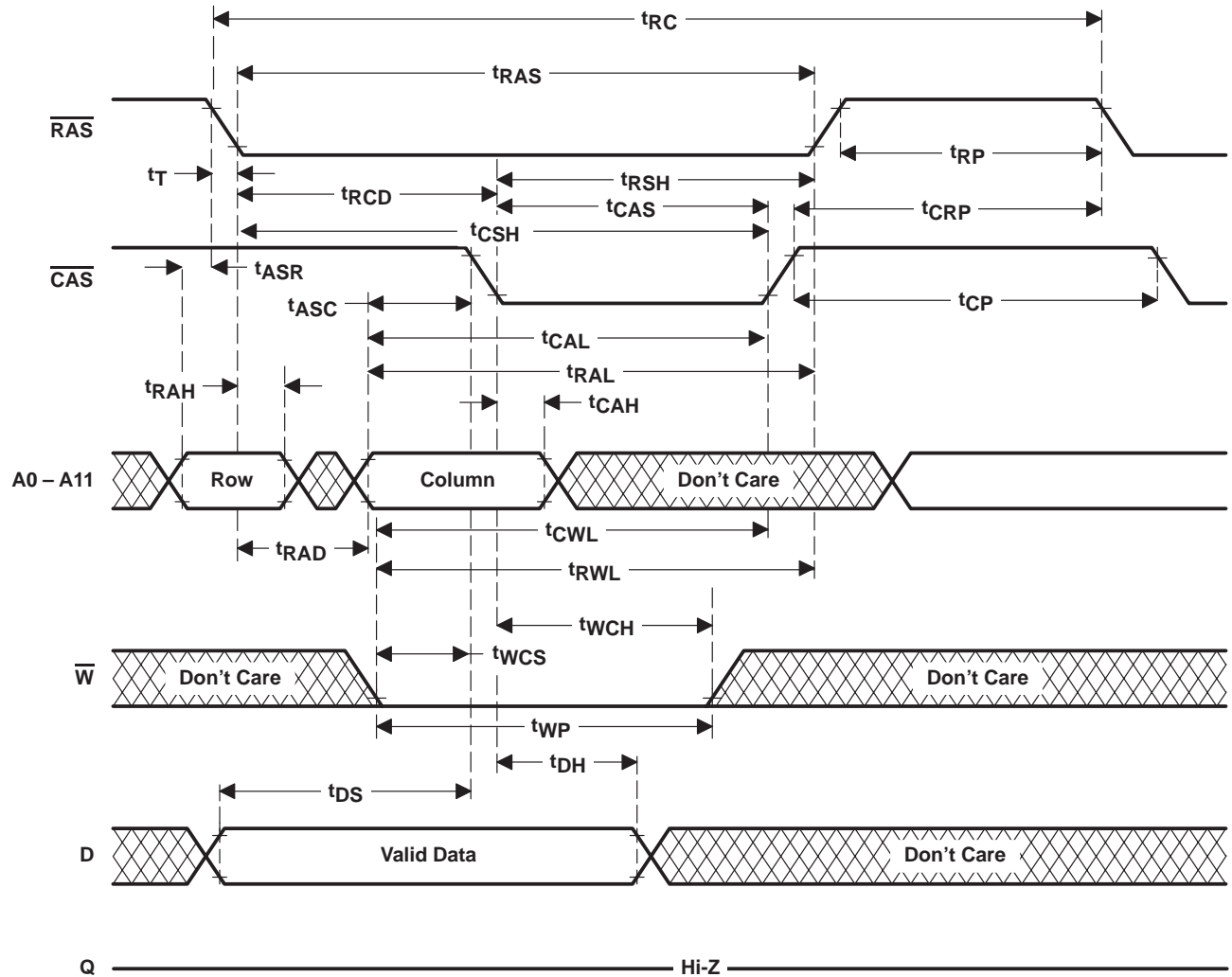


Figure 4. Early-Write-Cycle Timing

# PARAMETER MEASUREMENT INFORMATION

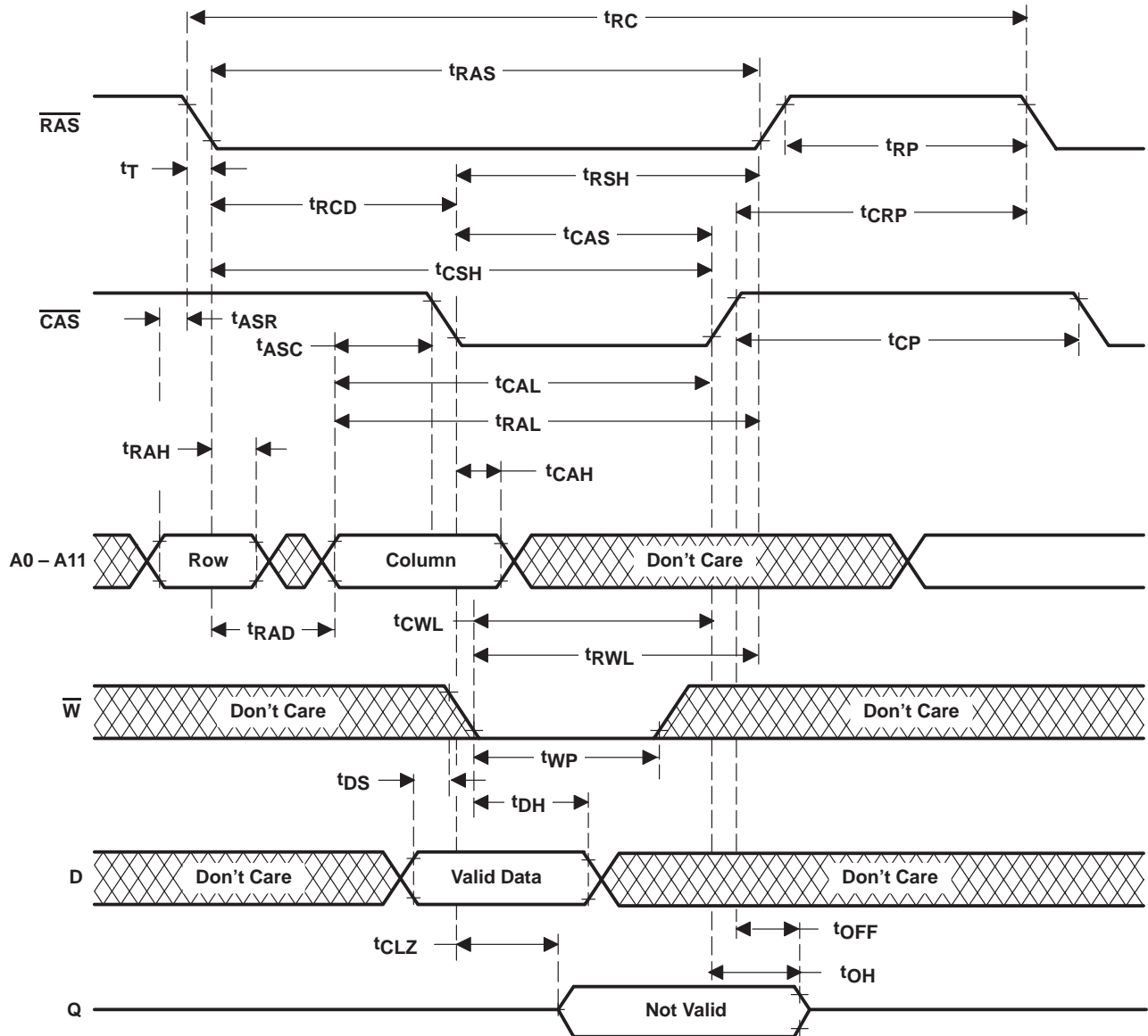
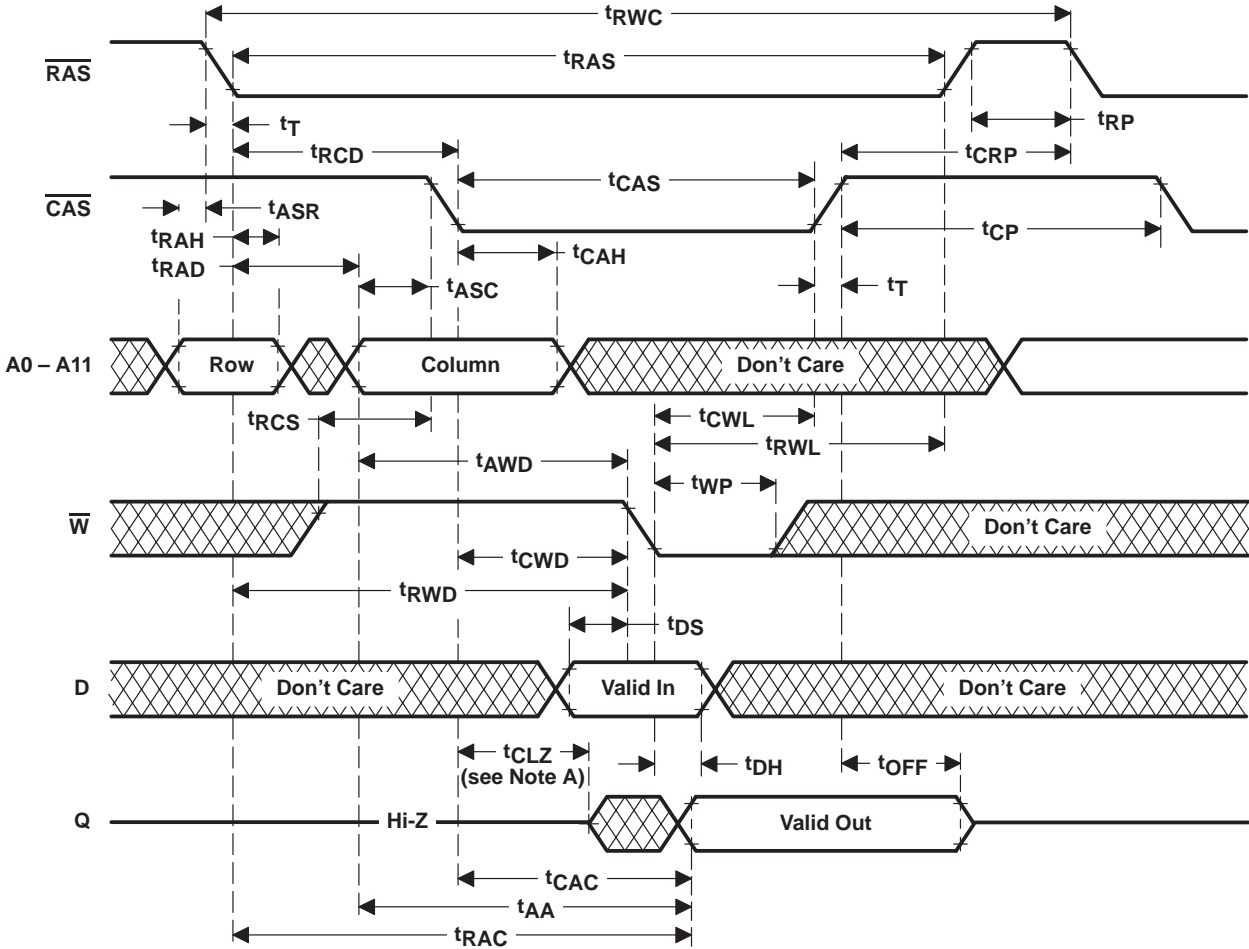


Figure 5. Write-Cycle Timing

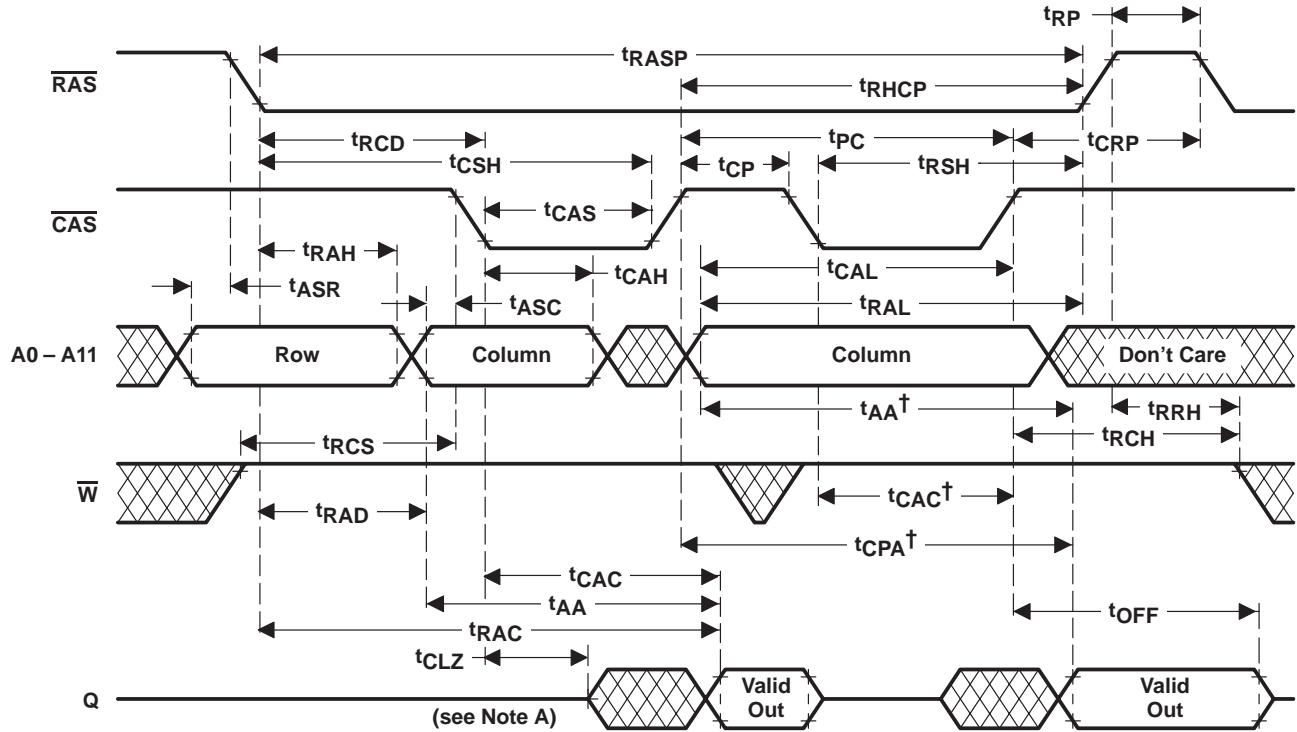
## PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from 3-state to an invalid data state prior to the specified access time.

### Figure 6. Read-Write-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION

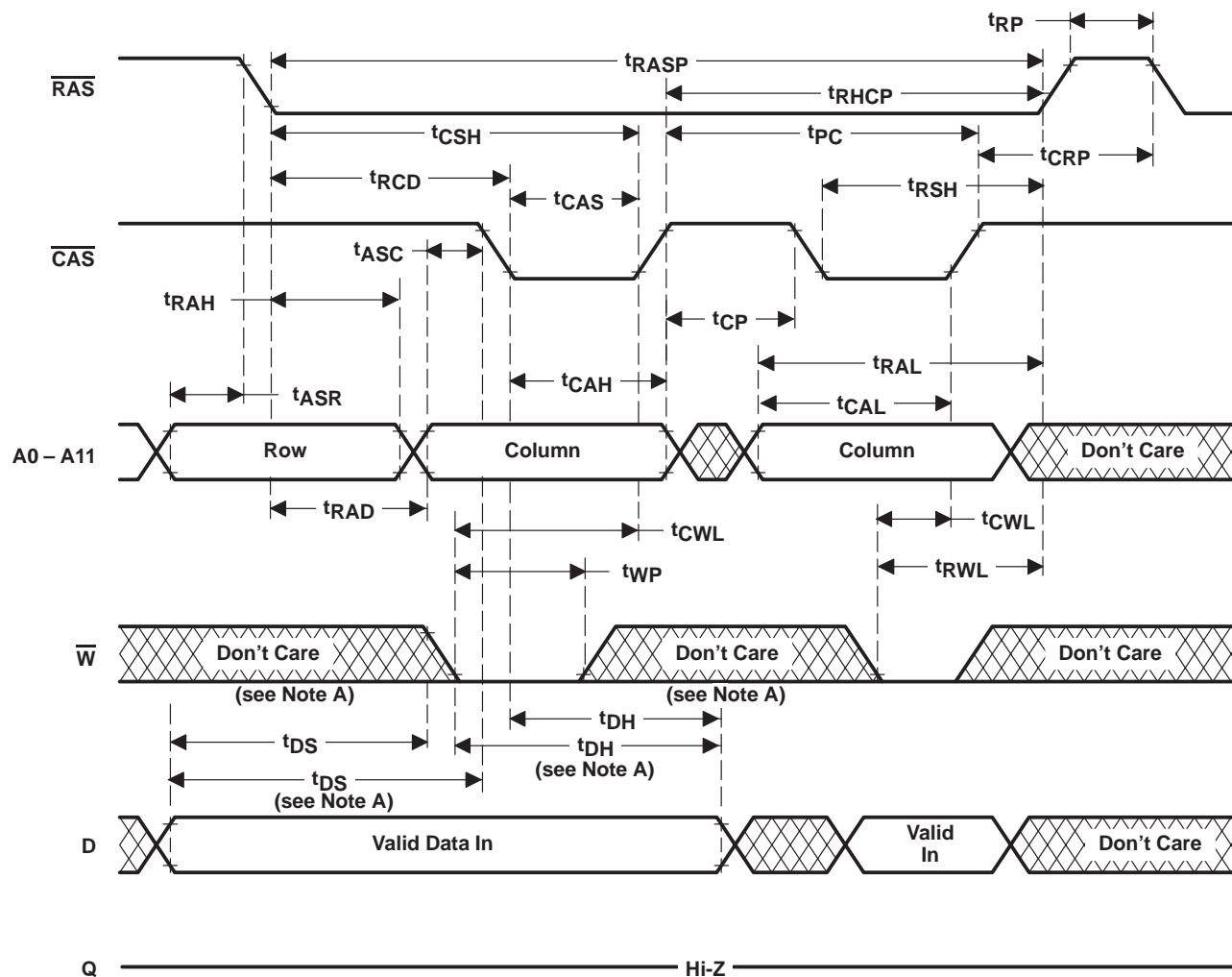


<sup>†</sup> Access time is  $t_{CPA}$ ,  $t_{CAC}$ , or  $t_{AA}$  dependent.

NOTE A: Output can go from 3-state to an invalid data state prior to the specified access time.

Figure 7. Enhanced-Page-Mode Read-Cycle Timing

## PARAMETER MEASUREMENT INFORMATION

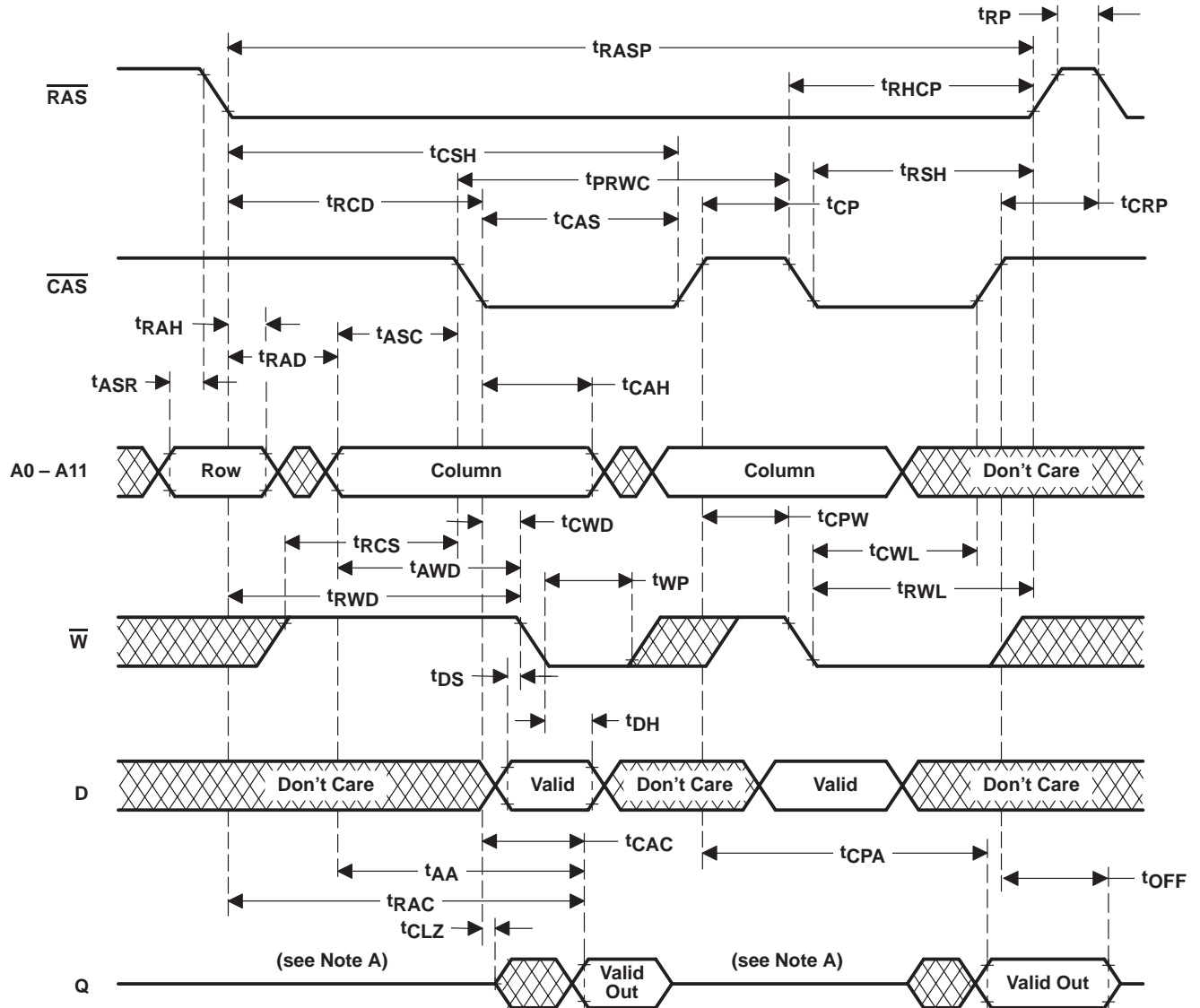


- NOTES: A. Referenced to  $\overline{\text{CAS}}$  or  $\overline{\text{W}}$ , whichever occurs last  
B. A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing



# PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output can go from 3-state to an invalid data state prior to the specified access time.  
B. A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

**Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing**

## PARAMETER MEASUREMENT INFORMATION

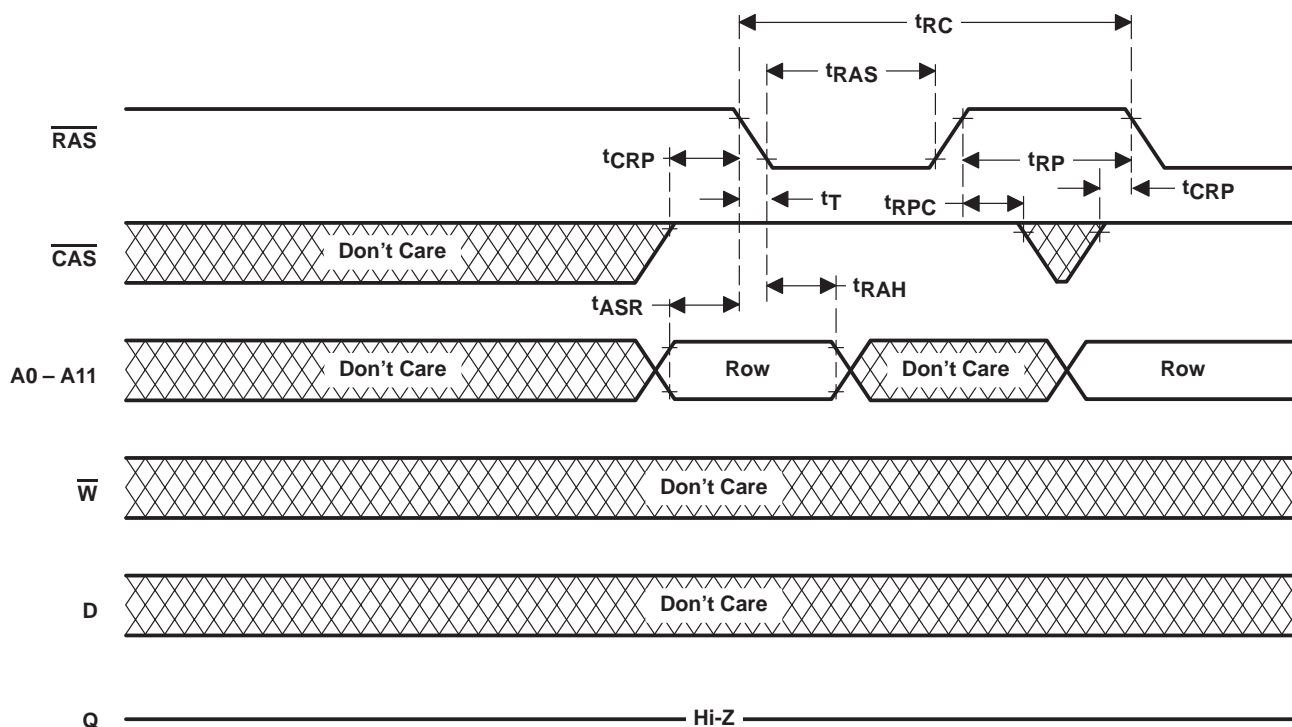


Figure 10.  $\overline{RAS}$ -Only-Refresh-Cycle Timing

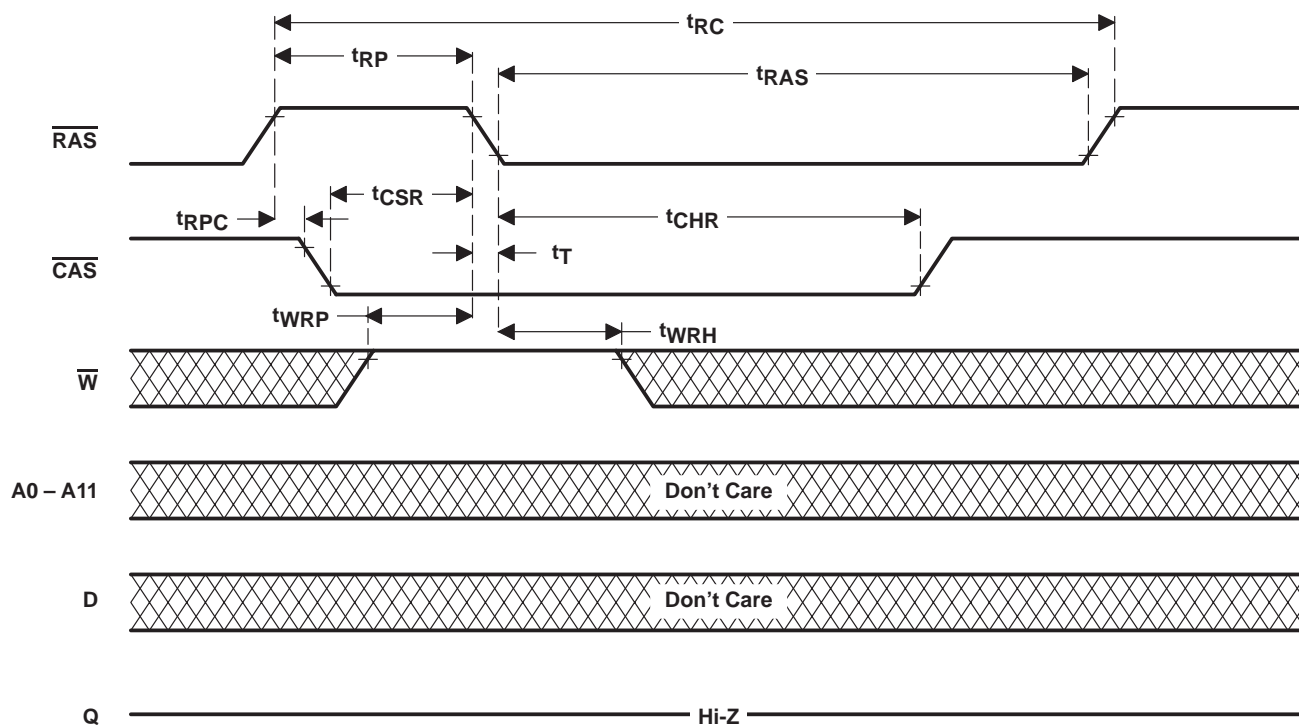


Figure 11. Automatic ( $\overline{CAS}$ -Before- $\overline{RAS}$ ) Refresh-Cycle Timing

The diagram illustrates the timing relationships for a memory device. The signals shown are  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\text{A0-A11}$ ,  $\overline{\text{W}}$ ,  $\text{D}$ , and  $\text{Q}$ . The diagram is divided into Memory Cycles and Refresh Cycles. Key timing parameters include  $t_{\text{RAS}}$  (RAS pulse width),  $t_{\text{RP}}$  (RAS precharge time),  $t_{\text{CAS}}$  (CAS pulse width),  $t_{\text{CH}}$  (CAS hold time),  $t_{\text{CAH}}$  (CAS afterpulse hold time),  $t_{\text{ASC}}$  (Address Setup time),  $t_{\text{RAH}}$  (RAS Afterpulse Hold time),  $t_{\text{ASR}}$  (Address Setup time),  $t_{\text{RRH}}$  (Row Refresh Hold time),  $t_{\text{WRH}}$  (Write Refresh Hold time),  $t_{\text{RCS}}$  (RAS to CAS delay),  $t_{\text{WRP}}$  (Write Refresh Precharge time),  $t_{\text{CAC}}$  (CAS Afterpulse to Address Setup time),  $t_{\text{AA}}$  (Address Afterpulse to Address Setup time),  $t_{\text{RAC}}$  (RAS Afterpulse to Address Setup time),  $t_{\text{CLZ}}$  (CAS to Address Setup time),  $t_{\text{OFF}}$  (RAS to Address Setup time), and Valid Data (Data Validity time).



## PARAMETER MEASUREMENT INFORMATION

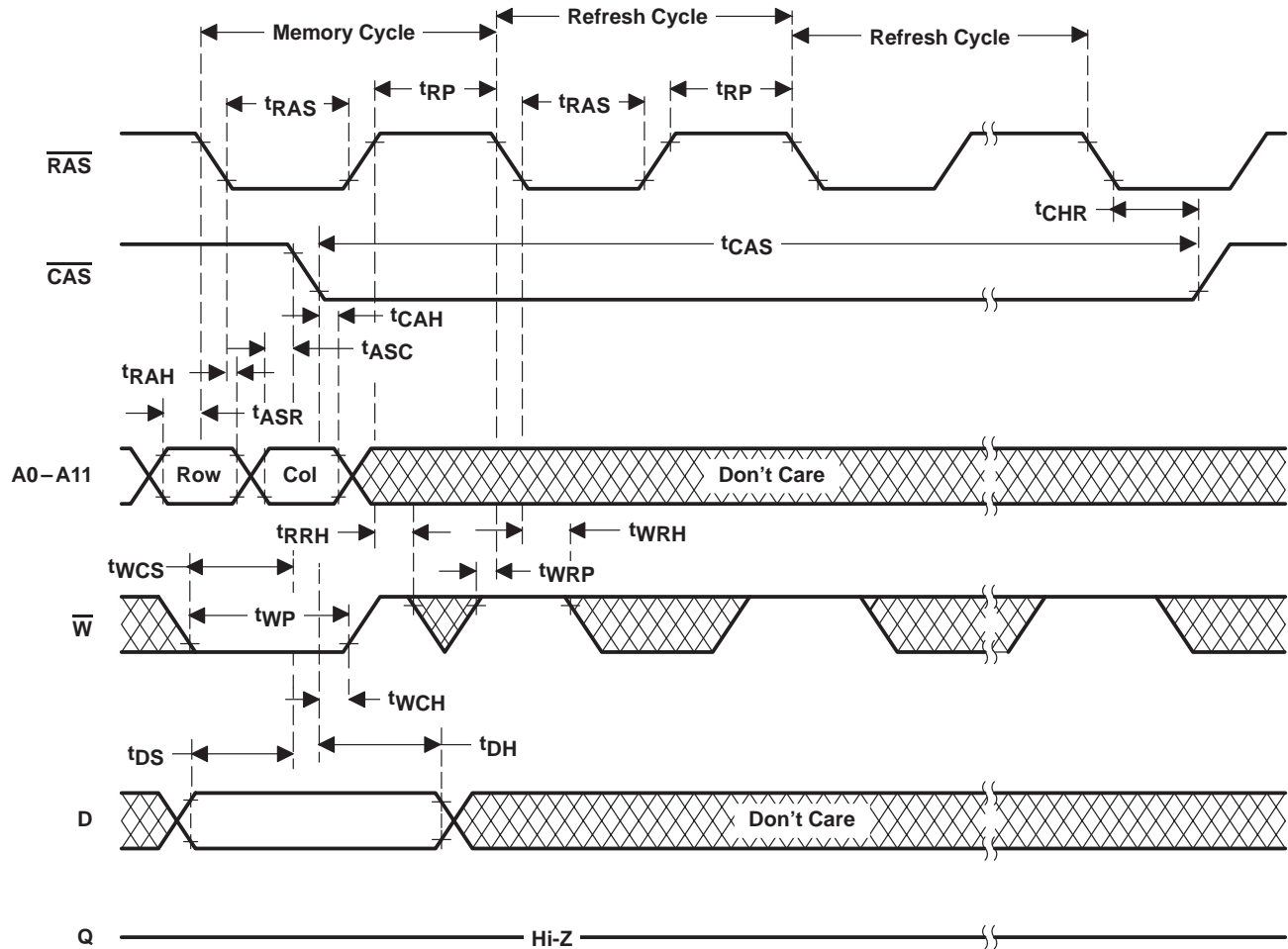


Figure 13. Hidden-Refresh-Cycle (Write) Timing

PARAMETER MEASUREMENT INFORMATION

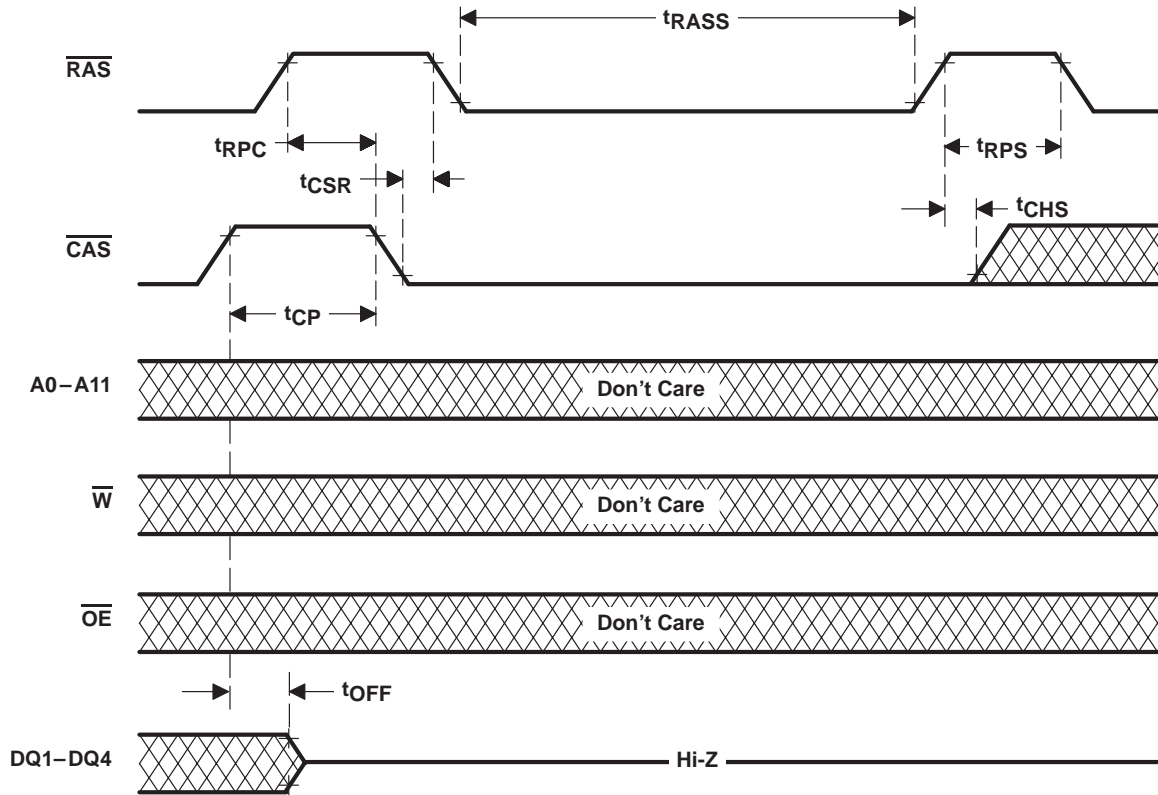
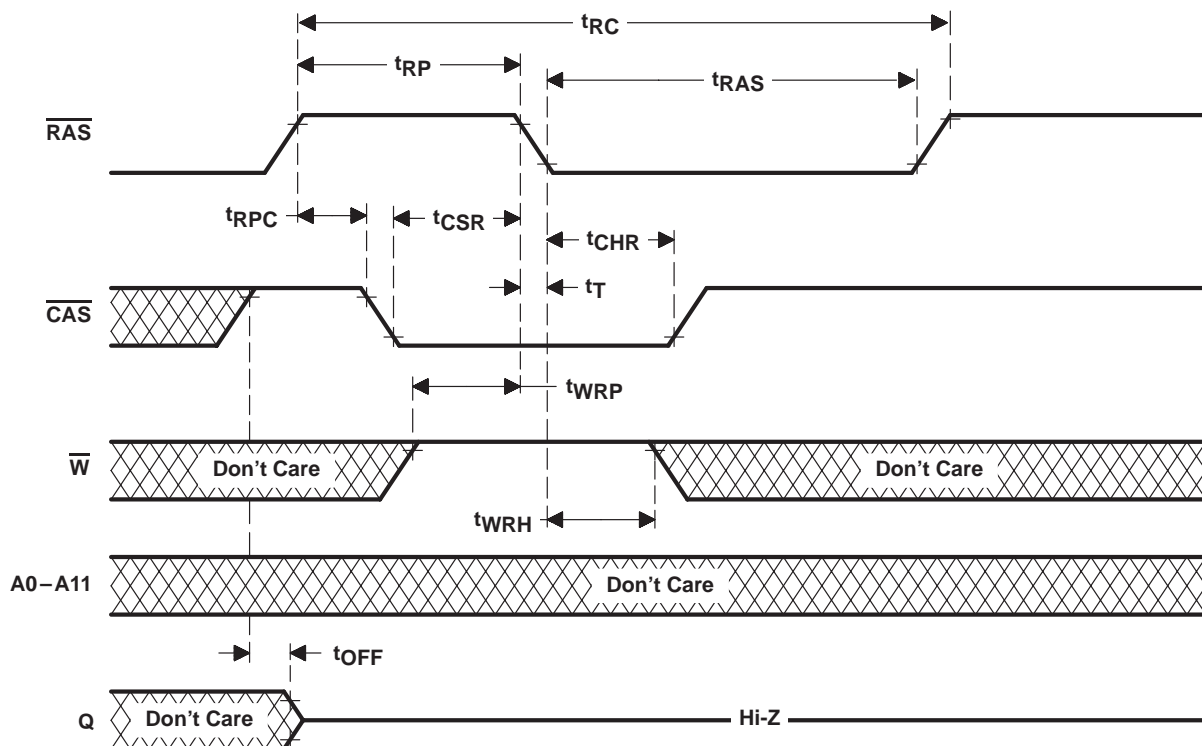
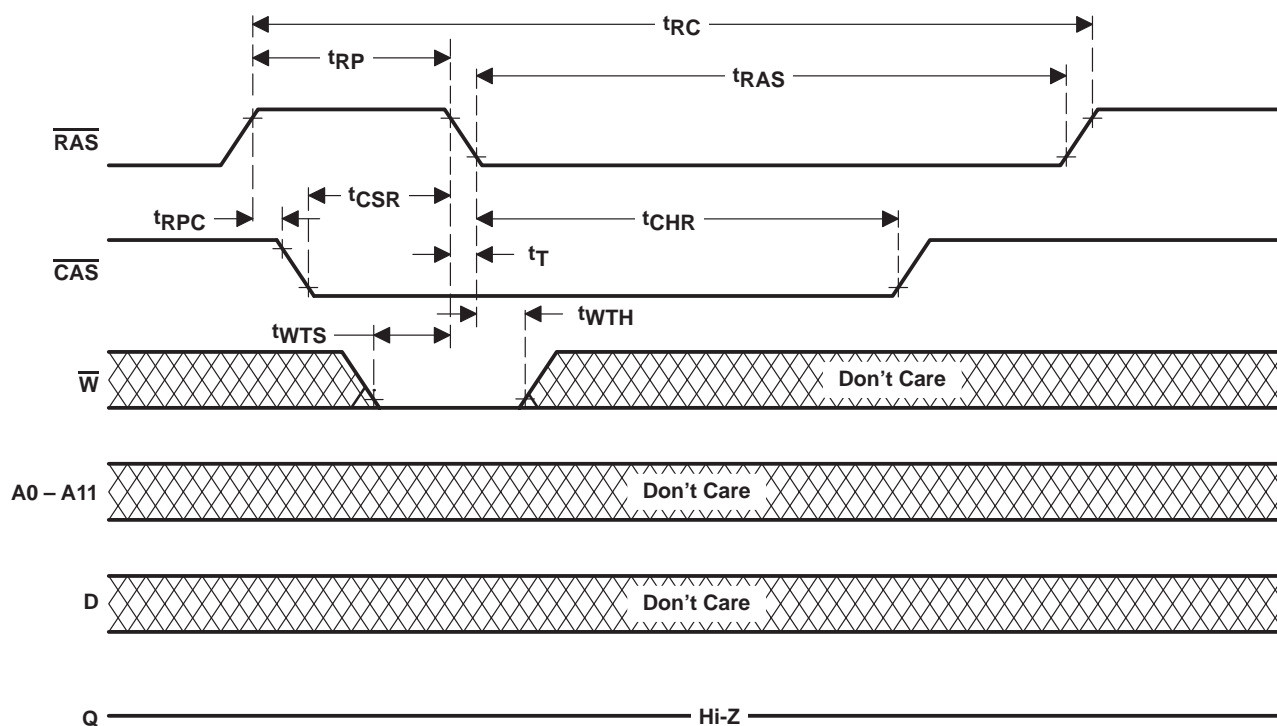


Figure 14. Self-Refresh-Cycle Timing

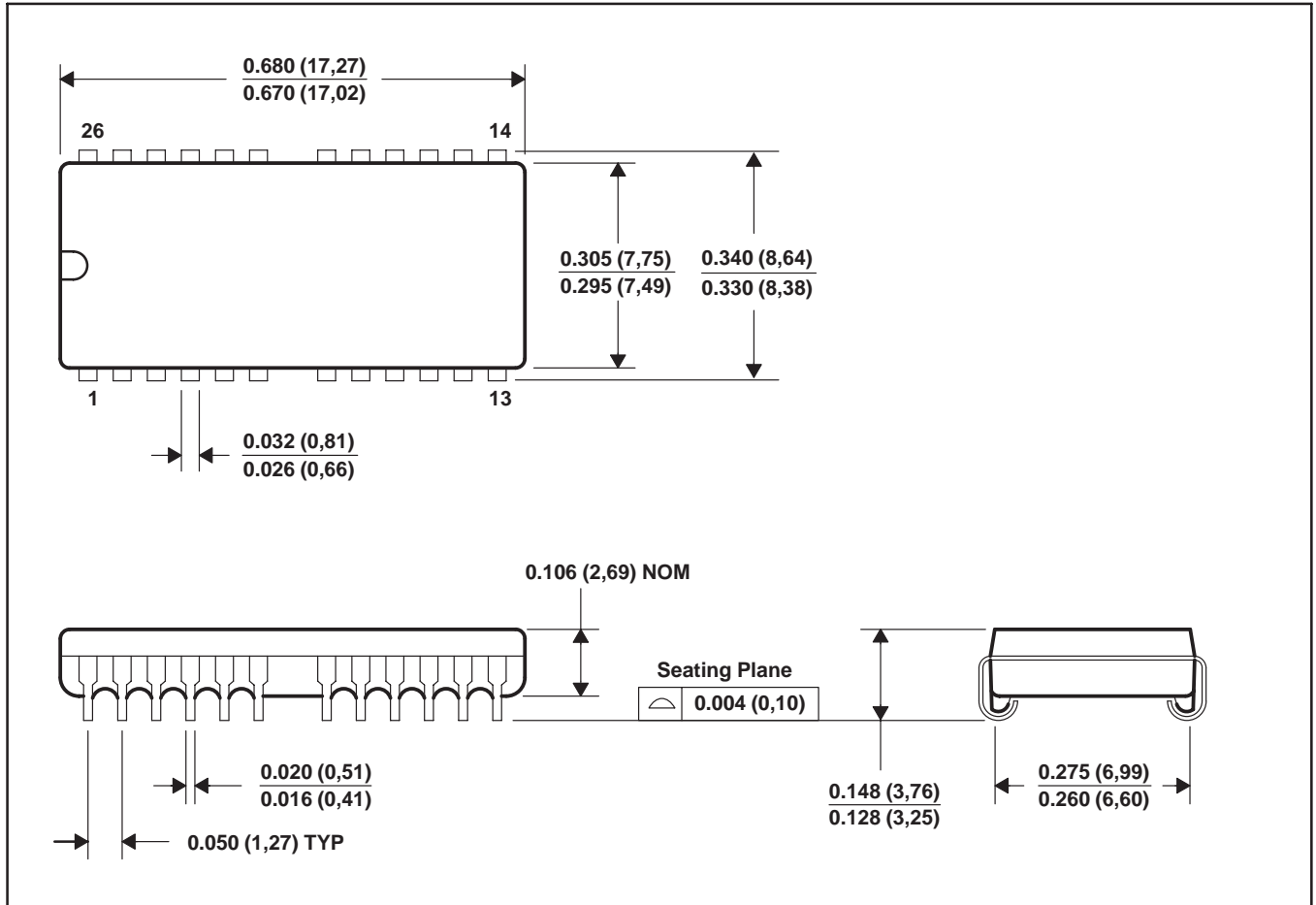
# PARAMETER MEASUREMENT INFORMATION



## MECHANICAL DATA

DJ-24/26 LEAD PLASTIC SMALL-OUTLINE J-LEAD PACKAGE

R-PDSO-J24/26

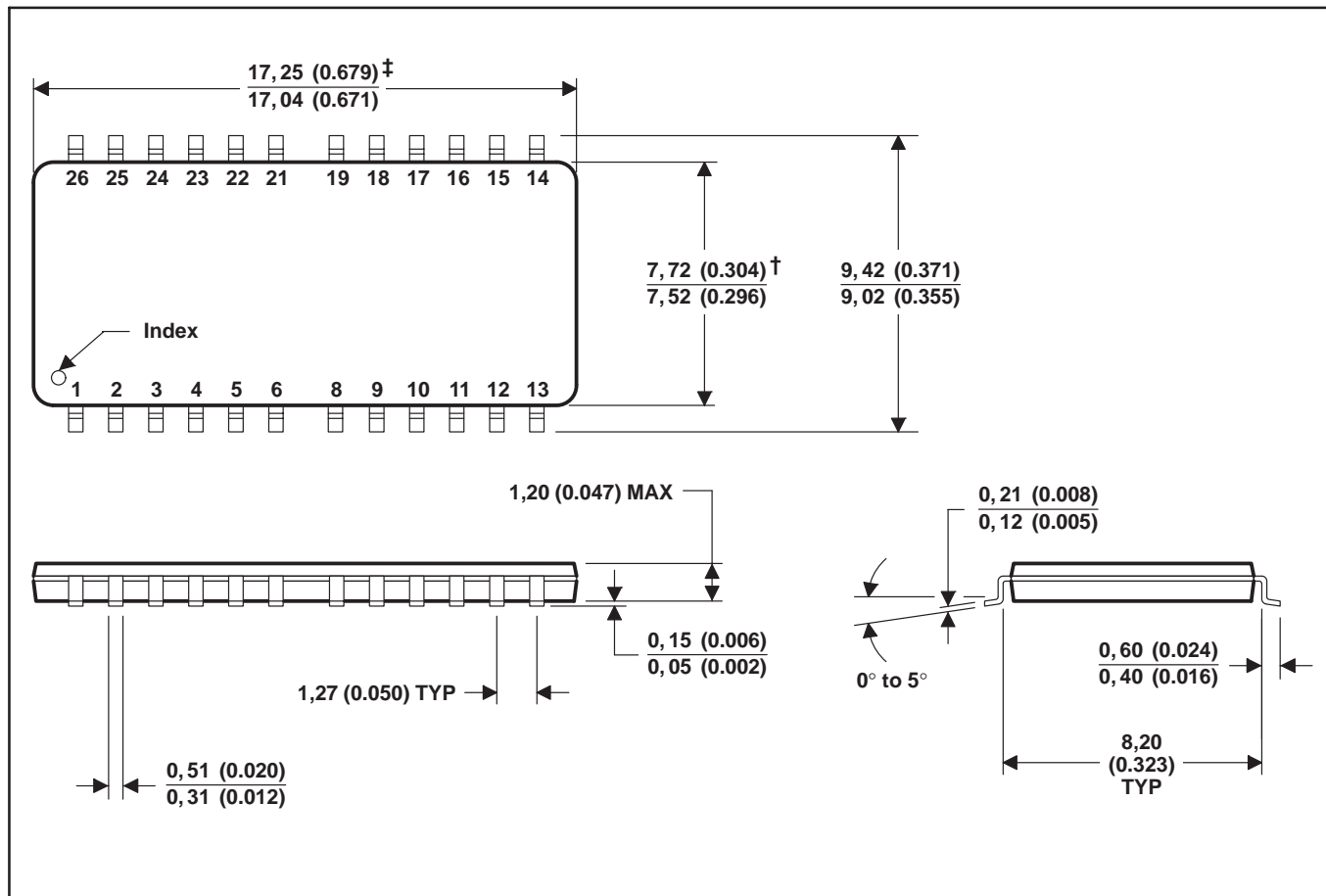


- NOTES: A. All linear dimensions are in inches (millimeters).  
B. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

## MECHANICAL DATA

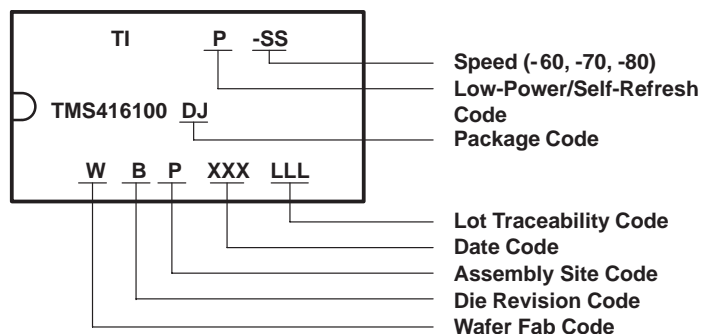
DGA-24/26 LEAD PLASTIC THIN SMALL-OUTLINE PACKAGE

R-PDSO-G24/26



† Plastic body width does not include mold protrusion. Maximum mold protrusion is 0,25 ( 0.010) per side from the edge of the package bottom.  
‡ Plastic body length does not include mold protrusion. Maximum mold protrusion is 0,15 (0.006) per side from the edge of the package bottom.  
NOTE A: All linear dimensions are in millimeters and parenthetically in inches.

## device symbolization





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