Preliminary

Am7985A

FDDI ENDEC Data Separator (EDS)

Advanced Micro Devices

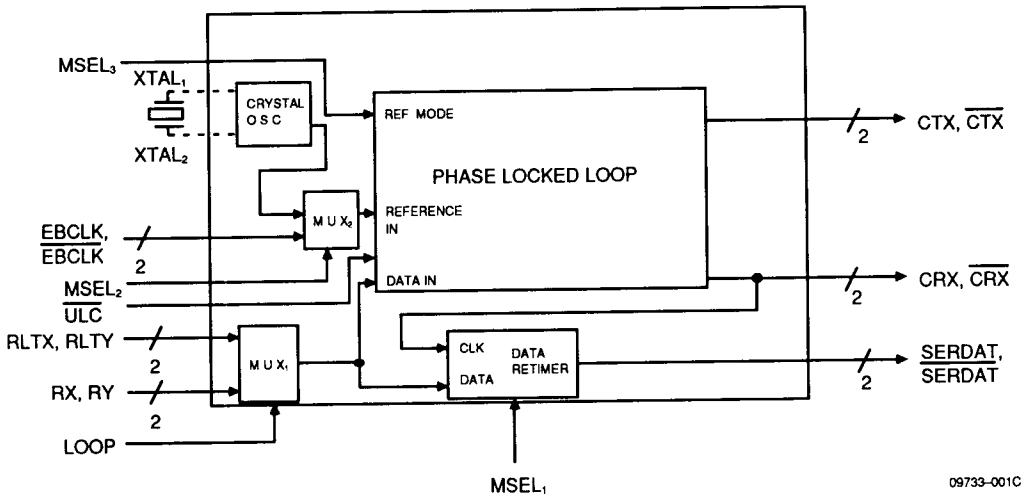
DISTINCTIVE CHARACTERISTICS

- 100 Mbps, 125 MBaud serial input
- Clock recovery
- Meets ANSI X3T9.5 Jitter Requirements
- Selectable loopback modes
- Single +5-V supply

GENERAL DESCRIPTION

The Am7985A ENDEC Data Separator (EDS) recovers clock and data from an FDDI bit stream. Running from a single +5-V supply, this device needs only a clock source (generally provided by an Am7984A ENDEC) to fulfill its role in the AMD SUPERNET chip set.

BLOCK DIAGRAM



NOTE:
The word "frame" is used in the SUPERNET data sheets to describe two different groups of information.

1) One group is passed over the network media and is structured as follows:

Frame Preamble	Start Delimiter	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence	End Delimiter	Frame Status

2) The second is stored in buffer memory and is structured as follows:

A) Transmit frame

Descriptor	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence	Pointer

B) Receive frame

Descriptor	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence

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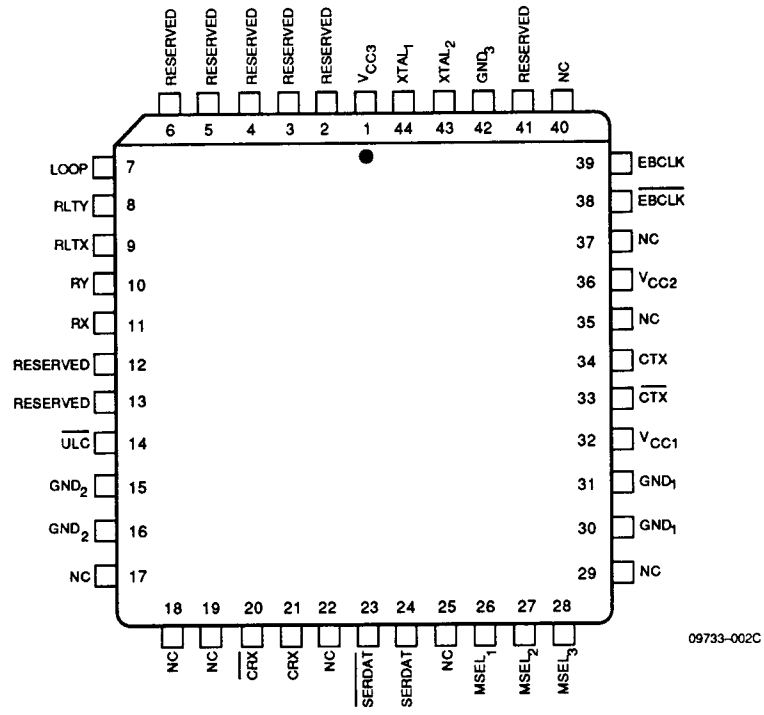
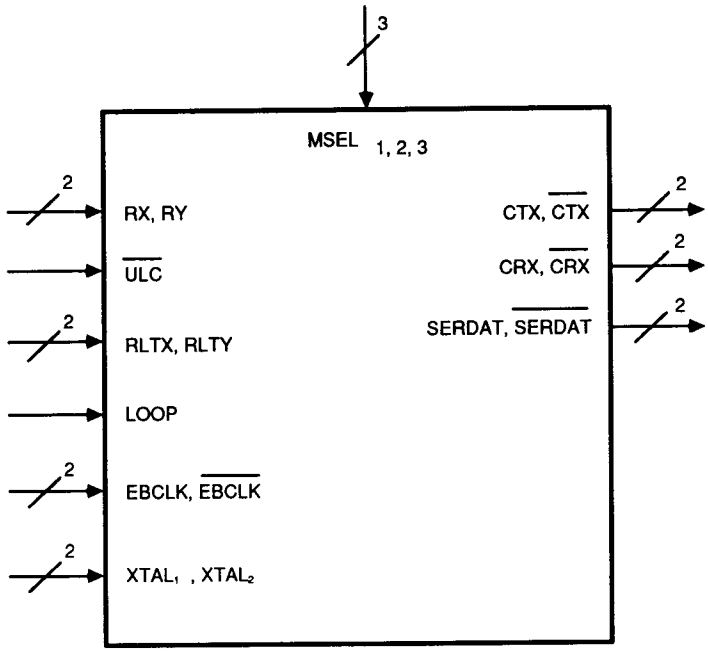
CONNECTION DIAGRAM
PL044 (Top View)

PLCC



LOGIC SYMBOL



V_{CC} = Power (3)
GND = Ground (3)

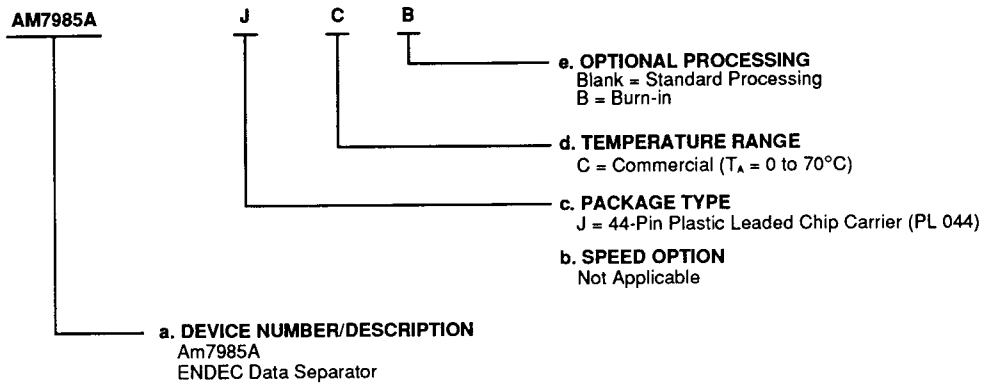
09733-003C

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7985A	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Optical Receiver Interface

RX, RY

Receive+, Receive- (Differential Pseudo-ECL Inputs)

RX and RY are differential 100K pseudo-ECL signals coming from the fiber optic receiver. They represent the serial data sent by the upstream node. These signals are referenced to +5 volts. If RY is grounded, then RX will become a single-ended 100K pseudo-ECL input.

ENDEC Interface

The following section describes the pins which connect to the Am7984A ENDEC.

CRX, $\overline{\text{CRX}}$

Clock Receive+, Clock Receive- (Differential CML/ECL Output)

The bit rate clock, derived from the received serial data (RX, RY, or RLTX, RLTY), is sent to the ENDEC using CRX, $\overline{\text{CRX}}$.

CTX, $\overline{\text{CTX}}$

Clock Transmit+, Clock Transmit- (Differential Pseudo-ECL Output)

CTX, $\overline{\text{CTX}}$ are differential output signals from the EDS and are used as the transmit bit clock for the ENDEC when it is in Test Mode. They are synchronous to either EBCLK or the internal crystal oscillator output depending on the state of the $MSEL_2$ pin. When $MSEL_2$ is floating, CTX is synchronous to the crystal oscillator. When $MSEL_2$ is connected to ground or V_{CC}, CTX is synchronous to EBCLK. When these signals are not used to drive CTX, $\overline{\text{CTX}}$ on the ENDEC, they should be terminated directly to V_{cc}.

EBCLK, $\overline{\text{EBCLK}}$

ECL Byteclock+, ECL Byteclock- (Differential Pseudo-ECL Input)

EBCLK, $\overline{\text{EBCLK}}$ are differential signals from the ENDEC. They serve as the frequency reference for the Phase Locked Loop. EBCLK, $\overline{\text{EBCLK}}$ can also come from an external source. When $\overline{\text{EBCLK}}$ is grounded, EBCLK becomes single-ended 100K Pseudo ECL input.

LOOP

Loop (Pseudo-ECL Input; active HIGH)

The LOOP signal, when active, tells the 7985A to loop the transmit output from the Am7984A back into the Am7985A receive input for diagnostic purposes. In this mode, the retimed data and recovered clock correspond to the data received in RLTX and RLTY.

RLTX, RLTY

Receive Loop Transmit+ Receive Loop Transmit- (Pseudo-ECL Inputs)

RLTX and RLTY are differential signals coming from the Am7984A ENDEC and are used when the LOOP pin is active (HIGH). This input signal is in NRZI form; a transition occurs during every logic "1" in the encoded data; logic "0" is represented by a steady signal with no transition. RLTX and RLTY are synchronous with the transmit bit clock. If RLTY is grounded, RLTX becomes a single ended 100K Pseudo-ECL input.

SERDAT, $\overline{\text{SERDAT}}$

Serial DATA+, Serial DATA- (Differential CML/ECL Output)

SERDAT, $\overline{\text{SERDAT}}$ represent the retimed receive data, synchronous to the falling edge of CRX. This is then sent to the ENDEC to be decoded.

$\overline{\text{ULC}}$ (Active LOW)

$\overline{\text{Use Local Clock}}$ (Single-Ended Pseudo-ECL Input)

$\overline{\text{ULC}}$, when HIGH, causes the PLL in the EDS to track the received data, or when LOW causes the PLL in the EDS to track the local bit clock (CTX) divided by two. CRX and SERDAT are derived from the chosen signal.

Crystal Pins

$XTAL_1$, $XTAL_2$

Crystal1, Crystal2 (Inputs)

These two crystal inputs connect to a parallel mode oscillator which operates at the fundamental frequency of the crystal. Either the crystal oscillator output or the EBCLK, $\overline{\text{EBCLK}}$ differential input can be selected as the frequency reference for the Phase Locked Loop by appropriate selection of $MSEL_2$ pin. When $MSEL_2$ is floating, the crystal oscillator is used as the reference. If the crystal oscillator is not used, $XTAL_1$ is grounded. $XTAL_1$ may be used as a TTL clock source input by grounding pin $XTAL_2$ and floating $MSEL_2$.

Mode Select Pins

$MSEL_1$

Mode Select 1 (3-State Input)

The $MSEL_1$ pin selects the data translation between the input and SERDAT, $\overline{\text{SERDAT}}$ pins. When $MSEL_1$ is connected to ground, the SERDAT, $\overline{\text{SERDAT}}$ outputs are converted from NRZI to NRZ form. When $MSEL_1$ is floating or connected to Vcc; the SERDAT and $\overline{\text{SERDAT}}$ outputs are not converted (they remain in NRZI form). When $MSEL_1$ is connected to V_{cc}, CTX, and

$\overline{CTX}$ are off. In the normal mode of operation, this pin is floating.

$MSEL_2$
Mode Select 2 (3-State Input)

The $MSEL_2$ pin selects the frequency reference for the PLL in the EDS. When $MSEL_2$ is floating, the crystal oscillator is used as the reference. When $MSEL_2$ is connected to ground or connected to V_{cc}, EBCLK is used as the reference. In the normal mode of operation, this pin is connected to ground.

$MSEL_3$
Mode Select 3 (3-State Input)

The $MSEL_3$ pin selects the frequency multiplication rate. When $MSEL_3$ is connected to ground, the frequency reference (either EBCLK or the internal crystal oscillator) is multiplied by ten to generate transmit bit rate clock (CTX). When $MSEL_3$ is floating, the frequency reference is multiplied by five. When $MSEL_3$ is connected to V_{CC}, the frequency reference is the same as that of the bit clock. In the normal mode of operation, this pin is connected to ground.

Power Supply

GND_1, GND_2, and GND_3
Ground

GND_1 is for input/output circuits, GND_2 is for internal CML logic, and GND_3 is for the oscillator.

V_{CC1}, V_{CC2}, V_{CC3}
Power Supply

These are +5-V nominal power supply pins. V_{cc1} powers input/output circuits, V_{cc2} powers internal CML logic, and V_{cc3} powers the oscillator.

FUNCTIONAL DESCRIPTION

The ENDEC and EDS implement the Fiber Distributed Data Interface (FDDI) physical layer protocol standards as defined by ANSI X3T9.5. There are five major sections in the EDS They are: Mux_1 Crystal Oscillator, Mux_2, the PLL, and the data retimer.

Overview Of User Accessible Resources

1) The EDS can output the retimed data in the form of NRZI (same format as RX, RY) or NRZ (transitions converted to "1" non transitions converted to "0".) form by the use of the $MSEL_1$ pin. When $MSEL_1$ is connected to ground, the output is in NRZ form. When $MSEL_1$ is floating or connected to V_{CC}, the output is in NRZI form.
2) The frequency reference for the PLL is selected to be either an external clock source (through the EBCLK, $\overline{EBCLK}$ pins) or the internal crystal oscillator by using the $MSEL_2$ pin. When $MSEL_2$ is floating, the crystal oscillator is chosen as the reference. When $MSEL_2$ is connected to ground or V_{CC}, EBCLK is chosen as the reference.
3) The frequency multiplication factor for the PLL is chosen by programming the $MSEL_3$ pin. When $MSEL_3$ is connected to ground, the frequency reference is multiplied by 10 to generate the bit clock. When $MSEL_3$ is floating, the frequency reference is multiplied by five. When $MSEL_3$ is connected to V_{CC}, the frequency reference is the same rate as the bit clock. For normal operation, $MSEL_3$ should be connected to ground.

Block Diagram Description

Mux_1

MUX_1 selects either the RX, RY or the RLTX, RLTY signal-pairs as inputs to the PLL and the data retimer. When the LOOP pin is active (HIGH), the RLTX, RLTY inputs are chosen. When the LOOP pin is LOW, the RX, RY inputs are chosen.

Crystal Oscillator

The crystal oscillator generates the frequency reference for the PLL. The specifications for a suitable crystal are given in the global issues section of this data sheet. If crystal oscillator is not used, the $XTAL_1$ pin should be grounded. $XTAL_2$ should be grounded if the $XTAL_1$ pin is driven by a TTL source.

Mux_2

Mux_2 is used to choose between the crystal oscillator output and the EBCLK, $\overline{EBCLK}$ inputs as the frequency reference for the PLL. The selection is made by the $MSEL_2$ pin. When $MSEL_2$ is floating, the crystal oscillator is used as the reference. When $MSEL_2$ is connected to ground or V_{CC}, EBLK is used as the reference.

PLL

The PLL block is used to recover the receive bit clock (CRX) from the received data stream. The frequency reference for the PLL is either the crystal oscillator output or EBCLK. The PLL block can also be used to generate the transmit bit clock (CTX) for use by an ENDEC (Am7984A) running in Test mode. CTX is synchronous with either the crystal oscillator or EBCLK depending on the state of the $MSEL_2$ pin as described in MUX_2. The PLL can recover CRX with input jitter up to ± 3 nsec. The PLL synchronizes CRX with input data in less than 100 microseconds. In cases where the input data is not usable, as in the case of noise or quiet conditions, the Use Local Clock, ($\overline{ULC}$) pin from the ENDEC is used to switch the frequency and phase reference for CRX from incoming data to $XTAL_1$ or EBCLK. This is done to reduce the time to acquire phase lock when proper data appears on the inputs. The $\overline{ULC}$ signal comes from the ENDEC. When the $\overline{ULC}$ pin is held HIGH, the PLL tracks incoming data and generates CRX. $MSEL_3$ determines the frequency multiplication factor for the PLL which generates CTX.

Data Retimer

The data retiming circuit retimes the received data (either RX, RY, or RLTX, RLTY) and aligns it with the negative edge of the recovered bit clock (CRX). The jitter component in the received input data is removed by the retiming. Encoding of the output signal can be chosen by the $MSEL_1$ pin. When $MSEL_1$ is connected to ground, the output is in NRZ form. When $MSEL_1$ is floating or connected to V_{CC}, the output is in Non-Return to zero Invert on ones (NRZI) form.

Global Issues

Following are the global objectives for the ENDEC.

Maximum Jitter tolerance at the receive input: 5.87 nsec peak-to-peak as specified in the ANSI X3T9.5 PMD document with the individual components of jitter consisting of :

Duty Cycle Distortion	—	1.4 ns (peak to peak)
Data Dependent Jitter	—	2.2 ns (peak to peak)
Random Jitter	—	2.27 ns peak to peak or 0.180 ns RMS (for a bit error rate of 2.5×10^{-10})
Acquisition Time	—	100 µs

Crystal Specifications

Following are the crystal specifications when a byte-rate reference is chosen for the PLL.

1)	Frequency (Fundamental)	12.5 MHz
2)	Resonant Mode	Parallel
3)	Load Capacitor (Correlation)	75 pF
4)	Operating Temperature range	0 to 70°C
5)	Temperature Stability	± 25 parts per million
6)	Drive Level (Correlation)	2 mW
7)	Effective Series Resistance	25 ohms (Max)
8)	Holder Type	Low Profile
9)	Aging for 10 years	± 10 ppm

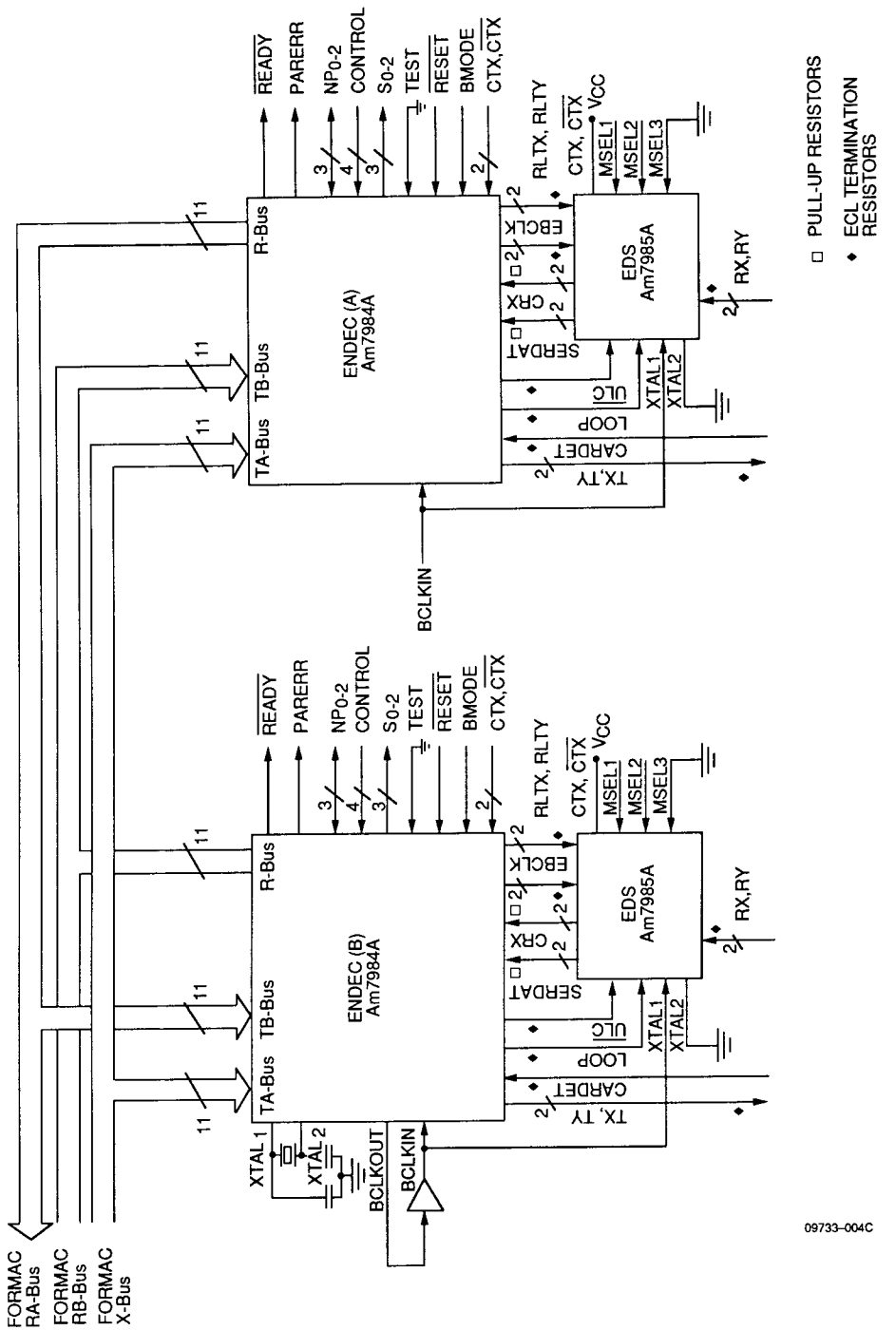


Figure 1: ENDEC-EDS Interconnections in a Dual-attach Station

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Ambient Temperature Under Bias	–55 to +125°C
Supply Voltage to Ground Potential Continuous	–0.5 to + 7.0 V
DC Voltage Applied to Outputs	–0.5 to V_{CC} Max.
DC Input Voltage	–0.5 to +5.5 V
DC Output Current	±100 mA
DC Input Current	–30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Extended Commercial (E) Devices

Case Temperature (T_C)	–55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Notes 1 & 5)		Min.	Max.	Unit
CML/ECL OUTPUT PINS (SERDAT, $\overline{\text{SERDAT}}$, CRX, $\overline{\text{CRX}}$, CTX, $\overline{\text{CTX}}$)						
I_{OH}	Output HIGH Current	V_{CC} = Max. V_{OH} = V_{CC}	R_L = 50Ω		100	µA
I_{OL}	Output Low Current	V_{CC} = Min. V_{OL} - 2.5 V (Note 7)	R_L = 50Ω	4		mA
ECL INPUT PINS (RX, RY, LOOP, $\overline{\text{ULC}}$, EBCLK, $\overline{\text{EBCLK}}$, RLTX, RLTY)						
V_{IHS}	Input HIGH Voltage	V_{CC} = Max. (Note 4)		(V_{CC} - 1.165)	(V_{CC} - 0.88)	V
V_{ILS}	Input LOW Voltage	V_{CC} = Max. (Note 4)		(V_{CC} - 1.81)	(V_{CC} - 1.475)	V
V_{DIFF}	Differential Input Voltage (Pins RX and RY or pins RLTX and RLTY)	V_{CC} = Max.		0.2	1.1	V
V_{ICM}	Input Common Mode Voltage (Pins RX and RY or pins RLTX and RLTY)	Note 3		3.05	V_{CC} - 1/2 V_{DIFF}	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} - 1.81 V		0.5		µA
I_{IL}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} - 0.88V			220	µA
POWER SUPPLY PINS (V_{CC1}, V_{CC2}, V_{CC3})						
I_{CC}	Supply Current	V_{CC1}= Max V_{CC2} = Max V_{CC3} = Max., (Note 3)	Pin V_{CC1} (I/O) Pin V_{CC2} (CML) Pin V_{CC3} (OSC) Total @ +125°C Total @ +25°C Total @ -55°C		 200 	mA mA mA mA mA mA

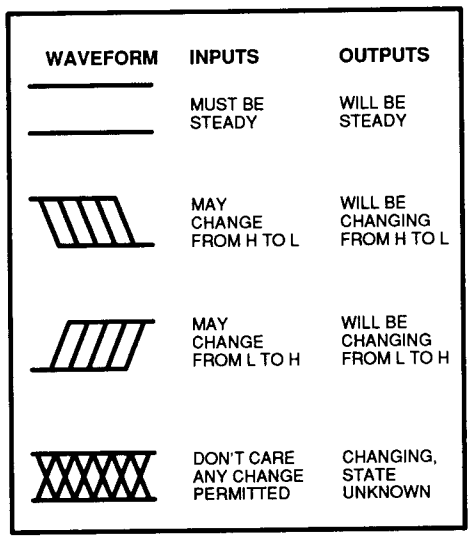
SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 2 and 6)

No.	Parameter	Signal Name		Min.	Max.	Unit
1	Clock Period	EBCLK,	$\overline{\text{EBCLK}}$	80		ns
2	HIGH Pulse Width	EBCLK,	$\overline{\text{EBCLK}}$	35		ns
3	LOW Pulse Width	EBCLK,	$\overline{\text{EBCLK}}$	35		ns
4	Data Valid prior to CRX	SERDAT,	$\overline{\text{SERDAT}}$	0.025 x T1		ns
5	Data Valid after CRX	SERDAT,	$\overline{\text{SERDAT}}$	0.025 x T1		ns
6	Transition Interval	RX,	$\overline{\text{RY}}$	0.1 x T1		ns
7	Delay from RX, RY or RLTX, RLTY	SERDAT,	$\overline{\text{SERDAT}}$	(0.1 x T1) + 1	(0.2 x T1) + 5	ns
8	Delay from EBCLK or $XTAL_1$	CTX,	$\overline{\text{CTX}}$	1.5	(0.05 x T1) +1.5	ns

Notes:

1. For conditions shown as Min. or Max., use the appropriate value specified under operating ranges.
2. All timing references are made with respect to the 50% point between V_{OH} and V_{OL} for ECL signals. ECL input rise and fall times must be 2 ns ± 0.2 ns between 20% and 80% points. V_{OUT} for these pins should not be above V_{CC} or below +2.5V to assure proper operation. They are typically connected through a 50n resistor to V_{CC}.
3. Voltage applied to any of RX, RY, RLTX, RLTY pins must not be above V_{CC} or below +2.5V to assure proper operation.
4. Measured with device in test mode while monitoring output logic states.
5. Nominal input voltages are V_{CC} - 0.9 V or V_{CC} - 1.7V on ECL input pins.
6. All testing is done with T1 = 80ns.
7. V_{OUT} for these pins should not be above V_{CC} or below +2.5 V to assure proper operation. They are typically connected through a 50Ω resistor to V_{CC}.

Key to Switching Waveforms



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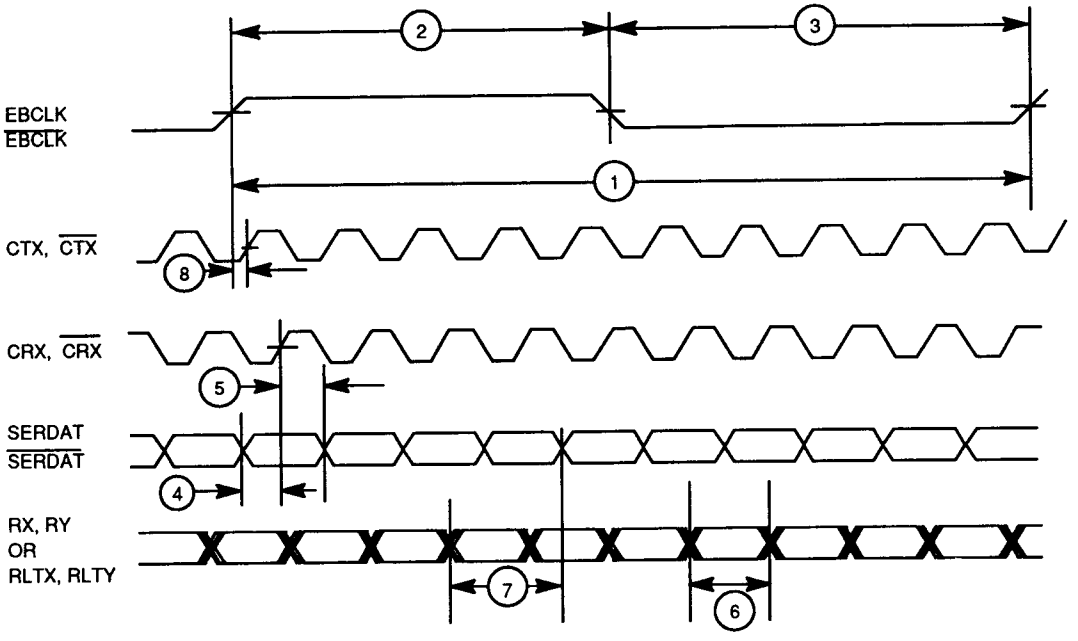
SWITCHING WAVEFORMS



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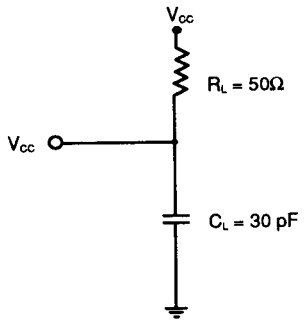
Clock & Data Timing

SWITCHING TEST CIRCUITS



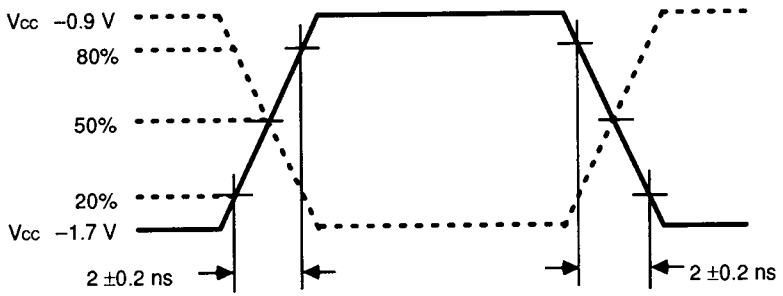
A. CML/ECL Output Load

09733-006B

Notes:

1. C_L includes scope probe, wiring, and stray capacitances without device in test fixture.
2. AMD uses ATE load configurations and forcing functions. This figure is for reference only.

SWITCHING TEST WAVEFORMS



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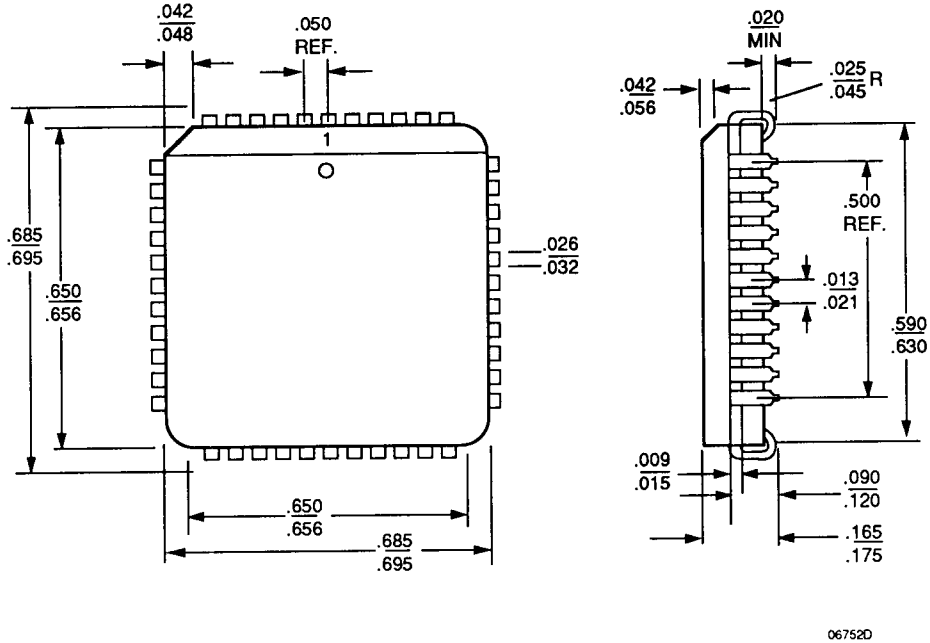
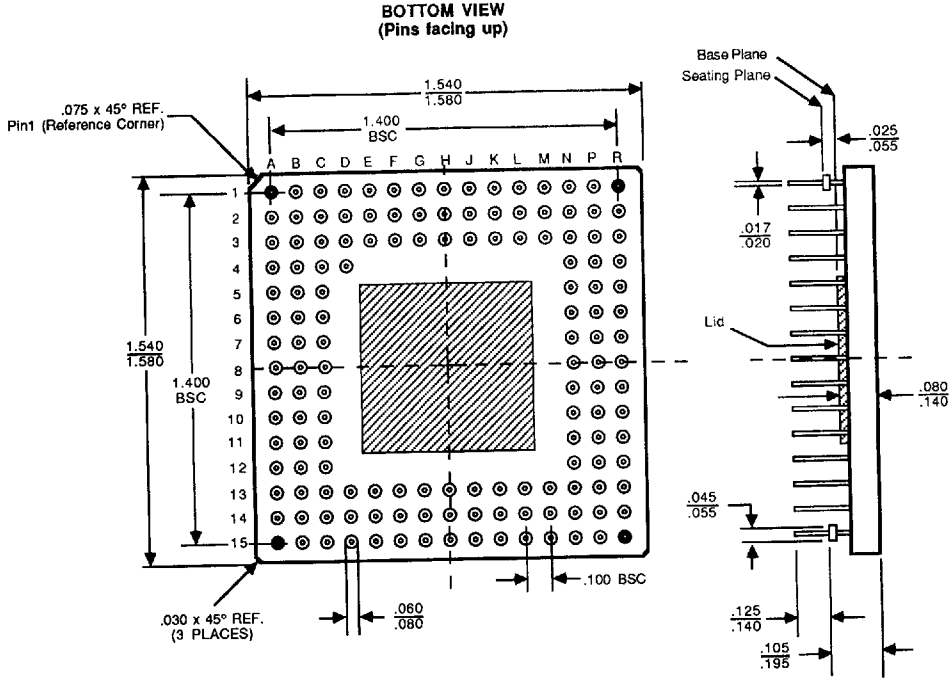
ECL Input Waveform

PHYSICAL DIMENSIONS
PL 044



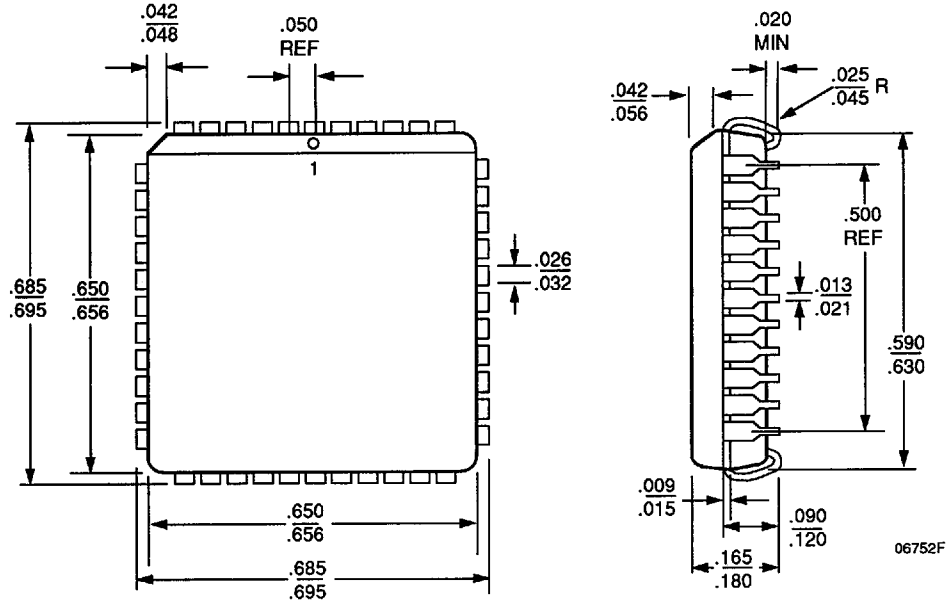
T-90-20

CGX145
145-Lead Pin Grid Array without Heat Sink

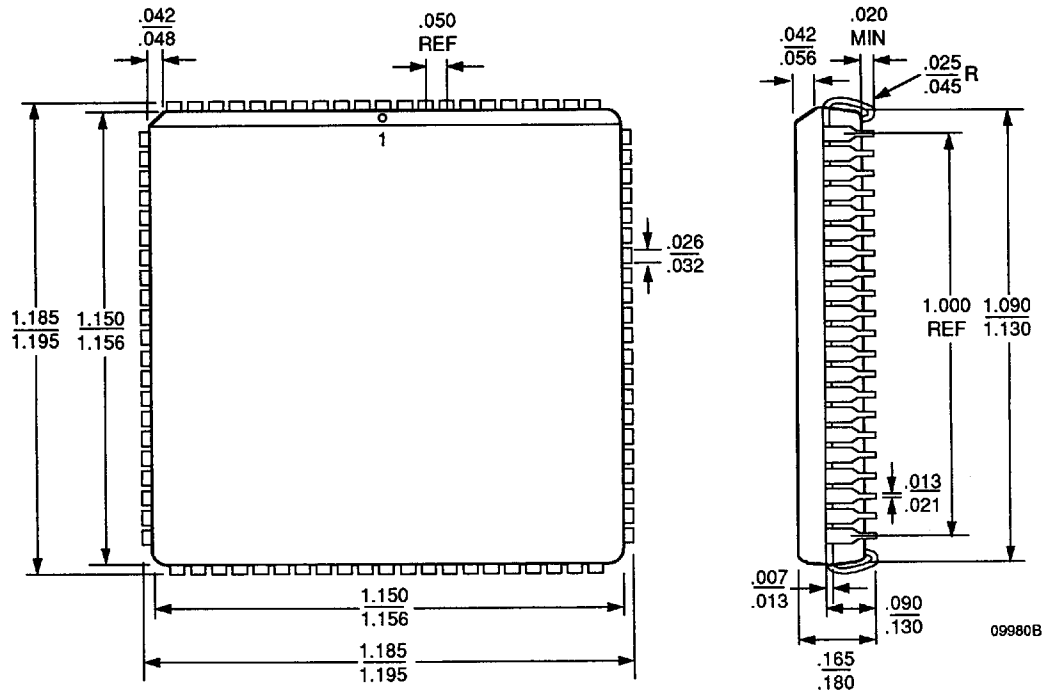


PID # 09691B

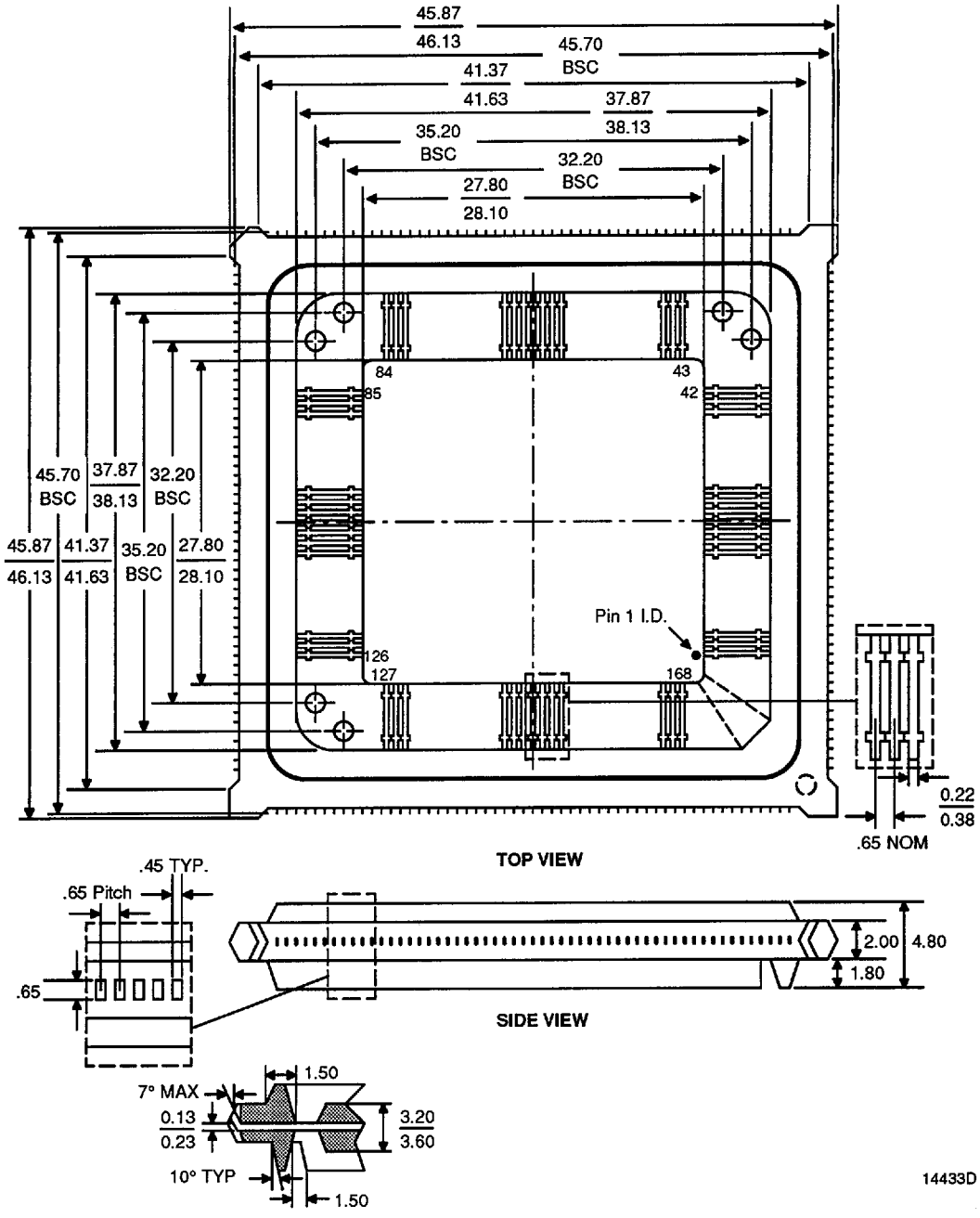
PL 044
44-Pin Plastic Leaded Chip Carrier



PL 084
84-Pin Plastic Leaded Chip Carrier

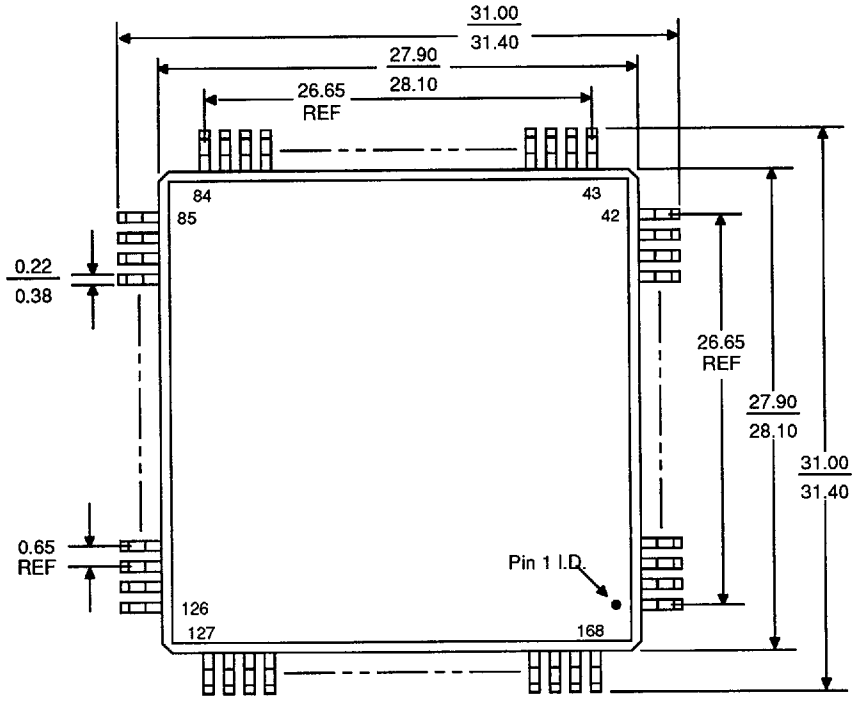


PQR168**
168-Pin Plastic Quad Flat Pack (Tape Pak)

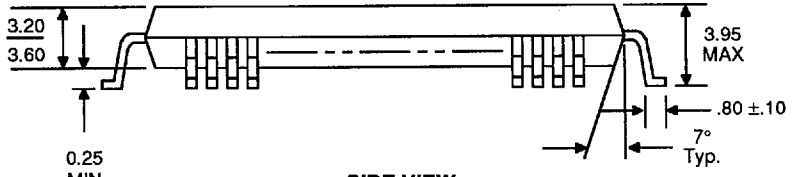


**Measured in Millimeters

PQJ168**
168-Pin Plastic Quad Flat Pack (Trimmed and Formed)



TOP VIEW



SIDE VIEW

**Measured in Millimeters