

T-75-57

DISTINCTIVE CHARACTERISTICS

- ## GENERAL DESCRIPTION

four bit times, and decodes Manchester data with worst case ± 19 ns phase jitter at 10 MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

The diagram illustrates the internal architecture of the 68180 SPI. It is divided into two main sections: the **Controller Interface** on the left and the **Transceiver Interface** on the right.

Controller Interface (Left):

- Receive Data (RX):** Connected to the **Manchester Decoder**.
- Receive Clock (RCLK):** Connected to the **Manchester Decoder**.
- Carrier Present (RENA):** Connected to the **Carrier Detect** block.
- Collision (CLSN):** Connected to the **Collision Detect** block.
- Transmit Data (TX):** Connected to the **Manchester Encoder**.
- Transmit Enable (TENA):** Connected to the **Manchester Encoder**.
- Transmit Clock (TCLK):** Connected to the **Manchester Encoder**.

Transceiver Interface (Right):

- Receive +** and **Receive -**: Connected to the **Data Receiver** and **Noise Reject Filter** blocks.
- Collision +** and **Collision -**: Connected to the **Noise Reject Filter** blocks.

Internal Components and Connections:

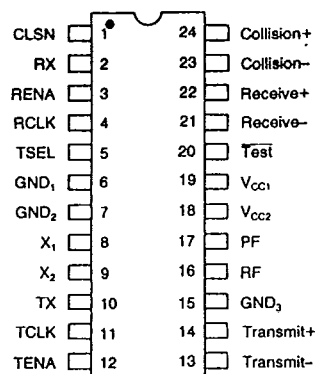
- Manchester Decoder** and **Manchester Encoder** are central processing blocks.
- Carrier Detect** and **Collision Detect** are monitoring blocks.
- Data Receiver** and **Noise Reject Filter** (two instances) are signal conditioning blocks.
- Crystal OSC** (Crystal Oscillator) provides the clock signal. It is connected to **XTAL₁** and **XTAL₂** pins, which are also connected to a **20 MHz** crystal.

BD002071

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE-802.3/Ethernet/Cheapernet/Transceiver

<u>Publication #</u>	<u>Rev.</u>	<u>Amendment</u>
03378	F	/0
Issue Date: March 1989		

CONNECTION DIAGRAM



CD001521

Note: Pin 1 is marked for orientation

ORDERING INFORMATION AMD STANDARD PRODUCTS

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing

Am7992B

D

C

B

e. OPTIONAL PROCESSING

Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE

C = Commercial (0 to +70°C)

c. PACKAGE TYPE

D = 28-Pin (Slim) Ceramic DIP (CD3024)

b. SPEED OPTION

Not Applicable

a. DEVICE NUMBER/DESCRIPTION

Am7992B
Serial Interface Adapter

Valid Combinations

AM7992B	DC, DCB
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Valid Combinations

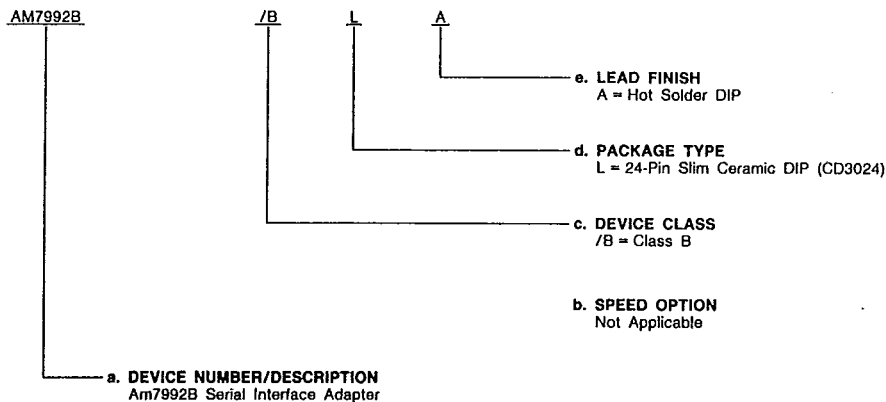
Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

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- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM7992B	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.