

E0C623E

4-bit Single Chip Microcomputer



- Core CPU Architecture
- SVD Circuit
- Sound Generator

DESCRIPTION

The E0C623E is a CMOS single-chip microcomputer composed of the 4-bit core CPU E0C6200A, ROM, RAM, LCD driver, time base counter, stopwatch timer, SVD circuit and sound generator. The E0C623E provides an excellent solution for low-power consumption systems with clock functions.

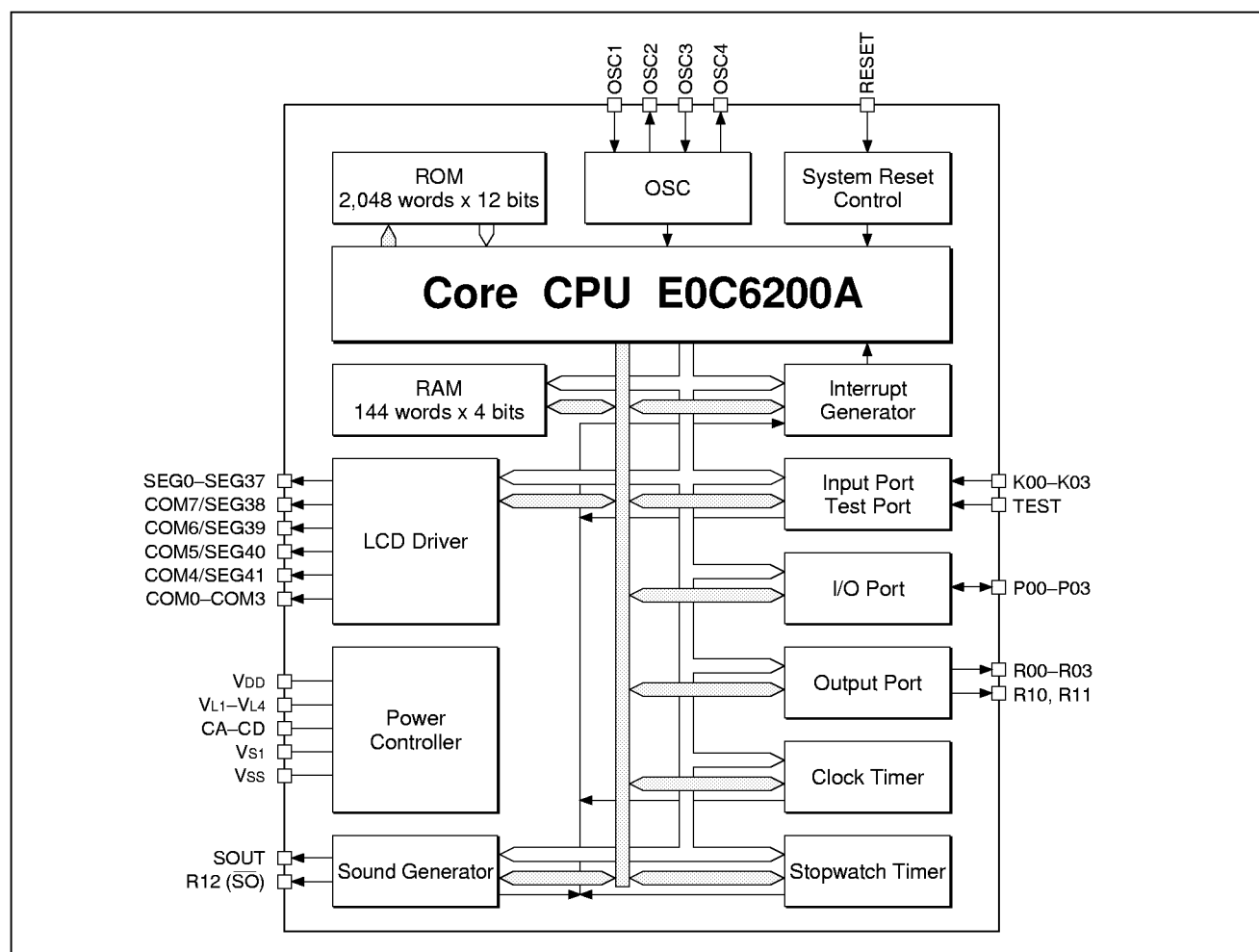
FEATURES

- CMOS LSI 4-bit parallel processing
- Clock 32.768kHz (Typ.) / 1MHz (Typ.)
- Instruction set 100 instructions
- Instruction execution time During operation at 32.768kHz : 153μsec, 214μsec, 366μsec
(depending on instruction) During operation at 1MHz : 5μsec, 7μsec, 12μsec
- ROM capacity 2,048 words × 12 bits
- RAM capacity 144 words × 4 bits
- Input port 4 bits (pull down resistors are available by mask option)
- Output port 5 bits (general purpose output)
1 bit (sound output)
1 bit (sound reverse or general purpose output)
1 bit (clock or general purpose output)
The clock frequency can be selected from OSC3 or 256Hz to 32kHz by mask option.
- I/O port 4 bits
- LCD driver 42 segments × 4 commons / 38 segments × 8 commons
(switching between 1/4 duty and 1/8 duty is available by mask option)
- Sound generator 8 programmable sounds
- Built-in stopwatch timer
- Built-in supply voltage detection (SVD) circuit
- Interrupt External : Input interrupt 2 systems
Internal : Timer interrupt 2 systems
- Current consumption E0C623E HALT mode (32kHz) : 1.5μA (Typ.)
OPERATING mode (32kHz) : 4.0μA (Typ.)
E0C62L3E HALT mode (32kHz) : 1.5μA (Typ.)
OPERATING mode (32kHz) : 4.0μA (Typ.)
E0C62A3E OPERATING mode (1MHz) : 150μA (Typ.)
- Package QFP5-80pin (plastic), QFP14-80pin (plastic)
Die form

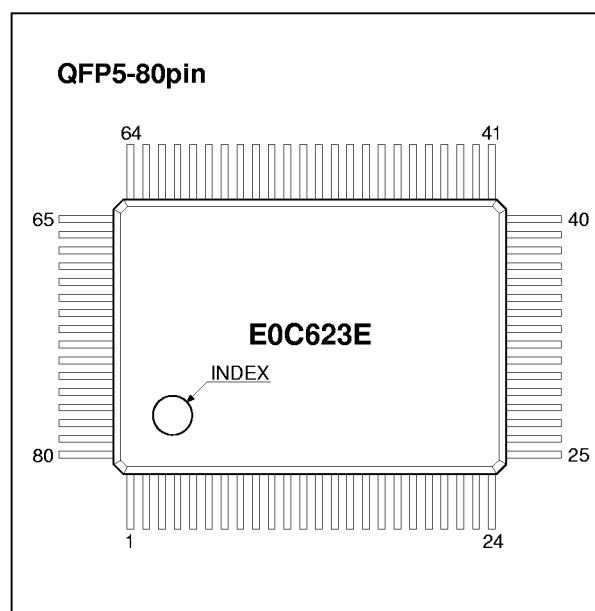
LINE UP

Model	Supply voltage	Clock (oscillation)
E0C62L3E	1.5V (1.1V to 3.5V)	32kHz (Crystal or CR)
E0C623E	3.0V (2.2V to 5.5V)	32kHz (Crystal or CR)
E0C62A3E	3.0V (2.2V to 5.5V)	32kHz (Crystal or CR) & 1MHz (Ceramic or CR)

■ BLOCK DIAGRAM

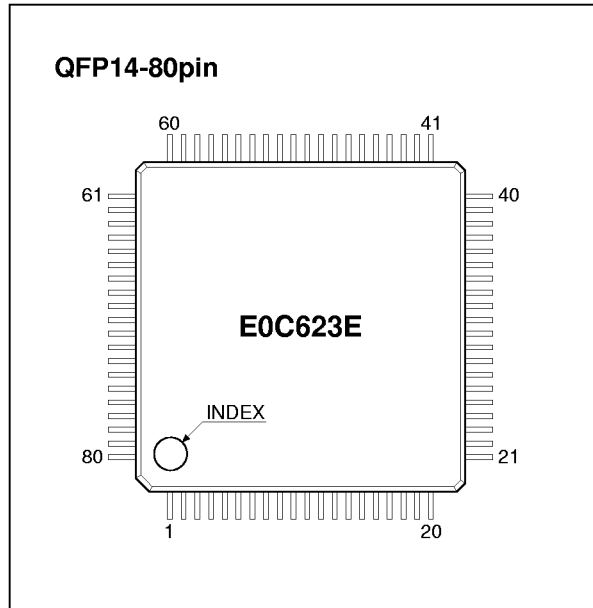


■ PIN CONFIGURATION



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG25	21	COM0	41	R10	61	SEG6
2	SEG26	22	CD	42	R11	62	N.C.
3	SEG27	23	CC	43	R12	63	SEG7
4	SEG28	24	CB	44	SOUT	64	SEG8
5	SEG29	25	CA	45	R00	65	SEG9
6	SEG30	26	VL4	46	R01	66	SEG10
7	SEG31	27	VL3	47	R02	67	SEG11
8	SEG32	28	VL2	48	R03	68	SEG12
9	SEG33	29	VL1	49	K00	69	SEG13
10	SEG34	30	VSS	50	K01	70	SEG14
11	SEG35	31	OSC4	51	K02	71	SEG15
12	SEG36	32	OSC3	52	K03	72	SEG16
13	SEG37	33	Vs1	53	TEST	73	SEG17
14	SEG38/COM7	34	OSC2	54	RESET	74	SEG18
15	SEG39/COM6	35	OSC1	55	SEG0	75	SEG19
16	SEG40/COM5	36	VDD	56	SEG1	76	SEG20
17	SEG41/COM4	37	P00	57	SEG2	77	SEG21
18	COM3	38	P01	58	SEG3	78	SEG22
19	COM2	39	P02	59	SEG4	79	SEG23
20	COM1	40	P03	60	SEG5	80	SEG24

N.C. : No Connection



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG27	21	CC	41	R11	61	SEG7
2	SEG28	22	CB	42	R12	62	SEG8
3	SEG29	23	CA	43	SOUT	63	SEG9
4	SEG30	24	VL4	44	R00	64	SEG10
5	SEG31	25	VL3	45	R01	65	SEG11
6	SEG32	26	VL2	46	R02	66	SEG12
7	SEG33	27	VL1	47	R03	67	SEG13
8	SEG34	28	Vss	48	K00	68	SEG14
9	SEG35	29	OSC4	49	K01	69	SEG15
10	SEG36	30	OSC3	50	K02	70	SEG16
11	SEG37	31	Vs1	51	K03	71	SEG17
12	SEG38/COM7	32	OSC2	52	TEST	72	SEG18
13	SEG39/COM6	33	OSC1	53	RESET	73	SEG19
14	SEG40/COM5	34	VDD	54	SEG0	74	SEG20
15	SEG41/COM4	35	P00	55	SEG1	75	SEG21
16	COM3	36	P01	56	SEG2	76	SEG22
17	COM2	37	P02	57	SEG3	77	SEG23
18	COM1	38	P03	58	SEG4	78	SEG24
19	COM0	39	R10	59	SEG5	79	SEG25
20	CD	40	N.C.	60	SEG6	80	SEG26

N.C. : No Connection

PIN DESCRIPTION

Pin name	Pin No.		I/O	Function
	QFP5	QFP14		
VDD	36	34	(I)	Power source (+) pin
Vss	30	28	(I)	Power source (–) pin
Vs1	33	31	—	Internal logic and oscillation system regulated voltage power source pin
VL1–VL4	29–26	27–24	—	LCD system power source pins
CA–CD	25–22	23–20	—	LCD system booster capacitor connection pins
OSC1	35	33	I	Crystal or CR oscillation input pin
OSC2	34	32	O	Crystal or CR oscillation output pin
OSC3	32	30	I	Ceramic or CR oscillation input pin (E0C62A3E)
OSC4	31	29	O	Ceramic or CR oscillation output pin (E0C62A3E)
K00–K03	49–52	48–51	I	Input port pins
P00–P03	37–40	35–38	I/O	I/O port pins
R00–R03	45–48	44–47	O	Output port pins
R10	41	39		R10: FOUT output available through mask option selection
R11	42	41		R12: Sound inverted output available through mask option selection
R12	43	42		
SOUT	44	43	O	Sound signal output pin
SEG0–SEG37	1–13 55–80	54–80 1–11	O	LCD segment output pins
COM0–COM3	21–18	19–16	O	LCD common output pins
SEG38–SEG41	14–17	12–15	O	LCD segment output pins (when 1/4 duty is selected)
COM4–COM7				LCD common output pins (when 1/8 duty is selected)
RESET	54	53	I	Initial reset input pin
TEST	53	52	I	Test input pin

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V _{SS}	-6.0 to 0.5	V
Input voltage (1)	V _I	V _{SS} - 0.3 to 0.5	V
Input voltage (2)	V _I OSC	V _{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI _{VSS}	10	mA
Operating temperature	T _{opr}	-20 to 70	°C
Storage temperature	T _{stg}	-65 to 150	°C
Soldering temperature / Time	T _{sol}	260°C, 10sec (lead section)	—
Allowable dissipation *2	P _D	250	mW

*1 The permissible total output current is the sum total of the current that simultaneously flows from the output pins (or is drawn in).

*2 In case of plastic package (QFP5-80pin, LQFP14-80pin).

● Recommended Operating Conditions

E0C623E

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-5.5	-3.0	-2.2	V
Oscillation frequency	f _{OSC1}		20	32.768	50	kHz

E0C62L3E

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-3.5	-1.5	-1.1	V
		V _{DD} =0V, with software control *1	-3.5	-1.5	-0.9 *2	V
Oscillation frequency	f _{OSC1}		20	32.768	50	kHz

*1 When switching to the heavy load protection mode. The SVD circuit is turned OFF.

*2 The voltage which can be displayed on the LCD panel will differ according to the characteristics of the LCD panel.

E0C62A3E

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V _{SS}	V _{DD} =0V	-5.5	-3.0	-2.2	V
Oscillation frequency	f _{OSC1}		—	32.768	—	kHz
	f _{OSC3}	Duty 50±5%	300	1,000	1,200	kHz

● DC Characteristics

E0C623E/62A3E

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}~V_{L4} are internal voltage, C₁~C₈=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00~K03, P00~P03	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	RESET, TEST	0.10•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00~K03, P00~P03	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	RESET, TEST	V _{SS}		0.90•V _{SS}	V
High level input current (1)	I _{IH1}	V _{IH1} =0V, No pull down resistor	0		0.5	μA
High level input current (2)	I _{IH2}	V _{IH2} =0V, With pull down resistor	5		16	μA
High level input current (3)	I _{IH3}	V _{IH3} =0V, With pull down resistor	30		100	μA
Low level input current	I _{IL}	V _{IL} =V _{SS}	-0.5		0	μA
High level output current	I _{OH1}	V _{OH1} =0.1•V _{SS}			-1.0	mA
Low level output current	I _{OL1}	V _{OL1} =0.9•V _{SS}	3.0			mA
Common output current 1/4 duty	I _{OH2}	V _{OH2} =-0.05V			-3	μA
	I _{OL2}	V _{OL2} =V _{L3} +0.05V	3			μA
Segment output current (LCD output) 1/4 duty	I _{OH3}	V _{OH3} =-0.05V			-3	μA
	I _{OL3}	V _{OL3} =V _{L3} +0.05V	3			μA
Common output current 1/8 duty	I _{OH4}	V _{OH4} =-0.05V			-3	μA
	I _{OL4}	V _{OL4} =V _{L4} +0.05V	3			μA
Segment output current (LCD output) 1/8 duty	I _{OH5}	V _{OH5} =-0.05V			-3	μA
	I _{OL5}	V _{OL5} =V _{L4} +0.05V	3			μA

E0C62L3E

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, T_a=25°C, V_{S1}/V_{L1}–V_{L4} are internal voltage, C₁–C₈=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V _{IH1}	K00–K03, P00–P03	0.2•V _{SS}		0	V
High level input voltage (2)	V _{IH2}	RESET, TEST	0.10•V _{SS}		0	V
Low level input voltage (1)	V _{IL1}	K00–K03, P00–P03	V _{SS}		0.8•V _{SS}	V
Low level input voltage (2)	V _{IL2}	RESET, TEST	V _{SS}		0.90•V _{SS}	V
High level input current (1)	I _{IH1}	V _{IH1} =0V, No pull down resistor	0		0.5	μA
High level input current (2)	I _{IH2}	V _{IH2} =0V, With pull down resistor	2.0		10	μA
High level input current (3)	I _{IH3}	V _{IH3} =0V, With pull down resistor	9.0		60	μA
Low level input current	I _{IL}	V _{IL} =V _{SS}	-0.5		0	μA
High level output current	I _{OH1}	V _{OH1} =0.1•V _{SS}			-200	μA
Low level output current	I _{OL1}	V _{OL1} =0.9•V _{SS}	700			μA
Common output current 1/4 duty	I _{OH2}	V _{OH2} =-0.05V			-3	μA
	I _{OL2}	V _{OL2} =V _{L3} +0.05V	3			μA
Segment output current (LCD output) 1/4 duty	I _{OH3}	V _{OH3} =-0.05V			-3	μA
	I _{OL3}	V _{OL3} =V _{L3} +0.05V	3			μA
Common output current 1/8 duty	I _{OH4}	V _{OH4} =-0.05V			-3	μA
	I _{OL4}	V _{OL4} =V _{L4} +0.05V	3			μA
Segment output current (LCD output) 1/8 duty	I _{OH5}	V _{OH5} =-0.05V			-3	μA
	I _{OL5}	V _{OL5} =V _{L4} +0.05V	3			μA

● Analog Circuit Characteristics and Current Consumption

E0C623E

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, C_G=25pF, T_a=25°C, V_{S1}/V_{L1}–V_{L4} are internal voltage, C₁–C₈=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (no panel load)	0.5•V _{L2} -0.1		0.5•V _{L2} +0.1	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (no panel load)	-2.25	-2.10	-1.95	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (no panel load)	3•V _{L1} -0.1		3•V _{L1} +0.9	V
	V _{L4}	Connect 1MΩ load resistor between V _{DD} and V _{L4} (no panel load)	4•V _{L1} -0.1		4•V _{L1} +0.9	V
SVD voltage	V _{SVD}		-2.55	-2.40	-2.25	V
SVD circuit response time	t _{SVD}				100	μS
Power current consumption (Normal mode)	I _{OP1}	During HALT *1	No panel load	1.5	3.0	μA
		During execution *1	OSC1: Crystal oscillation	4.0	7.0	μA
	I _{OP2}	During HALT *1	No panel load	6.0	10.5	μA
		During execution *1	OSC1: CR oscillation	8.7	14.0	μA
Power current consumption (Heavy load protection mode)	I _{OP1}	During HALT *1	No panel load	11.5	33.0	μA
		During execution *1	OSC1: Crystal oscillation	14.0	37.0	μA
	I _{OP2}	During HALT *1	No panel load	16.0	40.5	μA
		During execution *1	OSC1: CR oscillation	18.7	44.0	μA

*1 The SVD circuit is OFF status.

E0C62L3E

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, C_G=25pF, T_a=25°C, V_{S1}/V_{L1}–V_{L4} are internal voltage, C₁–C₈=0.1μF)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V _{L1}	Connect 1MΩ load resistor between V _{DD} and V _{L1} (no panel load)	-1.15	-1.05	-0.95	V
	V _{L2}	Connect 1MΩ load resistor between V _{DD} and V _{L2} (no panel load)	2•V _{L1} -0.1		2•V _{L1} +0.9	V
	V _{L3}	Connect 1MΩ load resistor between V _{DD} and V _{L3} (no panel load)	3•V _{L1} -0.1		3•V _{L1} +0.9	V
	V _{L4}	Connect 1MΩ load resistor between V _{DD} and V _{L4} (no panel load)	4•V _{L1} -0.1		4•V _{L1} +0.9	V
SVD voltage	V _{SVD}		-1.30	-1.20	-1.10	V
SVD circuit response time	t _{SVD}				100	μS
Power current consumption (Normal mode)	I _{OP1}	During HALT *1	No panel load	1.5	3.0	μA
		During execution *1	OSC1: Crystal oscillation	4.0	7.0	μA
	I _{OP2}	During HALT *1	No panel load	6.0	10.5	μA
		During execution *1	OSC1: CR oscillation	8.7	14.0	μA
Power current consumption (Heavy load protection mode)	I _{OP1}	During HALT *1	No panel load	2.5	6.0	μA
		During execution *1	OSC1: Crystal oscillation	7.0	12.0	μA
	I _{OP2}	During HALT *1	No panel load	11.5	20.5	μA
		During execution *1	OSC1: CR oscillation	16.5	27.0	μA

*1 The SVD circuit is OFF status.

E0C62A3E

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $f_{OSC1}=32.768kHz$, $C_G=25pF$, $T_a=25^{\circ}C$, $V_{S1}/V_{L1}-V_{L4}$ are internal voltage, $C_1-C_8=0.1\mu F$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
LCD drive voltage	V_{L1}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L1} (no panel load)	$0.5 \cdot V_{L2} - 0.1$		$0.5 \cdot V_{L2} + 0.1$	V
	V_{L2}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L2} (no panel load)	-2.25	-2.10	-1.95	V
	V_{L3}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L3} (no panel load)	$3 \cdot V_{L1} - 0.1$		$3 \cdot V_{L1} \times 0.9$	V
	V_{L4}	Connect $1M\Omega$ load resistor between V_{DD} and V_{L4} (no panel load)	$4 \cdot V_{L1} - 0.1$		$4 \cdot V_{L1} \times 0.9$	V
SVD voltage	V_{SVD}		-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}				100	μS
Power current consumption (Normal mode)	IOP1	During HALT *1	No panel load	1.70	3.0	μA
		During execution (32kHz) *1	OSC1: Crystal oscillation	4.0	7.0	μA
	IOP2	During HALT *1	No panel load	30	60	μA
		During execution (32kHz) *1	OSC1: CR oscillation	30	60	μA
	IOP3	During execution (1MHz) *2	No panel load	180	360	μA
			OSC3: CR or ceramic oscillation			
Power current consumption (Heavy load protection mode)	IOP1	During HALT *1	No panel load	11.7	33.0	μA
		During execution (32kHz) *1	OSC1: Crystal oscillation	14.0	37.0	μA
	IOP2	During HALT *1	No panel load	40	90	μA
		During execution (32kHz) *1	OSC1: CR oscillation	40	90	μA
	IOP3	During execution (1MHz) *2	No panel load	300	420	μA
			OSC3: CR or ceramic oscillation			

*1 The OSC3 oscillation circuit and SVD circuit are OFF status.

*2 The SVD circuit is OFF status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C623E/62A3E (OSC1 crystal oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Crystal: C-002R ($C_1=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta}	(V_{SS}) $t_{sta} \leq 3sec$	-2.2			V
Oscillation stop voltage	V_{stp}	(V_{SS}) $t_{stp} \leq 10sec$	-2.2			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS} = -2.2$ to $-5.5V$			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G = 5$ to $25pF$	40			ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 terminal and V_{DD} , V_{SS}	200			$M\Omega$

E0C62L3E (OSC1 crystal oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, Crystal: C-002R ($C_1=35k\Omega$), $C_G=25pF$, C_D =built-in, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	V_{sta}	(V_{SS}) $t_{sta} \leq 3sec$	-1.1			V
Oscillation stop voltage	V_{stp}	(V_{SS}) $t_{stp} \leq 10sec$	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacitance inside the IC		20		pF
Frequency/voltage deviation	$\partial f/\partial V$	$V_{SS} = -1.1$ to $-3.5V$ (-0.9V)*1			5	ppm
Frequency/IC deviation	$\partial f/\partial IC$		-10		10	ppm
Frequency adjustment range	$\partial f/\partial C_G$	$C_G = 5$ to $25pF$	40			ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.5	V
Permitted leak resistance	R_{leak}	Between OSC1 terminal and V_{DD} , V_{SS}	200			$M\Omega$

*1 Items enclosed in parentheses () are those used when operating in the heavy load protection mode.

E0C623E/62A3E (OSC1 CR oscillation circuit)

(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=850k\Omega$, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC1}		-30	32.768kHz	30	%
Oscillation start voltage	V_{sta}		-2.2			V
Oscillation start time	t_{sta}	$V_{SS}=-2.2$ to $-5.5V$		3		mS
Oscillation stop voltage	V_{stp}		-2.2			V

E0C62L3E (OSC1 CR oscillation circuit)(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-1.5V$, $R_{CR}=850k\Omega$, $T_a=25^{\circ}C$)

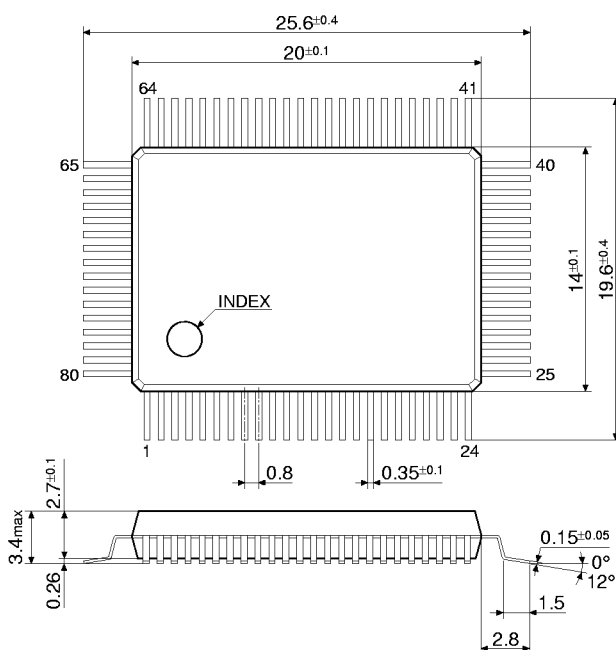
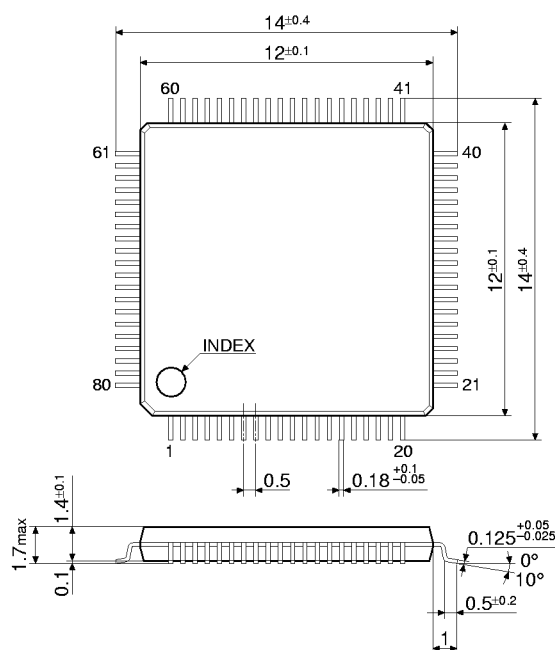
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc1		-30	32.768kHz	30	%
Oscillation start voltage	Vsta		-0.9			V
Oscillation start time	tsta	$V_{SS}=-0.9$ to $-3.5V$		3		mS
Oscillation stop voltage	Vstp		-0.9			V

E0C62A3E (OSC3 CR oscillation circuit)(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, $R_{CR}=35k\Omega$, $T_a=25^{\circ}C$)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	fosc3		-30	1MHz	30	%
Oscillation start voltage	Vsta		-2.2			V
Oscillation start time	tsta	$V_{SS}=-2.2$ to $-5.5V$			3	mS
Oscillation stop voltage	Vstp		-2.2			V

E0C62A3E (OSC3 ceramic oscillation circuit)(Unless otherwise specified: $V_{DD}=0V$, $V_{SS}=-3.0V$, Ceramic oscillator: 1MHz, $C_{GC}=C_{DC}=100pF$, $T_a=25^{\circ}C$)

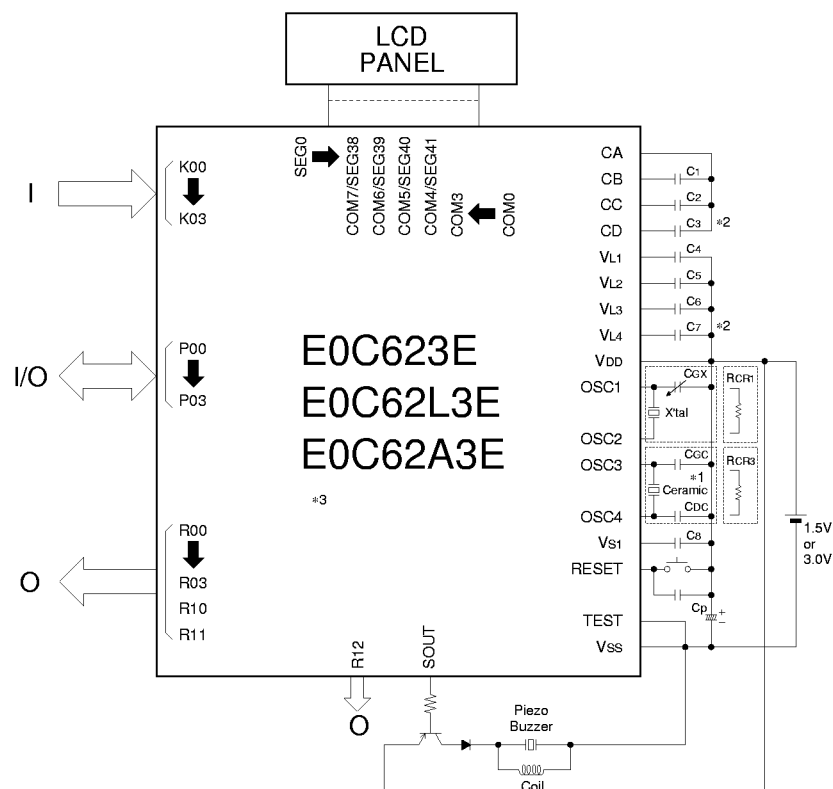
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta		-2.2			V
Oscillation start time	tsta	$V_{SS}=-2.2$ to $-5.5V$			5	mS
Oscillation stop voltage	Vstp		-2.2			V

■ PACKAGE DIMENSIONS**Plastic QFP5-80pin****Plastic QFP14-80pin**

Unit: mm

■ BASIC EXTERNAL CONNECTION DIAGRAM

Piezo Buzzer Single Terminal Driving (Piezo buzzer driving through PNP transistor)



X'tal	Crystal oscillator	32.768kHz, Cl(Max.)=35kΩ
RCR1	CR oscillation resistor	850kΩ
Ceramic	Ceramic oscillator	1 MHz (Typ.)
RCR3	CR oscillation resistor	35kΩ
CGC, CDC	Capacitor	100pF
CGX	Trimmer capacitor	5–25pF
C1–C8	Capacitor	0.1μF
Cp	Capacitor	3.3μF

*1 OSC3 oscillation circuit can be used only for E0C62A3E.

For the E0C623E and 62L3E, do not connect anything to terminals OSC3 and OSC4.

*2 In case 1/4 duty was selected with the mask option, set CD and VL4 to N.C. (not connected). The C3 and C7 capacitor are not required.

*3 The potential of the substrate is VDD.