HT7630
DC PIR Controller

Features

- Operating voltage : 5V~12V
- Low standby current : <30μA
- On-chip regulator
- 40 seconds warm-up
- Low battery detector
- Two-stage OP amp
- Multi-function indicator
- 16-pin DIP/SOP package

Applications

- PIR motion detector
- Alarm system
- Door bell

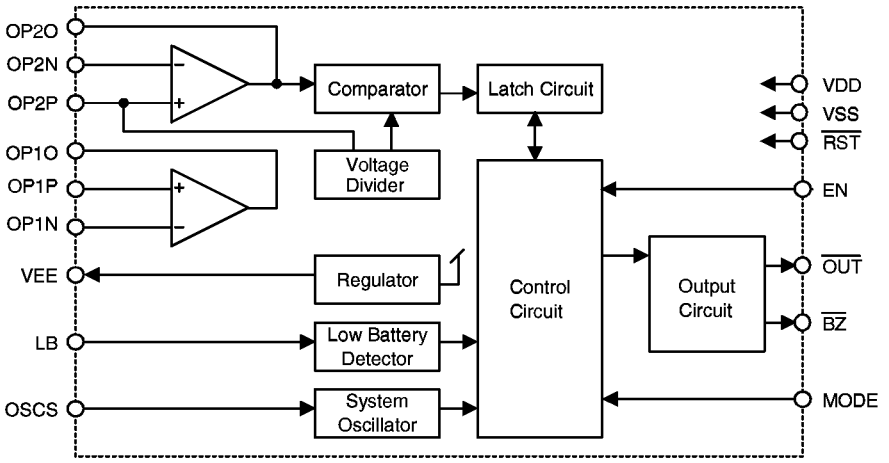
General Description

The HT7630 is a low power PIR controller LSI designed for battery powered door bell/alarm application. The chip contains operation amplifiers, comparators, a timer, a voltage regulator, an oscillator and control circuits.

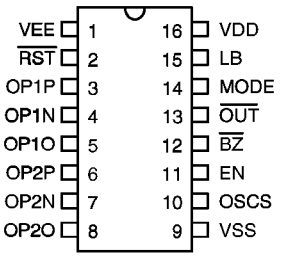
The chip amplifies the signal from a PIR (Pyroelectric Infrared) sensor to detect the motion of a human body. When the PIR output meets certain criteria (see functional description), the chip will output an active low signal to trigger a sound generator chip or another device. The output duration is 4 seconds for a door bell and 32 seconds for an alarm depending on the MODE pin selection.

It also provides an LB input pin for low battery detection during warm-up, a EN input pin for output enable/disable control and a $\overline{BZ}$ pin for status indication. An LED or piezo buzzer can be connected to the $\overline{BZ}$ pin to indicate the following: warm-up, triggering, alarm triggered memory and low battery. The IC is offered in a 16 pin DIP/SOP package.

Block Diagram



Pin Assignment



HT7630
– 16 DIP/SOP

Pin Description

Pin Name	I/O	Internal Connect	Description
VEE	O	NMOS	Internal voltage regulator output pin. The output voltage is -4V with respect to VDD.
$\overline{\text{RST}}$	I	CMOS	Chip reset input pin. Active low.
OP1P	I	PMOS	Noninverting input of OP1
OP1N	I	PMOS	Inverting input of OP1
OP1O	O	NMOS	OP1 output
OP2P	I	PMOS	Noninverting input of OP2. Internally biased to the comparator window center voltage.
OP2N	I	PMOS	Inverting input of OP2
OP2O	O	NMOS	OP2 output, connected to the internal comparator input.
VSS	—	—	Negative power supply
OSCS	I/O	—	System oscillator I/O pin. Connect an external RC to set the system frequency. The system frequency ≅ 8kHz for normal application.
EN	I	CMOS	Input pin for output enable/disable control. EN=VDD: Output enable EN=VSS: Output disable
$\overline{\text{BZ}}$	O	CMOS	Chip status indicator output pin. Drives an LED or piezo buzzer with various patterns for warm-up, triggering, trigger memory and low battery indication. Normal high. Active low.
$\overline{\text{OUT}}$	O	NMOS	Output pin for driving a sound generator chip or other device when triggered by a valid PIR signal. The output duration is 4 seconds or 32 seconds depending on the MODE pin selection. Normal open, active low.

Pin Name	I/O	Internal Connect	Description
MODE	I	CMOS	Operating mode selection pin. MODE=VDD: Door bell mode MODE=VSS: Alarm mode
LB	I	CMOS	Low battery level setting pin. Connect to VSS when not using this function.
VDD	—	—	Positive power supply

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 13V
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature ..... –50°C to 125°C
Operating Temperature ..... –25°C to 75°C

*Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Electrical Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	5	9	12	V
V_{EE}	Regulator Output Voltage	9V	V_{DD}–V_{EE}	3.5	4	4.5	V
I_{STB}	Standby Current	9V	No load, OSC off	—	20	30	μA
I_{DD}	Operating Current	9V	No load, OSC on	—	45	75	μA
V_{IH1}	MODE "H" Input Voltage	9V	V_{DD}–V_{EE}=4V	8	—	—	V
V_{IL1}	MODE "L" Input Voltage	9V	V_{DD}–V_{EE}=4V	—	—	6.6	V
I_{OH1}	$\overline{BZ}$ Source Current	9V	V_{OH}= 8.1V	–4.5	–7.5	—	mA
I_{OL1}	$\overline{BZ}$ Sink Current	9V	V_{OL}= 0.9V	6	12	—	mA
I_{OL2}	$\overline{OUT}$ Sink Current	9V		6	12	—	mA
V_{IH2}	EN "H" Input Voltage	—	—	0.8V_{DD}	—	—	V
V_{IL2}	EN "L" Input Voltage	—	—	—	—	0.2V_{DD}	V
F_{SYS}	System Oscillator Frequency	9V	R_S=910kΩ, C_S=100p	6.7	8	9.6	kHz
V_{REF}	Low Battery Detector Reference Voltage	9V	With respect to V_{DD}	–1.26	–1.45	–1.67	V
A_{VO}	OP Amp Open Loop Gain	9V	No load	60	80	—	dB
V_{OS}	OP Amp Input Offset Voltage	9V	No load	—	10	35	mV

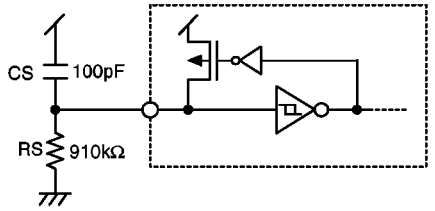
Functional Description

VEE

The VEE supplies power to the analog front end circuits with a stabilized voltage which is –4V with respect to VDD.

OSCS

This is the system oscillator input pin. Connect to an external RC to generate an 8kHz system frequency.



System oscillator

$\overline{OUT}$

This pin is an NMOS open drain structure. It stays open in standby and is active low when triggered by a valid PIR signal.

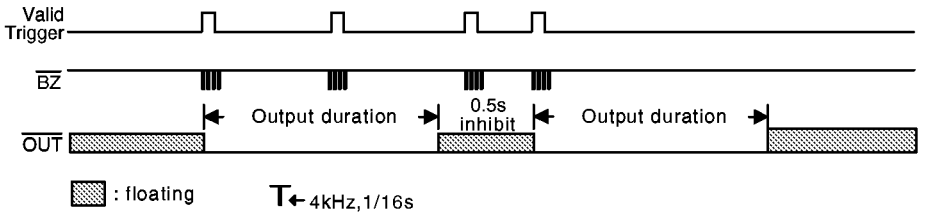
The output duration is 4 seconds for door bell application mode or 32 second (8, 16, 32 seconds selectable by mask option) for alarm application mode depending upon the MODE pin status. The output is nonretriggerable and has an inhibit duration of 0.5 seconds before the next output.

MODE

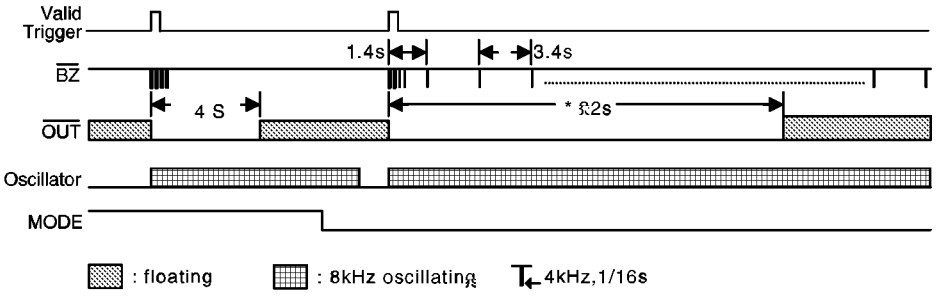
This pin is used to select the operating mode.

Mode Pin	Operating Mode	Output Duration	Trigger Memory
VDD	Door Bell	4s	No
VSS	Alarm	* 32s	Yes

* Note: The output duration in the alarm mode can be set to 8, 16 or 32 seconds by mask option.



Output timing



MODE status and output timing

EN

This pin is used to enable/disable $\overline{OUT}$, it is a CMOS input structure.

EN	$\overline{OUT}$
VSS	Disabled(Floating)
VDD	Enable

$\overline{BZ}$

This is a multi-function chip status indicator output. It can drive an LED or piezo buzzer to show the chip status. The chip status includes warm-up, triggering, trigger memory and low battery which are shown with various patterns.

Warm-up

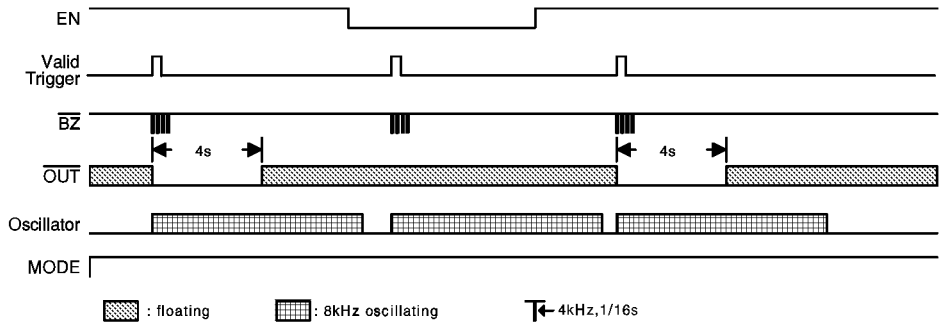
After power-on, the chip waits for 40 seconds for the PIR amplifier to stabilize, during which time the $\overline{BZ}$ output signal behaves as follows.

Low battery

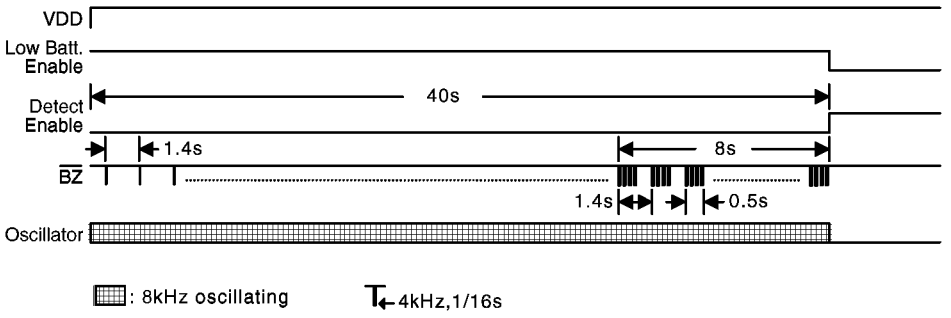
The chip performs low battery detection during the 40 second warm-up period. If a low battery signal is detected, the $\overline{BZ}$ output sounds eight times and then the system halts.

Triggering

The $\overline{BZ}$ pin output sounds four times every time the chip receives a valid PIR trigger signal.



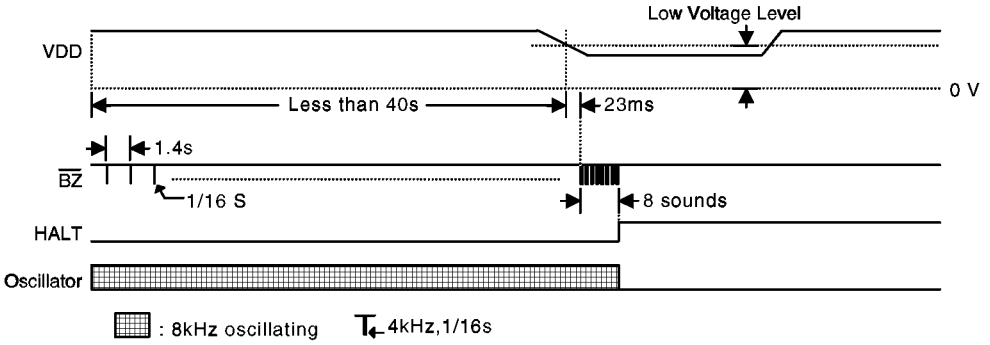
EN and output timing



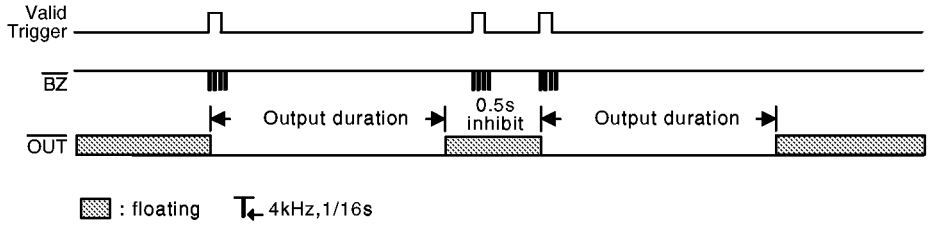
Warm-up timing

Trigger memory

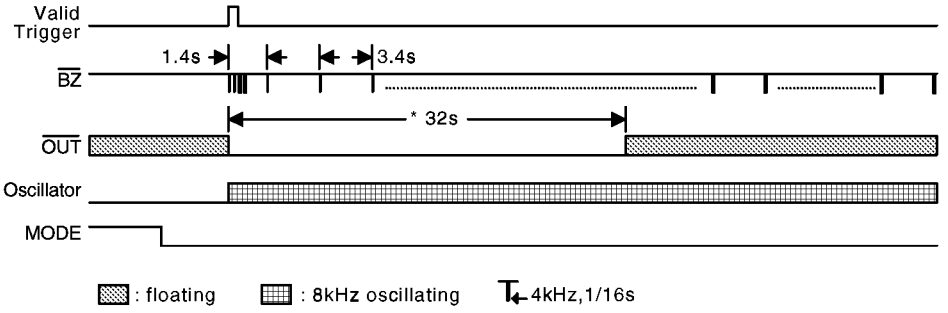
$\overline{BZ}$ will keep flashing at a 0.3Hz rate after a valid trigger, to show that a trigger has been received. This function is provided for alarm mode only.



Low battery detection timing



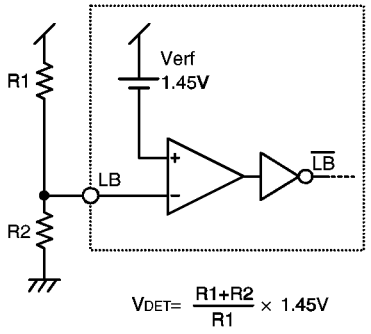
Triggering output timing



Trigger memory output timing

LB

This pin is used to set the low battery detection level.



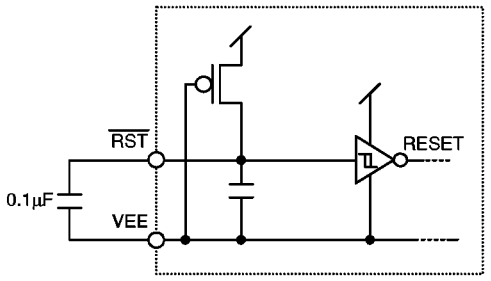
Low battery circuit

The internal reference voltage is 1.45V±15% and the defect voltage is set externally with the R1, R2 voltage divider.

The value of R1+R2 should be kept high enough to ensure low current consumption.

$\overline{\text{RST}}$

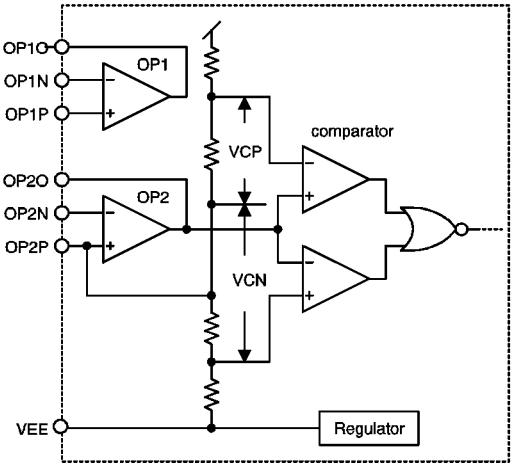
This is the active low system reset pin. The V_{IL} of this pin is about $\frac{1}{2}$ (VDD–VEE).



Reset circuit

PIR Amplifier

Consult the diagram below for details of the PIR front end amplifier.



PIR amplifier block diagram

In the figure there are two op-amps with different applications. OP1 can be used independently as a first stage inverting or noninverting amplifier for the PIR.

As the output of OP2 is directly connected to the input of the comparator it is used as a second stage amplifying device.

The noninverting input of OP2 is connected to the comparator's window centerpoint and can be used to check this voltage and to provide a bias voltage that is equal to the centerpoint voltage of the comparator.

In the figure, the comparator can have three window levels set by mask options.

1. $\frac{1}{16}$ (VDD–VEE), 2. $\frac{1}{11.3}$ (VDD–VEE), 3. $\frac{1}{9}$ (VDD–VEE). If not specified the default window will be set to $\frac{1}{16}$ (VDD–VEE). The preset voltage for VDD–VEE is 4V, the V_{CP} and V_{CN} default value is therefore 0.25V, ($\frac{4}{16}$).

Second Stage Amplifier

Usually the second stage PIR amplifier is a simple capacitively coupled inverting amplifier with low pass configuration. The noninverting input terminal is biased to the center point of the comparator window and the output of the second stage amplifier is directly coupled to the comparator center point.

In the figure, OP2P is directly connected to the comparator window center and with the C3 filter can act as the bias for OP2. For this configuration:

Voltage gain

$$Av = \frac{R2}{R1}$$

low cut off frequency

$$f_L = \frac{1}{2\pi R1C1}$$

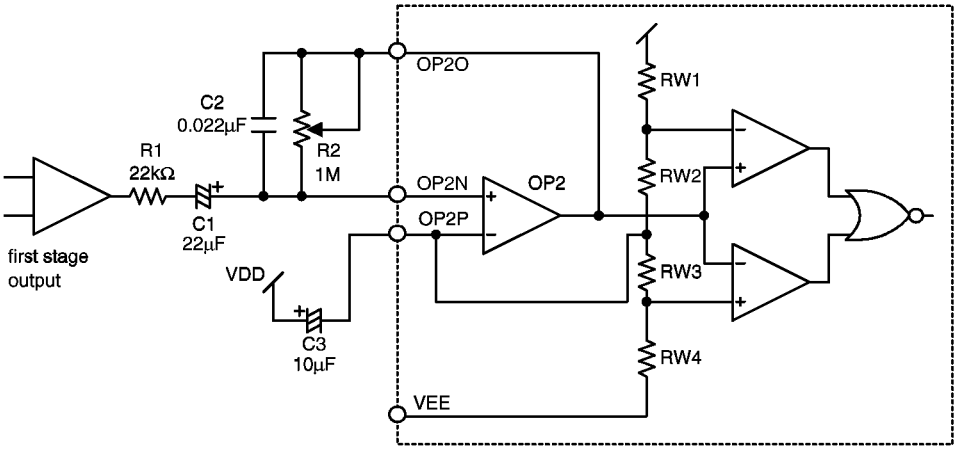
high cut off frequency

$$f_H = \frac{1}{2\pi R2C2}$$

By changing the value of R2, the sensitivity can be varied. C1 and C3 must be low leakage types to prevent the DC operating point from changing due to current leakage.

Each op-amp current consumption is approx. 5μA with all of the op-amps and comparator's working voltage provided by the regulator.

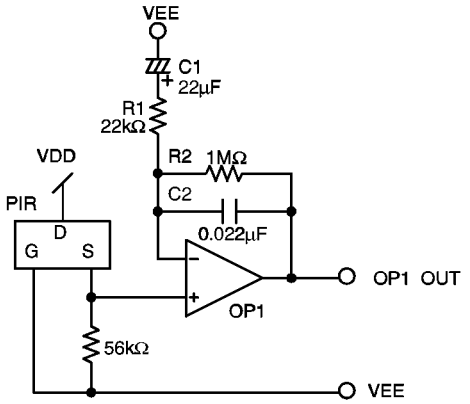
Consult the following diagrams for typical PIR front end circuits.



Typical second stage amplifier

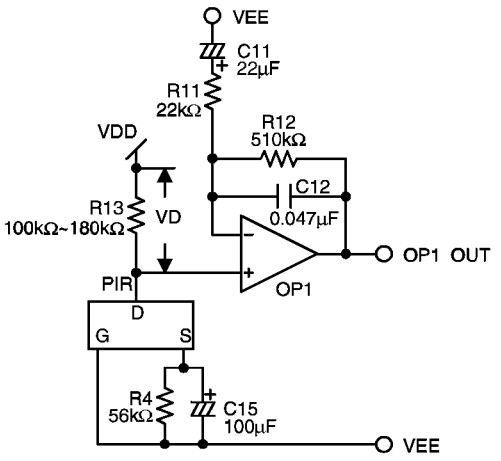
First Stage of PIR Amplifier

The figure shows a typical first stage amplifier. C2 and R2 form a simple low pass filter with cut off frequency of 7Hz. The low frequency response will be governed by R1 and C1 with cut-off frequency at 0.33Hz.



Typical PIR amplifier

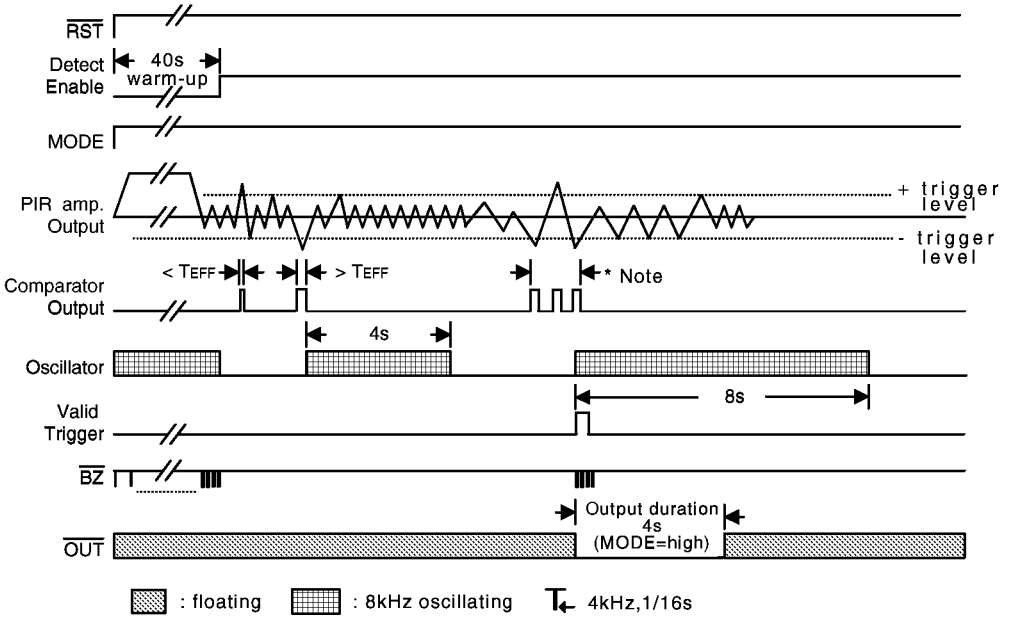
$$Av = \frac{(R1+R2)}{R1}$$



High gain first stage

The two figures are similar but in the second figure, the amplifier's input signal is taken from the drain of the PIR. This has higher gain than the previous figure. Since OP1 has PMOS inputs, V_D must be greater than 1.2V for adequate operation.

Trigger Timings



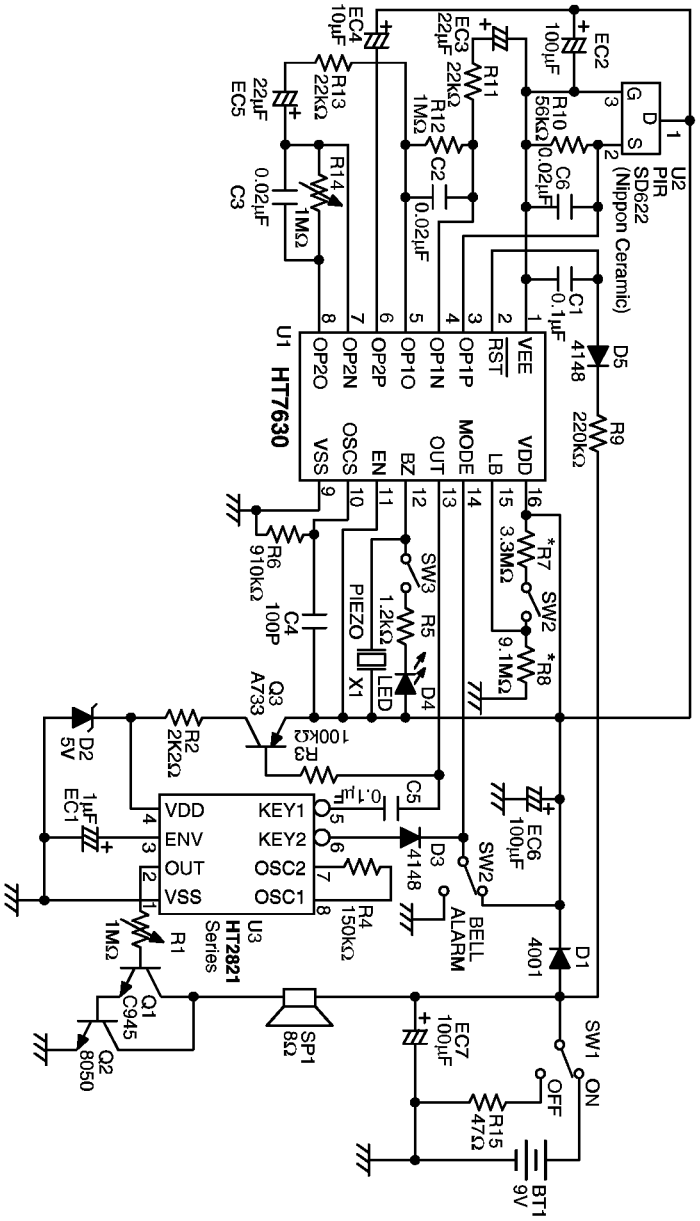
Note: The effective comparator output width (T_{EFF}) can be selected as either 24, 32 or 48ms by mask option. The default is 24ms.

T_{OUT}=4s (F_{SYS}=8kHz) when MODE=VDD. Nonretriggerable.

The $\overline{OUT}$ will be activated if the comparator output meets the following criteria:
A trigger signal with a sustained duration ≥ 0.34s
More than three effective trigger signal within 2s
Two effective trigger signals within 2s with one trigger signal sustained for ≥ 0.16s

The above timing is valid under F_{SYS}=8kHz.

Application Circuits



*Note: Adjust R7, R8 to set to low battery detection level