



3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCHR162601

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCHR162601:

- Balanced Output Drivers: $\pm 12\text{mA}$
- Low switching noise

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal

CMOS technology. The transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

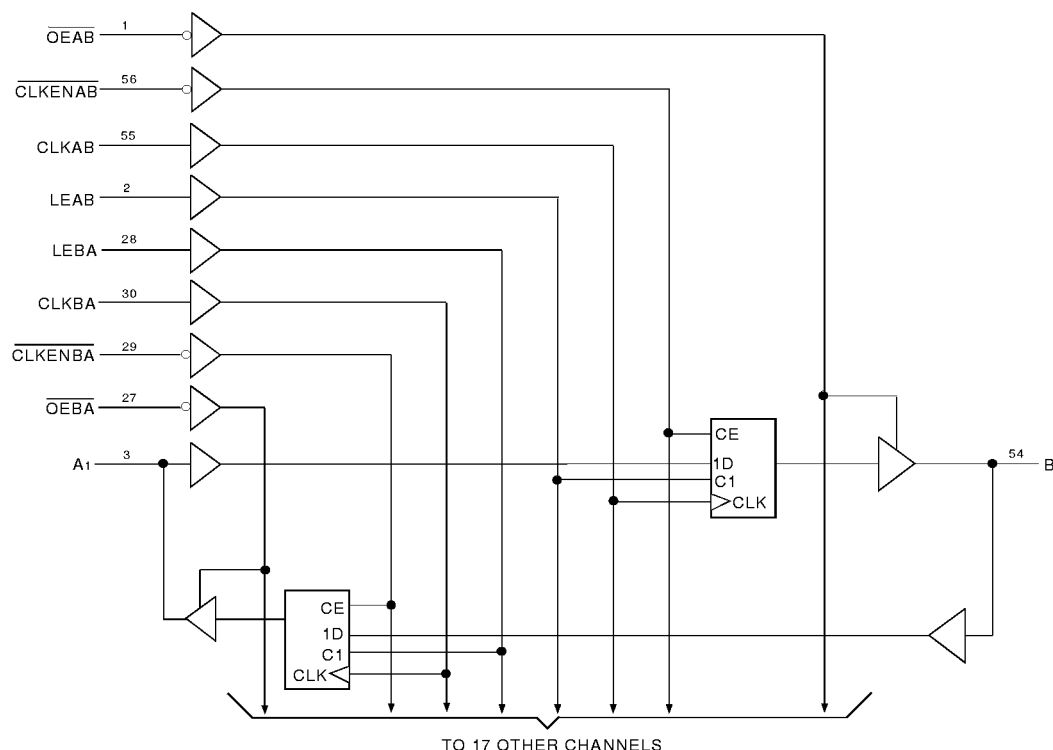
Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. Output enable $\overline{\text{OEAB}}$ is active low. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, CLKBA and $\overline{\text{CLKENBA}}$.

The ALVCHR162601 has series resistors in the device output structure which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels.

The ALVCHR162601 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

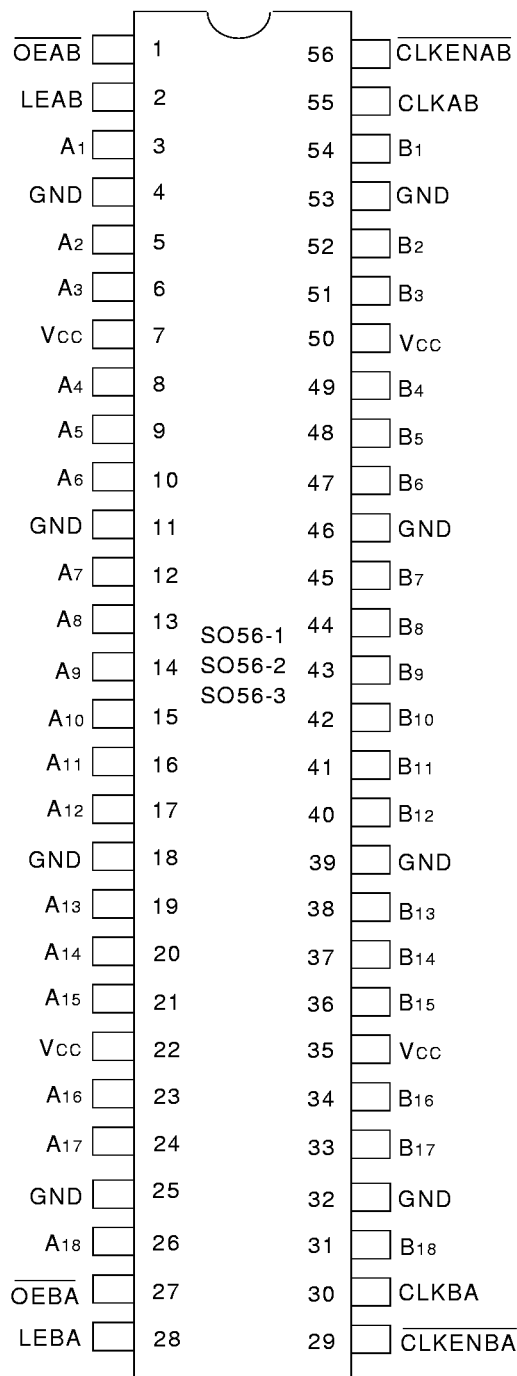
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

MARCH 1999

PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to V _{CC} + 0.5	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _I > V _{CC}	± 50	mA
I _{OK}	Continuous Clamp Current, V _O < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE^(1,2)

Inputs					Outputs
CLKENAB	OEAB	LEAB	CLKAB	A _x	B _x
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L or H	X	B ₀

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, CLKBA and CLKENBA.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
B₀ = Output level before the indicated steady-state input conditions were established.

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Inputs (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Inputs (Active LOW)
LEAB	A-to-B Latch Enable Inputs
LEBA	B-to-A Latch Enable Inputs
CLKAB	A-to-B Clock Inputs
CLKBA	B-to-A Clock Inputs
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾
$\overline{CLKENAB}$	A-to-B Clock Enable Inputs (Active LOW)
$\overline{CLKENBA}$	B-to-A Clock Enable Inputs (Active LOW)

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
			$V_O = \text{GND}$	—	—	± 10	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	

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NOTE:

- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^\circ\text{C}$ ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 3.0\text{V}$	$V_I = 2.0\text{V}$	-75	—	—	μA
			$V_I = 0.8\text{V}$	75	—	—	
I_{BHH} I_{BHL}	Bus-Hold Input Sustain Current	$V_{CC} = 2.3\text{V}$	$V_I = 1.7\text{V}$	-45	—	—	μA
			$V_I = 0.7\text{V}$	45	—	—	
I_{BHHO} I_{BHLO}	Bus-Hold Input Overdrive Current	$V_{CC} = 3.6\text{V}$	$V_I = 0$ to 3.6V	—	—	± 500	μA

NOTES:

- Pins with Bus-hold are identified in the pin description.
- Typical values are at $V_{CC} = 3.3\text{V}$, $+25^\circ\text{C}$ ambient.

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OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -4mA	1.9	—	
			I _{OH} = -6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = -4mA	2.2	—	
			I _{OH} = -8mA	2	—	
		V _{CC} = 3.0V	I _{OH} = -6mA	2.4	—	
			I _{OH} = -12mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		V _{CC} = 3.0V	I _{OL} = 6mA	—	0.55	
			I _{OL} = 12mA	—	0.8	

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NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	C _L = 0pF, f = 10Mhz	56	63	pF
CPD	Power Dissipation Capacitance Outputs disabled		12	13	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Bx to Ax	1	4.8	—	5.1	1	4.4	ns
t _{PLH} t _{PHL}	Propagation Delay LEAB to Bx or LEBA to Ax	1	5.5	—	5.8	1	5.1	ns
t _{PLH} t _{PHL}	Propagation Delay CLKAB to Bx or CLKBA to Ax	1.2	5.9	—	6.3	1.4	5.4	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax	1.1	6.3	—	6.6	1.1	5.6	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{OEAB}$ to Bx or $\overline{OEBA}$ to Ax	1	4.2	—	5.1	1.6	4.7	ns
t _{SU}	Setup Time, data before CLK↑	2.3	—	2.4	—	2.1	—	ns
t _{SU}	Setup Time, data before LE↓, CLK HIGH	2	—	1.6	—	1.6	—	ns
t _{SU}	Setup Time, data before LE↓, CLK LOW	1.3	—	1.2	—	1.1	—	ns
t _{SU}	Setup Time, $\overline{CLKEN}$ before CLK↑	2	—	2	—	1.7	—	ns
t _H	Hold Time, data after CLK↑	0.7	—	0.7	—	0.8	—	ns
t _H	Hold Time, data after LE↓, CLK HIGH	1.3	—	1.6	—	1.4	—	ns
t _H	Hold Time, data after LE↓, CLK LOW	1.7	—	2	—	1.7	—	ns
t _H	Hold Time, $\overline{CLKEN}$ after CLK↑	0.3	—	0.5	—	0.6	—	ns
t _W	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
t _W	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{SK(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

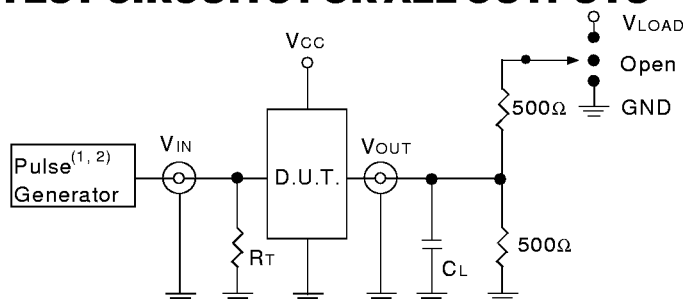
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.
R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

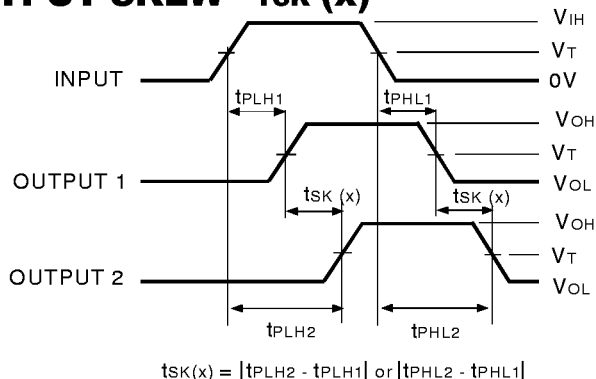
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



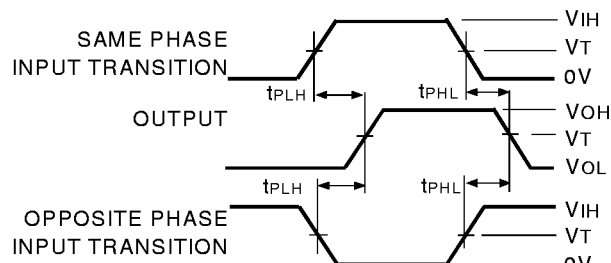
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

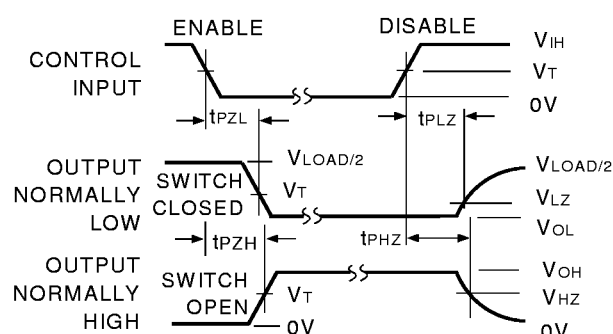
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

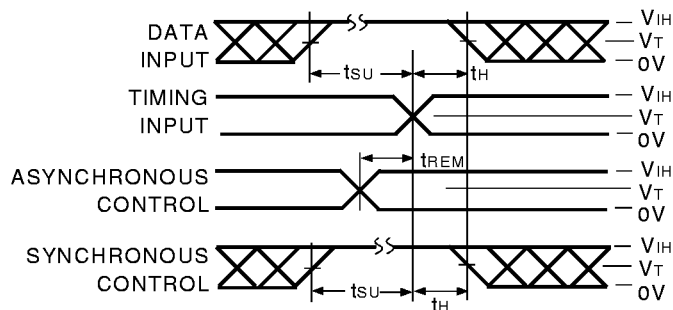


ALVC Link

NOTE:

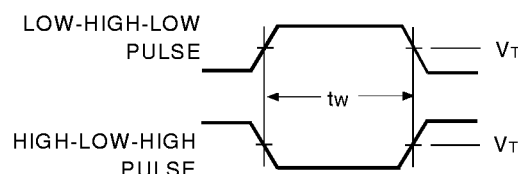
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					601		18-Bit Universal Bus Transceiver with 3-State Outputs
				R162			Double-Density with Resistors, $\pm 12\text{mA}$
			H				Bus-Hold
						74	-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

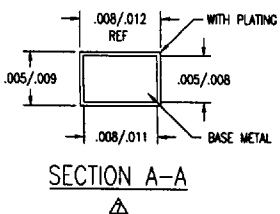
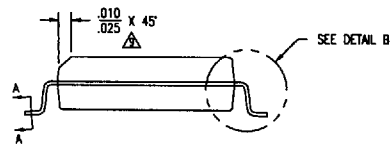
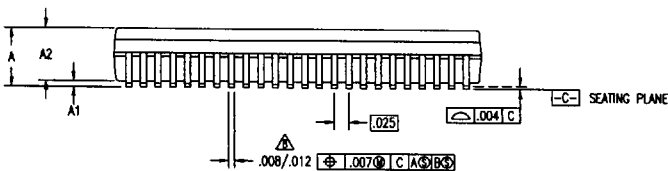
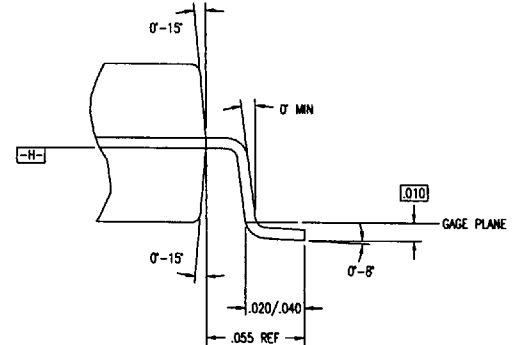
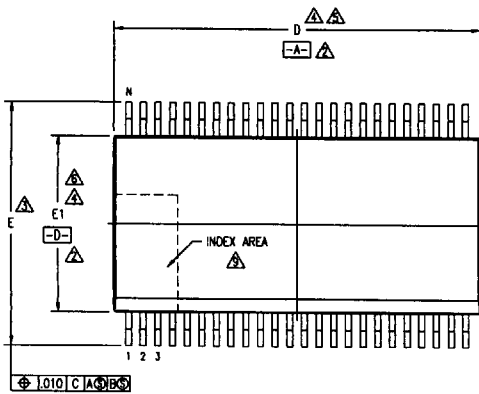
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 fax: 408-492-8674
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PACKAGE DIAGRAM OUTLINES

SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
XXX	±	PHONE: (408) 727-8118	
XXX		FAX: (408) 482-8874	
XXX		TWC: 910-338-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	08/15/90	PV PACKAGE OUTLINE	02
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	
		C	
		DRAWING No.	
		PSC-4029	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES SSOP (Continued)

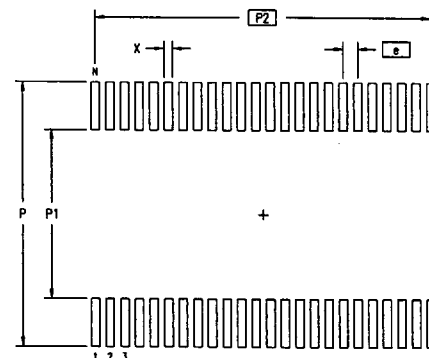
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

DWG #		S048-1				DWG #		S056-1			
SYMBOL	JEDEC VARIATION				NOTE	JEDEC VARIATION				NOTE	
	AA			AB							
	MIN	NOM	MAX	MIN		NOM	MAX				
A	.095	.102	.110			.095	.102	.110			
A1	.008	.012	.016			.008	.012	.016			
A2	.088	.090	.092			.088	.090	.092			
D	.620	.625	.630	4,5		.720	.725	.730	4,5		
E	.395	.405	.420	3		.395	.405	.420	3		
E1	.291	.295	.299	4,6		.291	.295	.299	4,6		
N	48					56					

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

LAND PATTERN DIMENSIONS



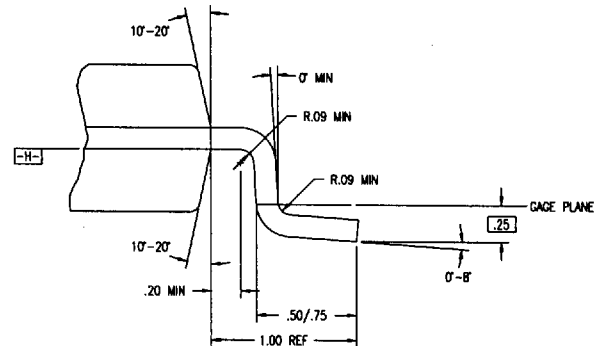
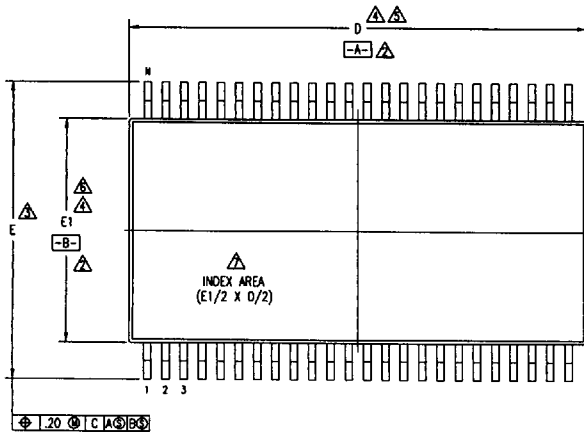
	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Stoner Way, Santa Clara, CA 95054	
X.XX	±	PHONE: (408) 727-8116	
X.XXX	±	FAX: (408) 482-8874	
X.XXX	±	TW: 810-338-2070	
APPROVALS	DATE	TITLE	REV
DRN	06/15/90	PV PACKAGE OUTLINE	02
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	
		C	
		DRAWING No.	
		PSC-4029	
		DO NOT SCALE DRAWING	

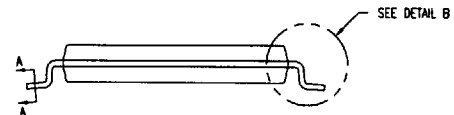
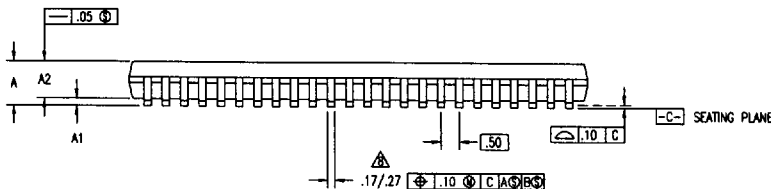
PACKAGE DIAGRAM OUTLINES

TSSOP

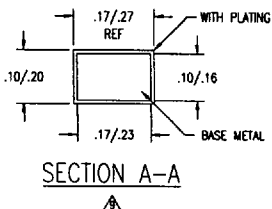
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	



DETAIL B



SEE DETAIL B



SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2975 Slender Way, Santa Clara, CA 95054	
XXX.X	±	PHONE: (408) 727-8118	
XXXX.X		FAX: (408) 492-8674	
XXXX.X		TW: 910-336-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	01/15/93	PA PACKAGE OUTLINE	
CHECKED		6.10 mm BODY WIDTH TSSOP	
		.50 mm PITCH	
		SIZE	DRAWING No.
		C	PSC-4039
			03
			DO NOT SCALE DRAWING

PACKAGE DIAGRAM OUTLINES TSSOP (Continued)

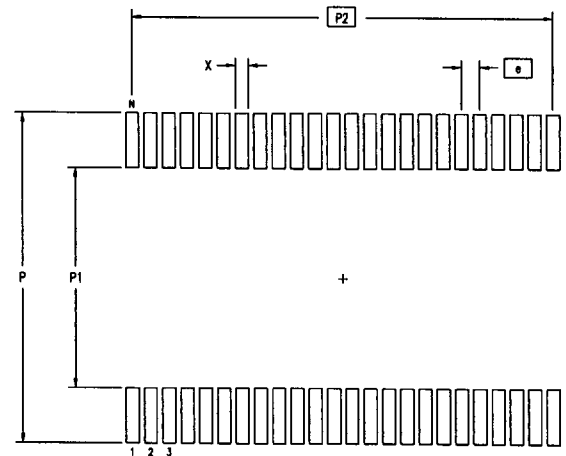
DWG #				S048-2		DWG #				S056-2		
SYMBOL	JEDEC VARIATION					NOTE	JEDEC VARIATION					NOTE
	ED						EE					
	MIN	NOM	MAX				MIN	NOM	MAX			
A	-	-	1.10				-	-	1.10			
A1	.05	-	.15				.05	-	.15			
A2	.85	1.00	1.05				.85	1.00	1.05			
D	12.40	12.50	12.60	4,5			13.90	14.00	14.10	4,5		
E	7.95	8.10	8.25	3			7.95	8.10	8.25	3		
E1	6.00	6.10	6.20	4,6			6.00	6.10	6.20	4,6		
N	48						56					

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- and $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

LAND PATTERN DIMENSIONS



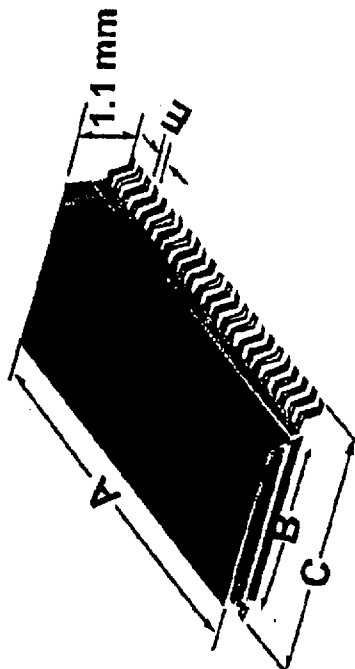
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50 BSC		13.50 BSC	
X	.30	.40	.30	.40
e	.50 BSC		.50 BSC	
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 482-8874 TWC: 910-338-2070	
DECIMAL	ANGULAR	TITLE PA PACKAGE OUTLINE 6.10 mm BODY WIDTH TSSOP .50 mm PITCH SIZE C DRAWING No. PSC-4039 DO NOT SCALE DRAWING	
10X	±		
100X			
1000X			
APPROVALS	DATE	REV	
DRAWN	01/19/93	03	
CHECKED			



TVSOP

The Most Compact Double Density Package

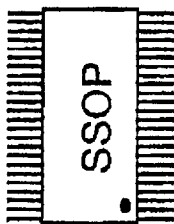


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50



Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

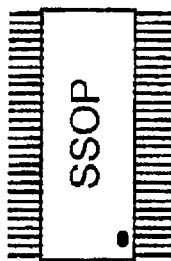


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²



9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0