Integrated Device Technology, Inc

64K (8K x 8) CMOS EEPROM MODULE

IDT78M64

FEATURES:

- Equivalent to JEDEC standard 8K x 8 monolithic EEPROM
- 8,192 x 8 CMOS EEPROM module complete with decoder and decoupling capacitor
- Fast access times
  - Military: 85ns (max.)
  - Commercial: 70ns (max.)
- On-chip timer
  - Automatic byte erase before write
  - Byte write 10ns max.
- $\overline{DATA}$ Polling—detection of write cycle completion
- Utilizes IDT78C16As—high-performance 16K EEPROMs
- Single 5V (±10%) power supply
- Data protection circuitry (V_{CC} lockout for V_{CC} < 3.8V)
- Provides data integrity on power up/power down
- Minimum endurance of 10,000 write cycles per byte
- Endurance failure rate < 0.1% per 1000 cycles
- Available in 28-pin, 600 mil DIP
- Military modules available with semiconductor components compliant to MIL-STD-883, Class B

DESCRIPTION:

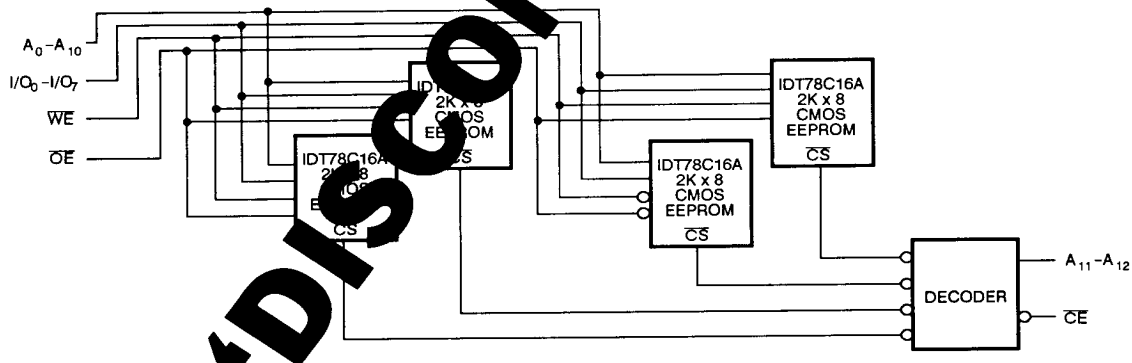
The IDT78M64 is a 5 volt only 8K x 8 Electrically Erasable Programmable Read-Only Memory (EEPROM) constructed on a co-fired ceramic substrate using four IDT78C16A (2K x 8) EEPROMs in leadless chip carriers. Functional equivalence to monolithic 64K EEPROMs is achieved by utilization of an on-board decoder circuit that interprets the higher order address A_{11} and A_{12} to select one of the four 2K x 8 EEPROMs.

The IDT78M64 offers a reduced power standby mode. When $\overline{CE}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as these conditions are held. In standby mode, the module dissipates less than 440mW. Substantially lower power levels can be achieved in the I_{SB1} mode (less than 20mW max.).

The pinout of the IDT78M64 is equivalent to monolithic 64K EEPROMs. Fast read access time allows zero wait state read cycles with high performance microprocessors.

All IDT module semiconductor components are manufactured in accordance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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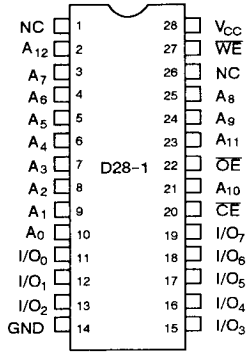
PIN CONFIGURATIONS



DIP
TOP VIEW

DEVICE OPERATIONAL MODE [1]

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 - I/O_7$
Read	V_{IL}	V_{IL}	V_{IH}	$DATA_{OUT}$ ($O_0 - O_7$)
Byte Write	V_{IL}	V_{IH}	V_{IL}	$DATA_{IN}$ ($I_0 - I_7$)
Standby	V_{IH}	Don't Care	Don't Care	High Z
Write Inhibit	Don't Care	V_{IL}	Don't Care	High Z
	Don't Care	Don't Care	V_{IH}	High Z

NOTE:
1. All control inputs are TTL-compatible.

PIN NAMES

$A_0 - A_{12}$	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$I/O_0 - I/O_7$	Data Input ($I_0 - I_7$) during write; Data Output ($O_0 - O_7$) during read

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READ MODE

Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) must be logically active in order for data to be available at the outputs. After a selected byte address is stable, $\overline{CE}$ is taken to a TTL LOW (enabling chip). The Write Enable ($\overline{WE}$) pin should remain deselected (TTL HIGH) during the entire read cycle. Data is gated from the device outputs by selecting the $\overline{OE}$ pin (TTL LOW).

WRITE MODE

The IDT78M64 is programmed electrically in-circuit and does not require any external latching, erasing or timing. Writing to the IDT78M64 is as easy as writing to a static RAM. When a write cycle is initiated the device automatically latches the address, data and control signals as it begins its write operation.

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The IDT78M64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. All inputs, except for data, are latched on the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Data is then latched in by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurred first. An automatic byte erase of the existing data at the addressed location is performed before the new data byte is written. Once initiated, a byte write operation will automatically proceed to completion within 10ms.

STANDBY MODE

The IDT78M64 features a standby mode which reduces the maximum active current from 250mA to 80mA for TTL levels and to 4mA for CMOS levels. With $\overline{CE} \geq V_{IH}$, all outputs are in the high impedance state.

DATA PROTECTION

Nonvolatile data is protected from inadvertent writes in the following manner:

Power Up/Down

On-chip circuitry provides protection against false write during V_{CC} power up/down. The IDT78M64 features an internal sensing circuit that disables the internal programming circuit if $V_{CC} < 3.8V$. This prevents input signals at $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ from triggering a write cycle during a V_{CC} power up/down event.

Noise Protection

The IDT78M64 will typically reject write pulses that are less than 15ns. This prevents the initiation of a write cycle by a noise occurence.

Write Inhibit

Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during a power-on and power-off will inhibit inadvertent writes.

$\overline{DATA}$ POLLING

The IDT78M64 has a maximum write cycle time of 10ms; a write will always be completed in less than the maximum cycle time. Write cycle completion is readily determined via a simple software routine ($\overline{DATA}$ Polling) that performs a read operation while the device is in an automatic write mode. If a read command (addressed to the last byte written) is given while the IDT78M64 is still writing, the inverse of the most significant bit (I/O_7 pin) of the last byte written will be present. True data is not released until the write cycle is completed. Thus, a $\overline{DATA}$ polling monitor of the output (or periodic read of the last written byte) for true data can be used to detect early completion of a write cycle.

ENDURANCE

IDT's EEPROM technology employs the industry accepted Fowler-Nordheim tunneling across a thin oxide. IDT78M64 EEPROM modules are designed and tested for applications requiring extended endurance.

The endurance failure mechanism associated with EEPROMs results from the charge trapping in the thin tunneling dielectric. This failure is a function of the number of write cycles that each byte in the part has experienced. Trapped charges accumulate slowly with each write cycle and eventually become large enough to prevent reliable writing to the cell. Since some bits may be more sensitive than others, an endurance failure is typically a single bit failure (i.e. a failure of a single bit to properly write or retain data).

To test for endurance, a sample of devices is written 10,000 times at every byte location and checked for data retention capability. IDT test screens ensure that shipped devices will write a minimum of 10,000 times (at every byte location) with a maximum failure rate of 1%. This means that up to 1% of a sample of devices will fail to write or retain data after being written to 10,000 times. Those devices that do fail typically have a single bit(s) that fails to retain data after being written.

For more detailed information please refer to the *IDT Reliability Report on Endurance*.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ENDURANCE

PARAMETER	VALUE	UNIT
Minimum Endurance	10,000	Cycles/Byte

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.3	0.4	0.8	V
V_{WI}	Write Inhibit	3.8	–	–	V

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 5.0V)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	28	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	33	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified

T_A = 0°C to +70°C V_{CC} = 5.0V ± 10% (Commercial)

T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)

V_{LC} = 0.2V V_{HC} = V_{CC} -0.2V

C_L = 30pF

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–	15	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	—	15	µA
I_{CC1}	Operating Power Supply Current V_{CC} = Max., f = 0	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	—	250	mA
I_{CC2}	Dynamic Operating Current V_{CC} = Max., f = f_{MAX}	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	—	250	mA
I_{SB}	Standby Power Supply Current (TTL Level)	$\overline{CE}$ ≥ V_{IH}, V_{CC} = Max., $I_{I/O}$ = 0mA V_{IN} ≥ V_{IH} or 0 ≤ V_{IN} ≤ V_{IL}	—	80	mA
I_{SB1}	Full Standby Power Supply Current (CMOS Level)	$\overline{CE}$ ≥ V_{HC}, V_{CC} = Max., $I_{I/O}$ = 0mA V_{IN} ≥ V_{CC} -0.2V or 0 ≤ V_{IN} ≤ 0.2V	—	4.0	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	V

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF)

SYMBOL	PARAMETER	MILITARY ONLY												UNIT
		78M6485/100 MIN.	78M6485/100 MAX.	78M64120/150 MIN.	78M64120/150 MAX.	78M64200 MIN.	78M64200 MAX.	78M64250 MIN.	78M64250 MAX.	78M64300 MIN.	78M64300 MAX.	78M64350 MIN.	78M64350 MAX.	
READ CYCLE														
t_{CE}	Chip Enable Access Time	–	85/100	–	120/150	–	200	–	250	–	300	–	350	ns
t_{AA}	Address Access Time	–	85/100	–	120/150	–	200	–	250	–	300	–	350	ns
t_{OE}	Output Enable to Output Valid	–	60/65	–	70	–	70	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z	0	30	0	30	0	30	0	30	0	30	0	30	ns
t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	0	30	0	30	0	30	0	30	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, C_L = 30pF)

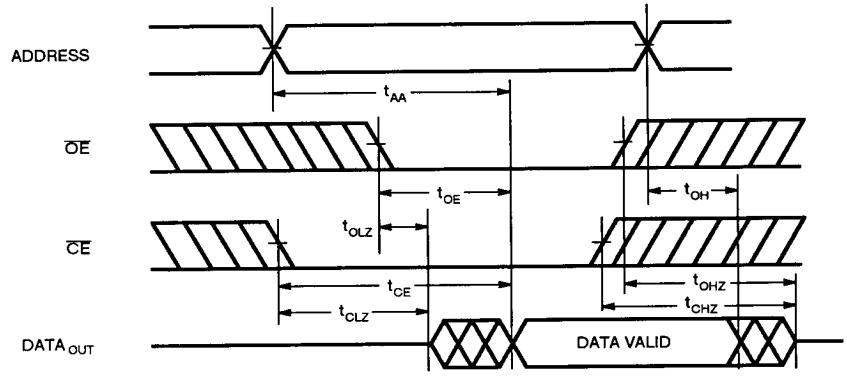
SYMBOL	PARAMETER	COMMERCIAL ONLY												UNIT
		78M6470 MIN.	78M6470 MAX.	78M6485 MIN.	78M6485 MAX.	78M64100 MIN.	78M64100 MAX.	78M64120 MIN.	78M64120 MAX.	78M64150 MIN.	78M64150 MAX.	78M64200 MIN.	78M64200 MAX.	
READ CYCLE														
t_{CE}	Chip Enable Access Time	–	70	–	85	–	100	–	120	–	150	–	200	ns
t_{AA}	Address Access Time	–	70	–	85	–	100	–	120	–	150	–	200	ns
t_{OE}	Output Enable to Output Valid	–	50	–	60	–	60	–	70	–	70	–	70	ns
t_{CLZ}	Chip Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OLZ}	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Disable to Output in High Z	0	20	0	20	0	20	0	20	0	20	0	20	ns
t_{OHZ}	Output Disable to Output in High Z	0	20	0	20	0	20	0	20	0	20	0	20	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} ± [illegible] All Temperature Ranges; C_L = 30pF)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
WRITE CYCLE				
t_{AS}	Address Set-up Time	5	–	ns
t_{AH}	Address Hold Time	50	–	ns
t_{DS}	Data Set-up Time	20	–	ns
t_{DH}	Data Hold from Write T[illegible]	15	–	ns
t_{OES}	Output Enable Set-up T[illegible]	5	–	ns
t_{OEH}	Chip Enable Hold [illegible]rite Time	15	–	ns
t_{CES}	Chip Enable S[illegible] Time	0	–	ns
t_{CEH}	Chip Enab[illegible]old T[illegible]	0	–	ns
t_{WP}	Write Pulse [illegible]	50	–	ns
t_{WB}	Byte Wri[illegible]ycle	–	10	ms
t_{DBV}	$\overline{DAT}$[illegible]ling to $\overline{DATA}$ Valid	–	t_{OE}	
t_{WH}	Write Hold Time	15	–	ns
t_{DP}	End of Write Pulse to $\overline{DATA}$ Polling	15	–	ns
t_{WES}	Write Enable Set-up Time	0	–	ns
t_{WEH}	Write Enable Hold Time	0	–	ns
t_{DV}	Data Valid Time	–	1	µs

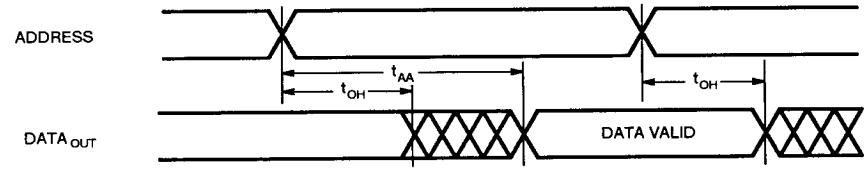
NOTES:
1. Data must be valid within 1µs maximum and must remain valid if t_{WP} is longer than 1µs.
2. This parameter is guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



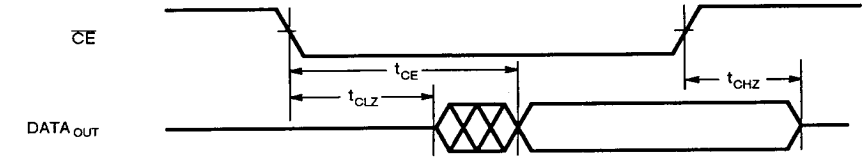
NOTE:
1. $\overline{WE}$ is HIGH for Read Cycle.

TIMING WAVEFORM OF READ CYCLE NO. 2[1]



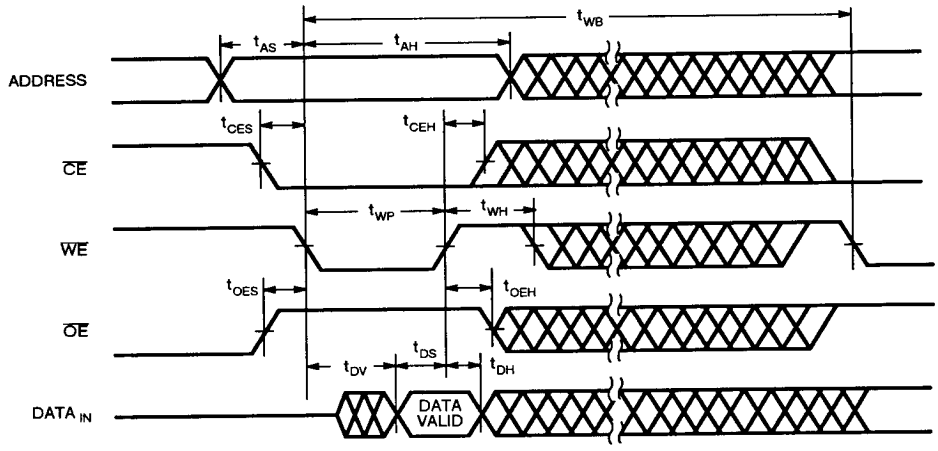
NOTE:
1. $\overline{WE}$ is HIGH; $\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IL}

TIMING WAVEFORM OF READ CYCLE NO. 3[1]

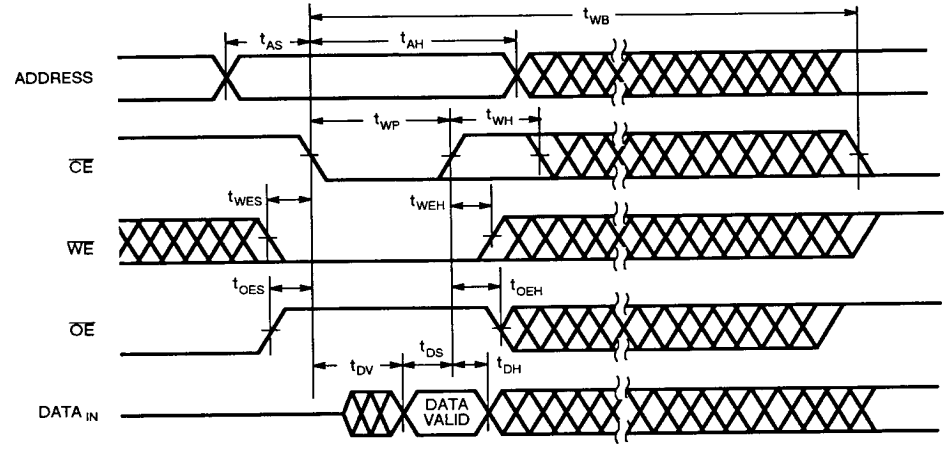


NOTE:
1. $\overline{WE}$ is HIGH; $\overline{OE}$ = V_{IL}; address valid prior to or coincident with $\overline{CE}$ transition LOW.

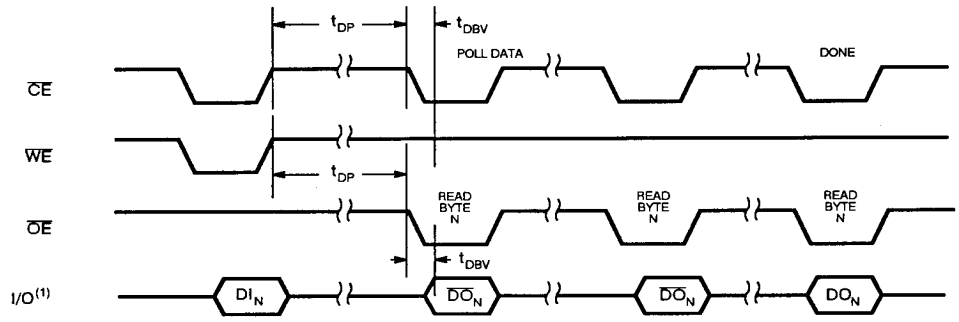
TIMING WAVEFORM OF WRITE CYCLE NO. 1, $\overline{WE}$ CONTROLLED



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED

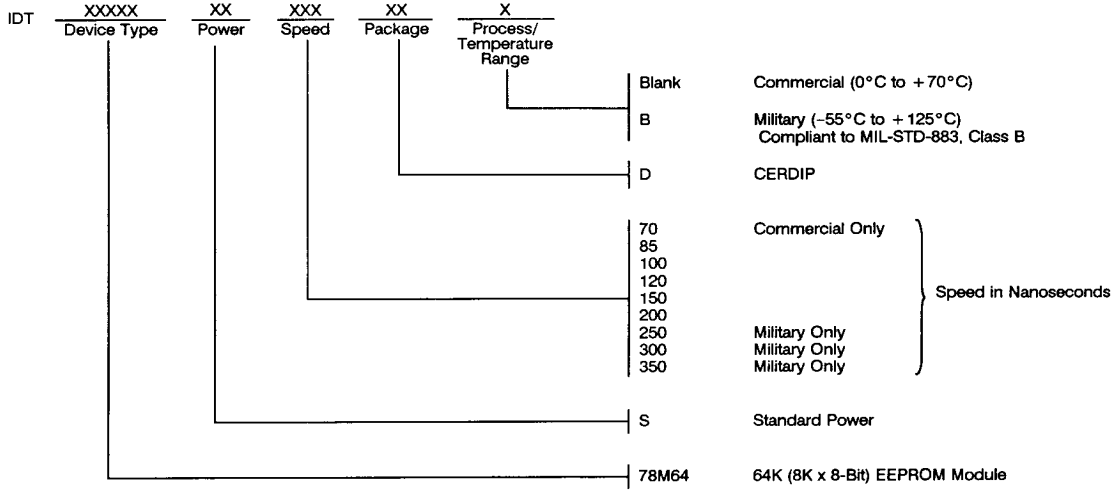


$\overline{\text{DATA}}$ POLLING



NOTE:
1. Most significant bit of the byte being written is inverted and available at I/O_7 if a Read command is issued. All other outputs are high impedance at this time. True data will not be released until the Write cycle is completed.

ORDERING INFORMATION



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